

Computer-Aided VLSI System Design

FPGA Lab

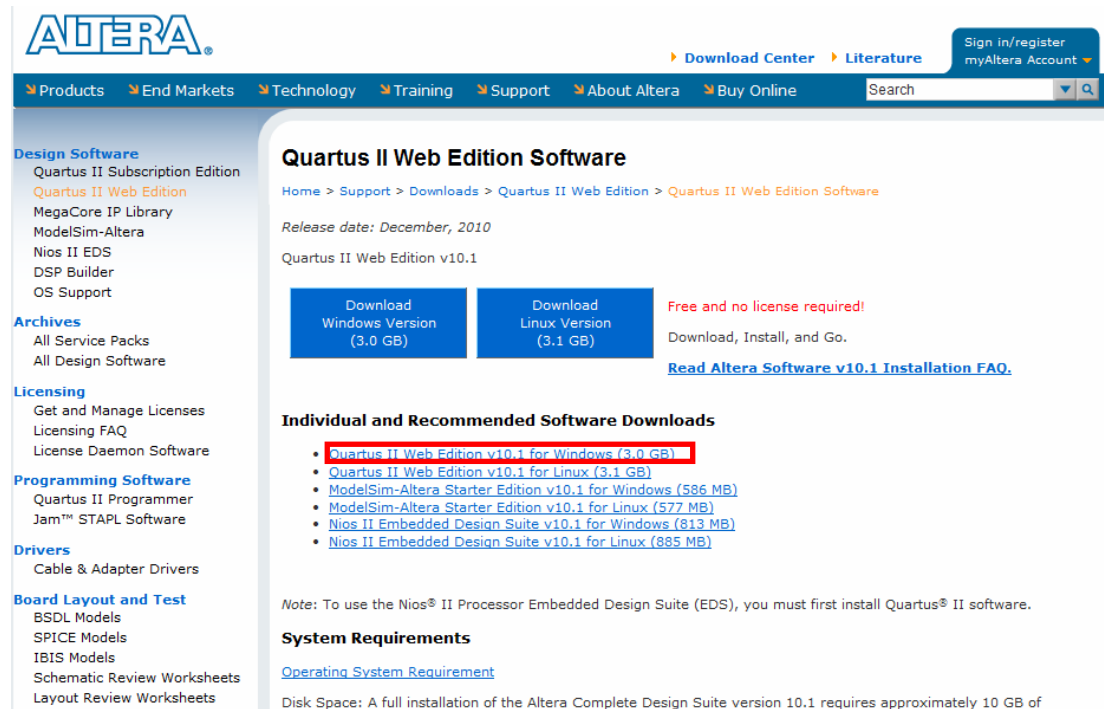
- 一、ALTERA Quartus II Web Edition Software 下載安裝過程
- 二、安裝 USB-Blaster Driver 讓電腦可以透過 USB 與 FPGA 溝通
- 三、實驗步驟

一、ALTERA Quartus II Web Edition Software 下載安裝過程

1. 打開 IE，進入 ALTERA Quartus II Web Edition Software 下載網址

<https://www.altera.com/download/software/quartus-ii-we>

點選 Quartus II Web Edition v10.1 for Windows (3.0 GB)軟體下載



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- License Daemon Software

Programming Software

- Quartus II Programmer
- Jam™ STAPL Software

Drivers

- Cable & Adapter Drivers

Board Layout and Test

- BSDL Models
- SPICE Models
- IBIS Models
- Schematic Review Worksheets
- Layout Review Worksheets

Quartus II Web Edition Software

Home > Support > Downloads > Quartus II Web Edition > Quartus II Web Edition Software

Release date: December, 2010

Quartus II Web Edition v10.1

Download Windows Version (3.0 GB) Download Linux Version (3.1 GB) Free and no license required! Download, Install, and Go. Read Altera Software v10.1 Installation FAQ.

Individual and Recommended Software Downloads

- Quartus II Web Edition v10.1 for Windows (3.0 GB)
- Quartus II Web Edition v10.1 for Linux (3.1 GB)
- ModelSim-Altera Starter Edition v10.1 for Windows (586 MB)
- ModelSim-Altera Starter Edition v10.1 for Linux (577 MB)
- Nios II Embedded Design Suite v10.1 for Windows (813 MB)
- Nios II Embedded Design Suite v10.1 for Linux (885 MB)

Note: To use the Nios® II Processor Embedded Design Suite (EDS), you must first install Quartus® II software.

System Requirements

[Operating System Requirement](#)

Disk Space: A full installation of the Altera Complete Design Suite version 10.1 requires approximately 10 GB of

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 Password
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Enter your email address.

(If your email address already exists in our system we will retrieve the associated information.)

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Enter your email address.

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3. 填寫資料有「*」是必填的部分，其中 email address、帳號、密碼一定要設定正確。填完後按 Create Account

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(Note: Data must be entered in English)

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 * Company Name
 * Address
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 * City
 * Country
 State / Province (Outside of USA)
 Zip / Postal Code
 E-mail Address [\(Edit Email\)](#)
 * Telephone Number
 Example: +6046366100x1234
 Language Preference
 * My primary job function is
 * My preferred distributor is

*** For what end applications do you design? (check all that apply)**

- | | |
|--|---|
| ☐ Academic/Research | ☐ Military or Aerospace |
| ☐ Automotive | ☐ Semiconductors |
| ☐ Computing and Office Automation | ☐ Storage Systems |
| ☐ Consumer Electronics or Digital Entertainment | ☐ Test and Measurement Equipment |
| ☐ Digital Broadcast | ☐ Wireless Communications |
| ☐ Industrial | ☐ Wireline Communications |
| ☐ Medical Equipment | ☒ Other |

*** Please check all topics that interest you:**

- | | |
|--|---|
| ☒ CPLDs | ☐ HardCopy ASICs |
| ☐ Digital signal processing | ☐ High-density FPGAs |
| ☐ Embedded processors | ☐ Low-cost FPGAs |

*** When was the last time you designed with an Altera® product?**

- ☐ I'm currently designing with Altera products
☐ More than 1 year ago
☒ Never

- ☐ Yes, I'd like to receive product announcement and update emails from Altera.
☐ Yes, I'd like to receive the Inside Edge-Altera's Monthly eNewsletter.

*** Create User Name** (3-20 characters, no spaces)

*** Create Password** (Minimum 6 characters)

*** Confirm password**

☒ I agree to the [Terms of Service](#)

☐ Remember me

* Indicates required field.

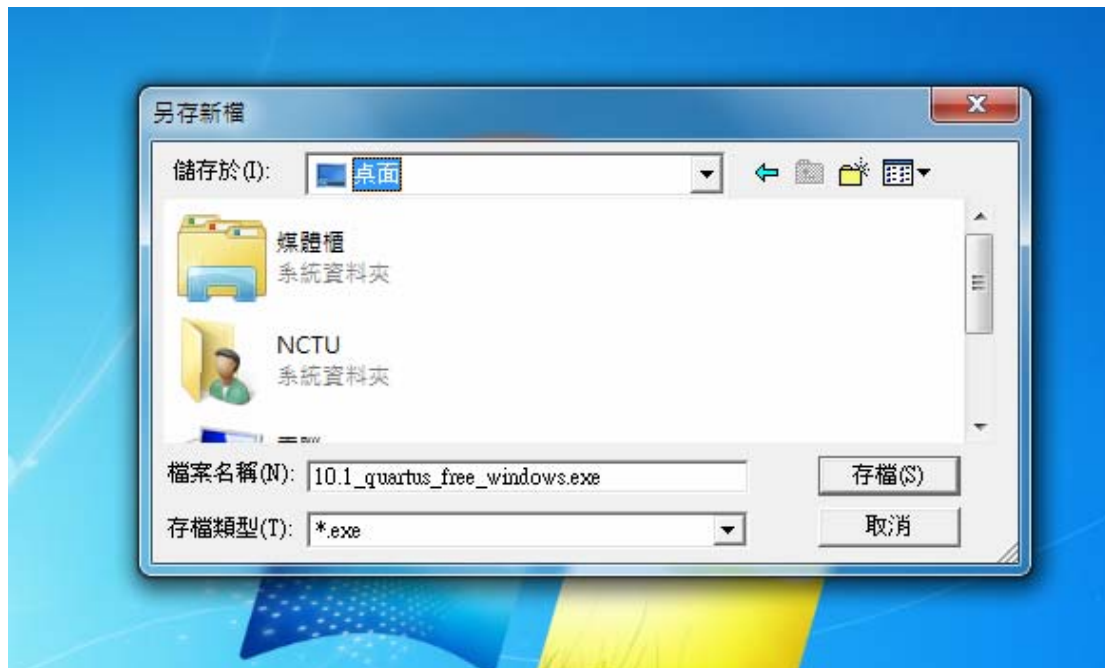
4. 出現訊息告知系統有送出 email 到您信箱，按下 Continue 可開始下載檔案

The screenshot shows the 'Your myAltera Account has been Created' page. The top navigation bar includes links for Products, End Markets, Technology, Training, Support, About Altera, and Buy Online, along with a search bar. The left sidebar contains 'myAltera Account' with sub-links: How to Register, Terms and Conditions, and Help. The main content area has a breadcrumb trail: Home > Support > mySupport > Your myAltera Account has been Created. The text states: 'Thank you for registering with Altera! You now have a myAltera account. We are sending you a confirmation email for your reference. You can use this account to register for classes, download software, file a service request and much more.' Below this text are two buttons: 'Continue' and 'Rate This Page' (which is checked). At the bottom, there is a footer with a copyright notice: 'Copyright © 1995-2010 Altera Corporation. All Rights Reserved.' and a row of social media icons: Altera Forum, Twitter, RSS, Facebook, Flickr, YouTube, and Email Updates.

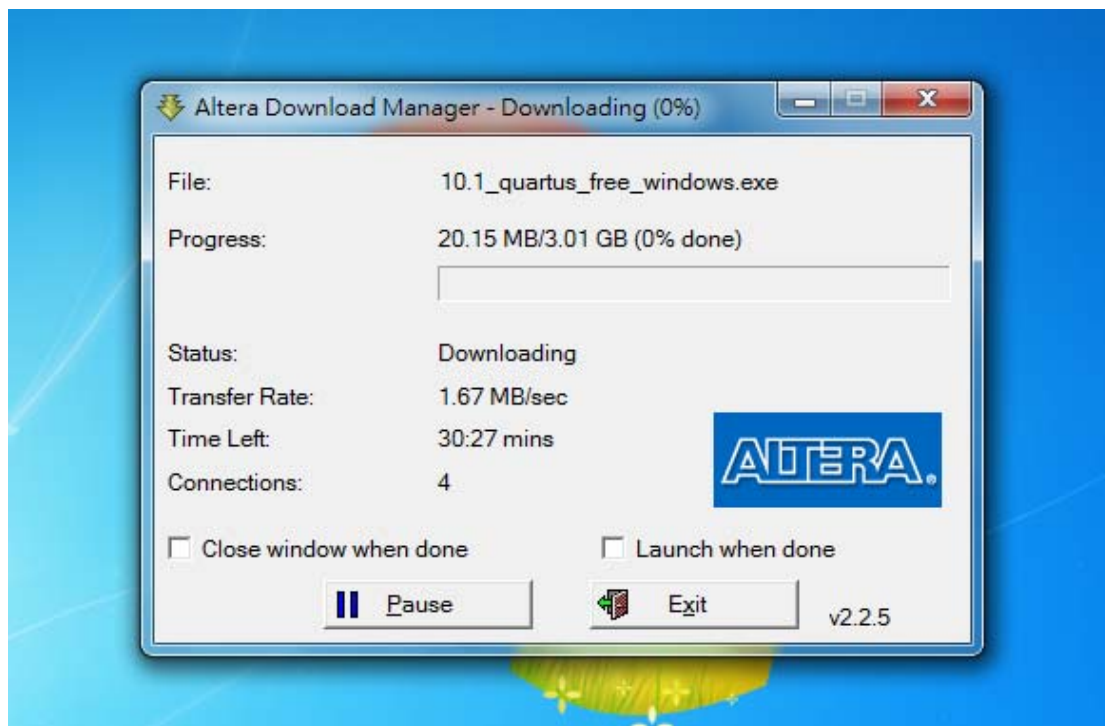
5. 如果之後想重新下載檔案，可以回到之前的申請帳號頁面，填入剛剛申請的帳號密碼後按下 Sign In 下載檔案

The screenshot shows the 'myAltera Account Sign-In' page. The top navigation bar is the same as the previous page. The left sidebar is also the same. The main content area has a breadcrumb trail: Home > Support > mySupport > myAltera Account Sign-In. The sign-in form is highlighted with a red rectangle and includes fields for 'User Name' (containing 'twusatw0') and 'Password' (masked with dots). There is a 'Remember me' checkbox and a 'Sign In' button. A link 'Forgot Your User Name or Password?' is also present. Below the sign-in form is a section titled 'Don't have an account?' with two options: 'Create Your myAltera Account' and 'Get One-Time Access'. The 'Create Your myAltera Account' option includes a text input for 'Enter your email address.' and a 'Create Account' button. The 'Get One-Time Access' option includes a text input for 'Enter your email address.' and a 'Get One-Time Access' button. A checkbox for 'Yes, I'd like to receive product announcement and update emails from Altera.' is also present.

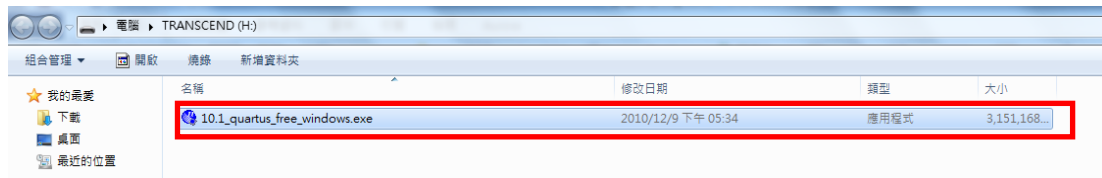
6. 剛剛按下 Sign In 後會詢問安裝檔要存在哪裡，選擇一個資料夾後按存檔



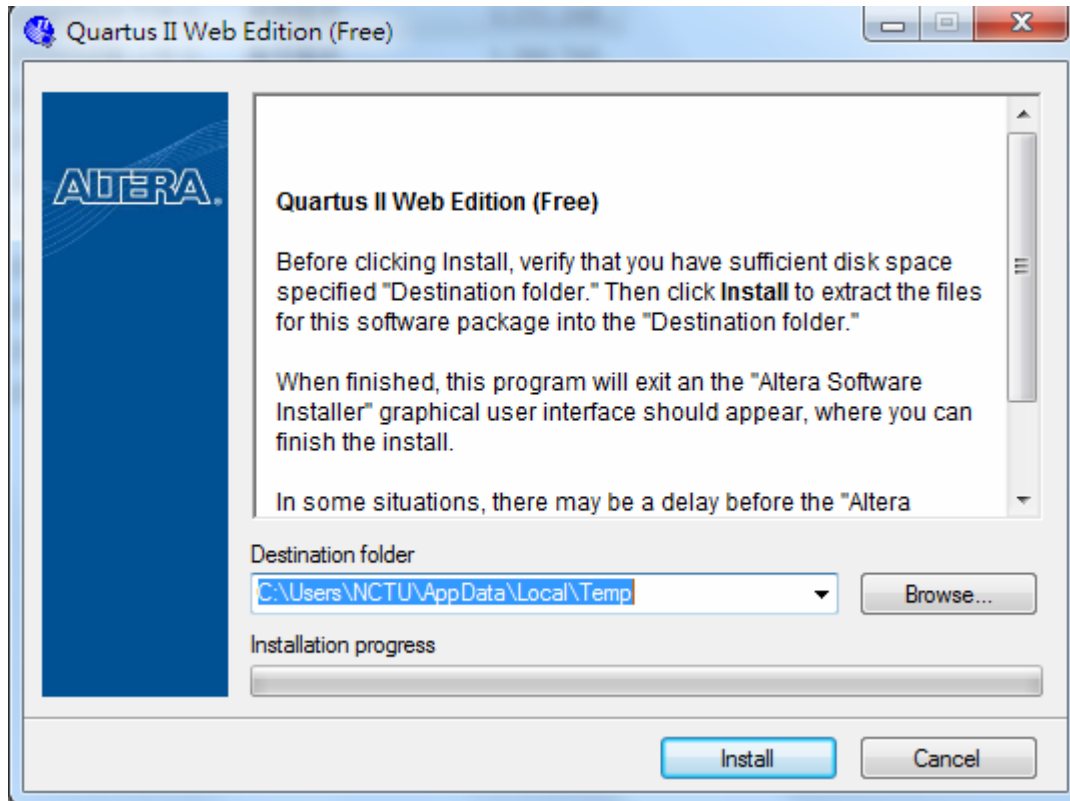
7. 按下存檔後會跳出下載畫面，等待一段時間直到下載結束



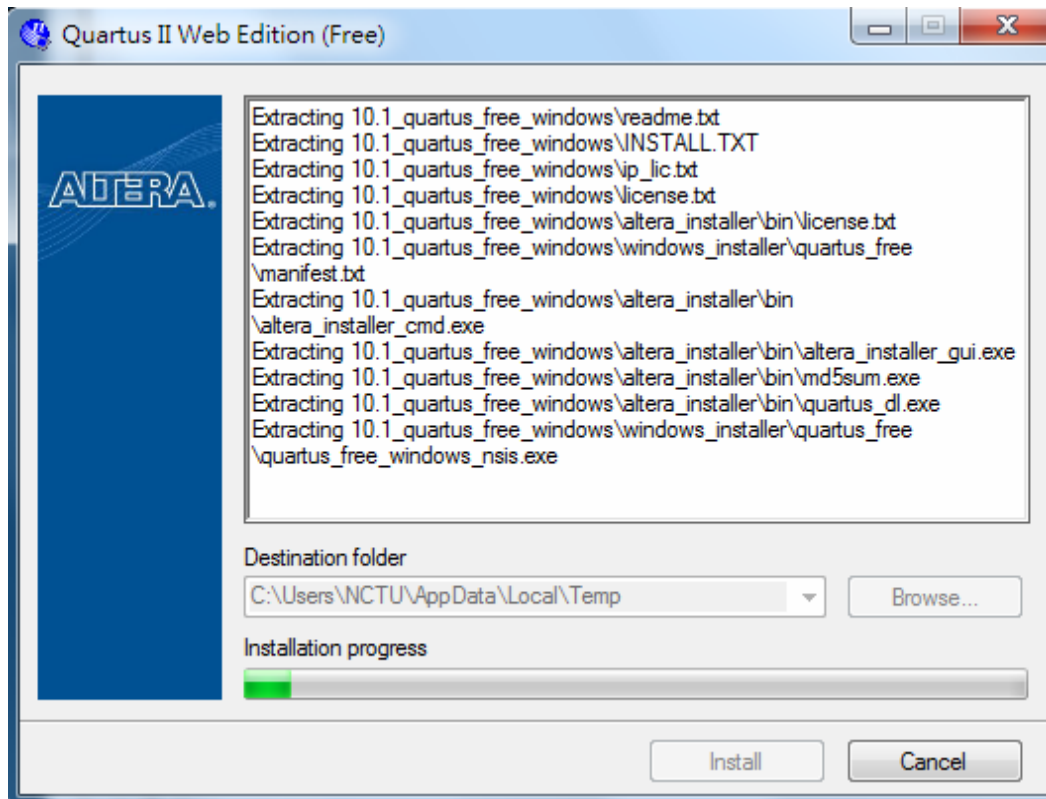
8. 點兩下執行檔進行安裝



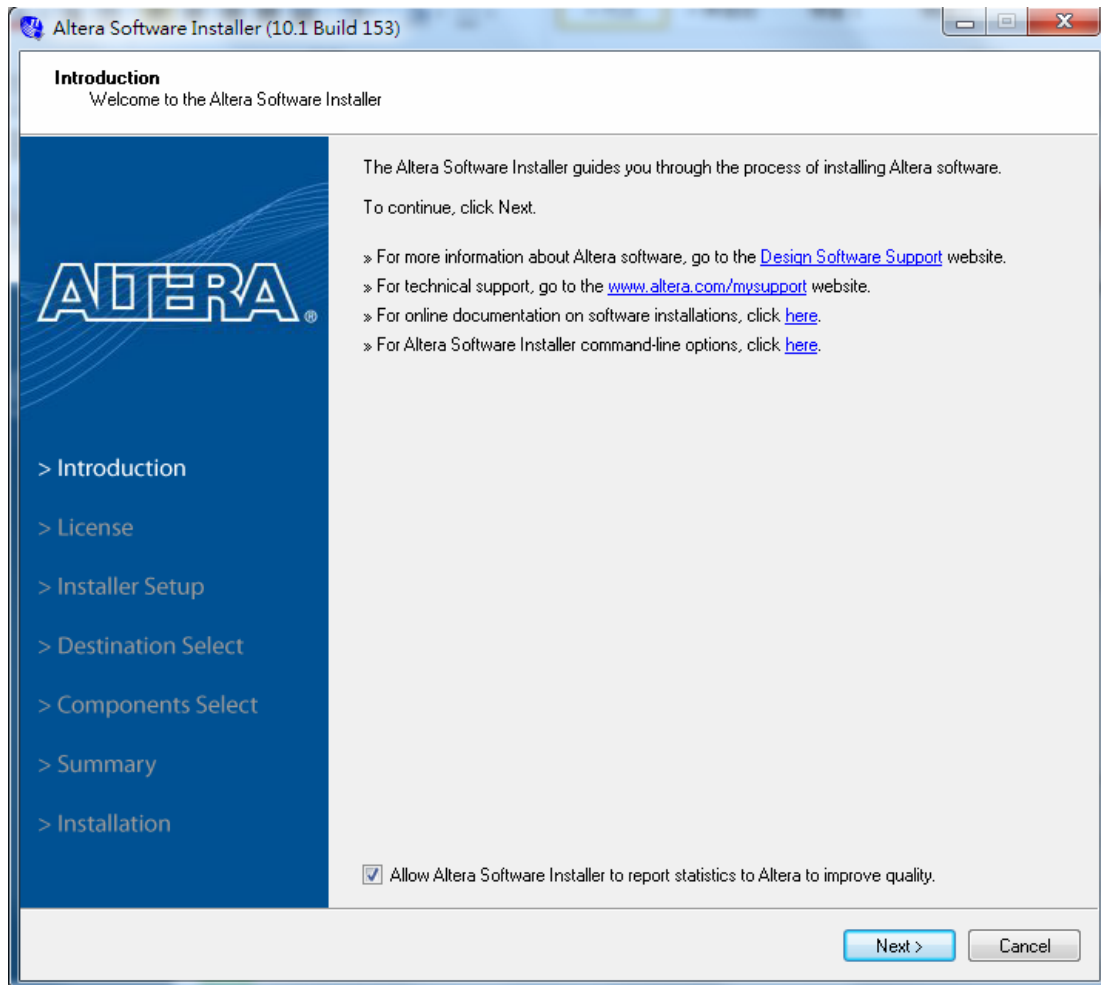
9. 出現第一個安裝畫面，點選 Install



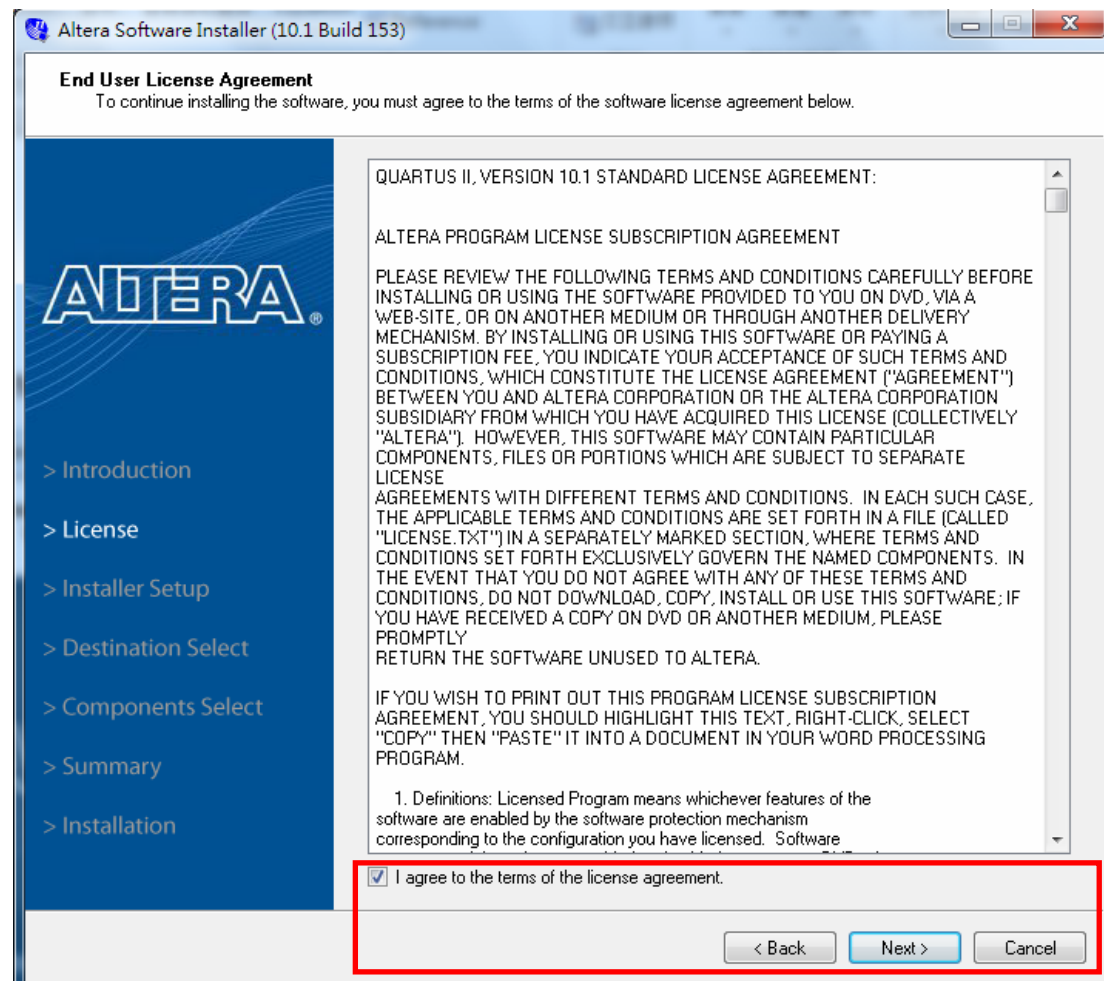
10. 出現 Extracting 的畫面



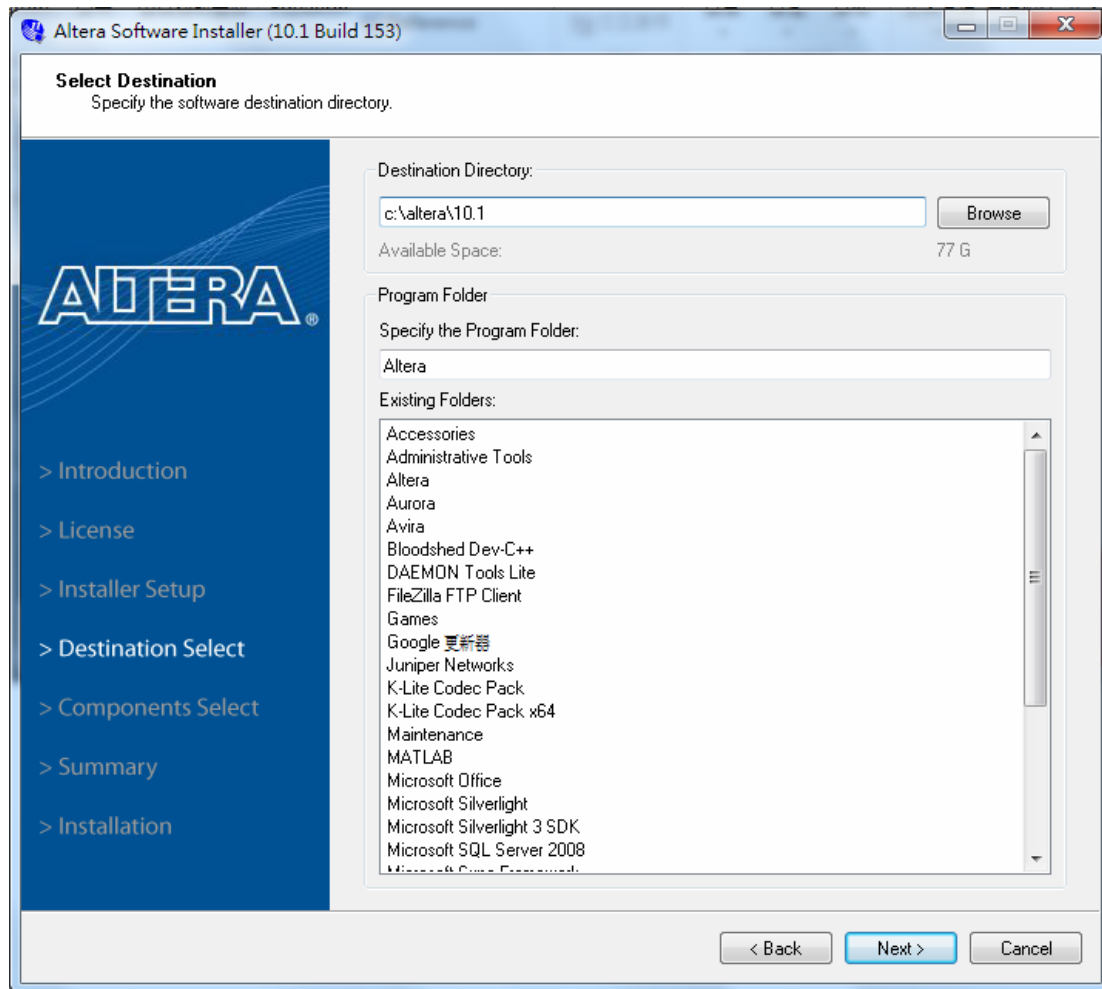
11. Extracting 完後，點選 Next 繼續安裝



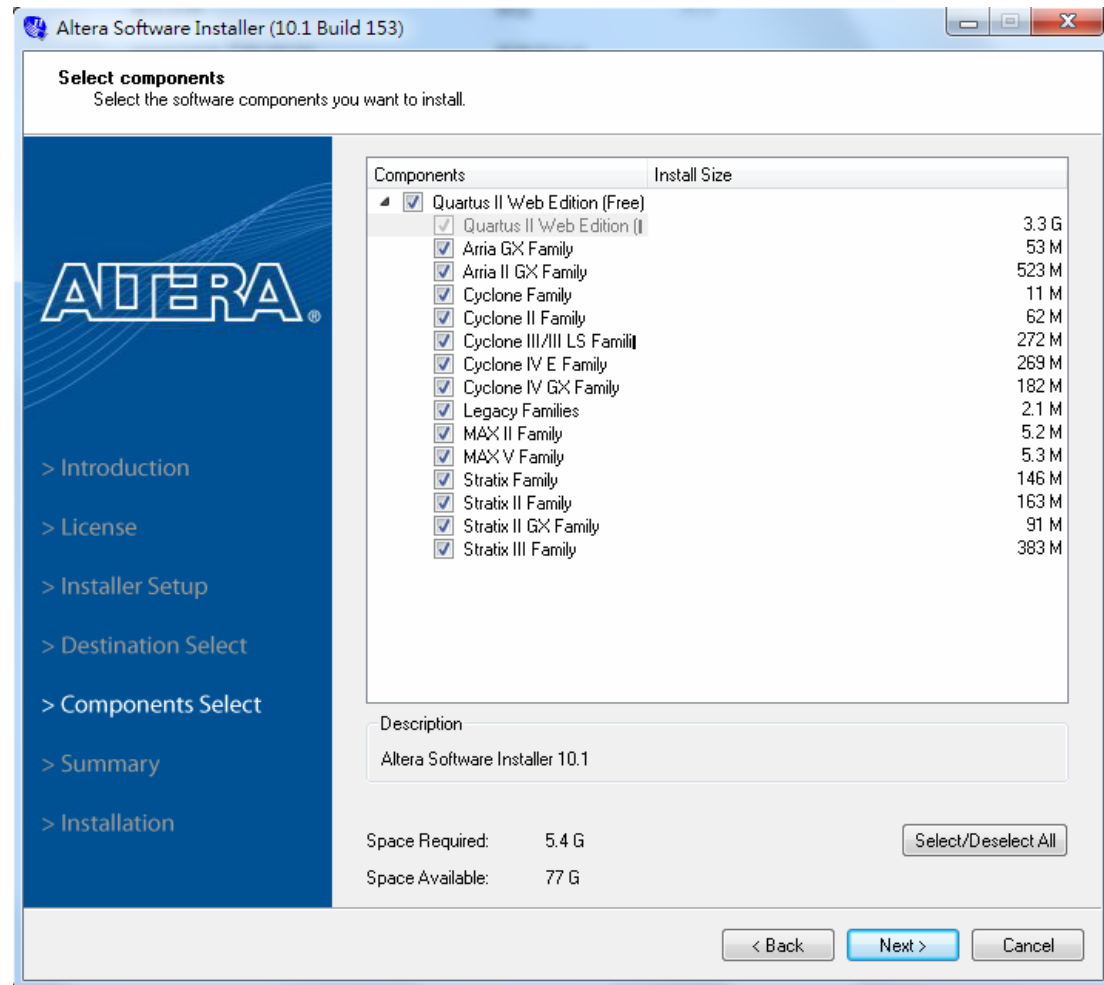
12. 勾選 I agree to the terms of the license agreement 並按下 Next 繼續安裝



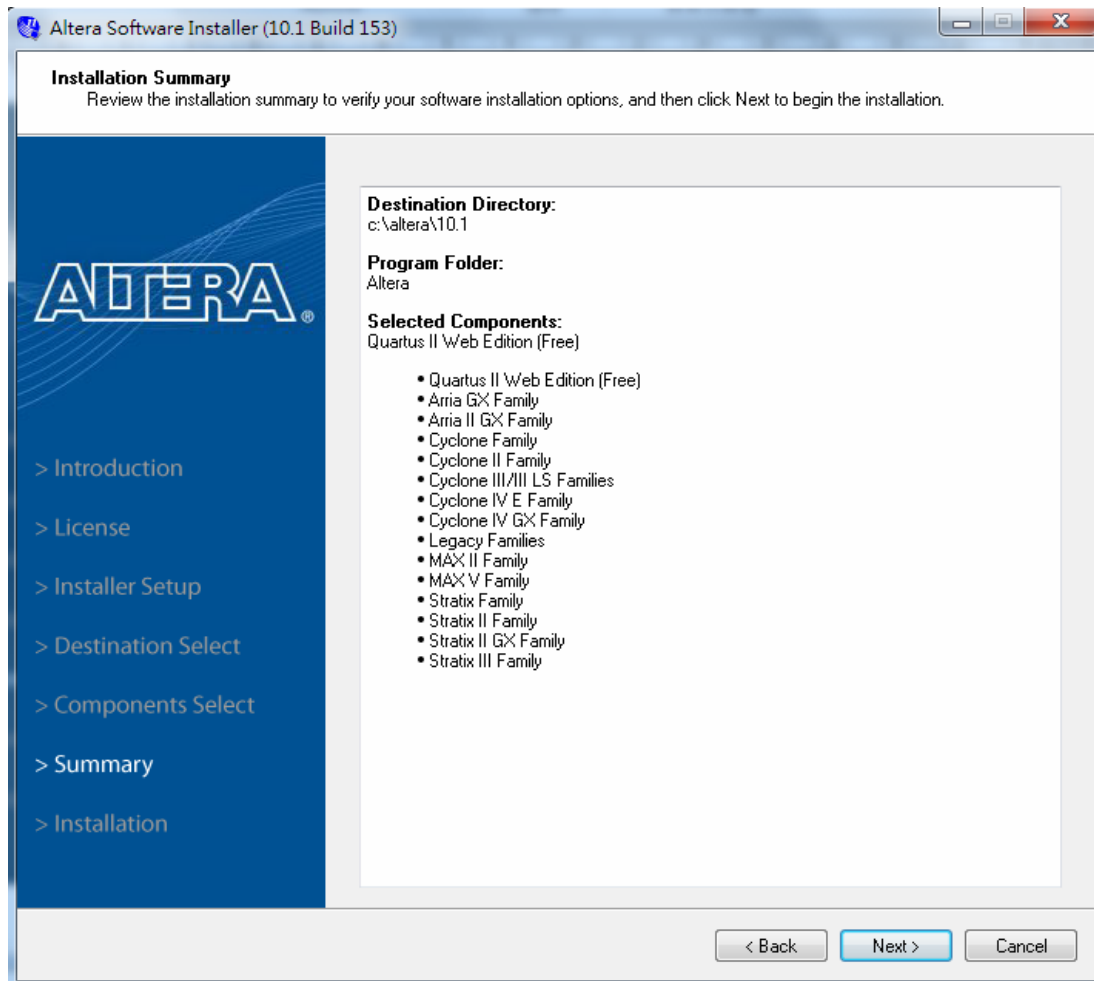
13. 按下 Next 繼續安裝



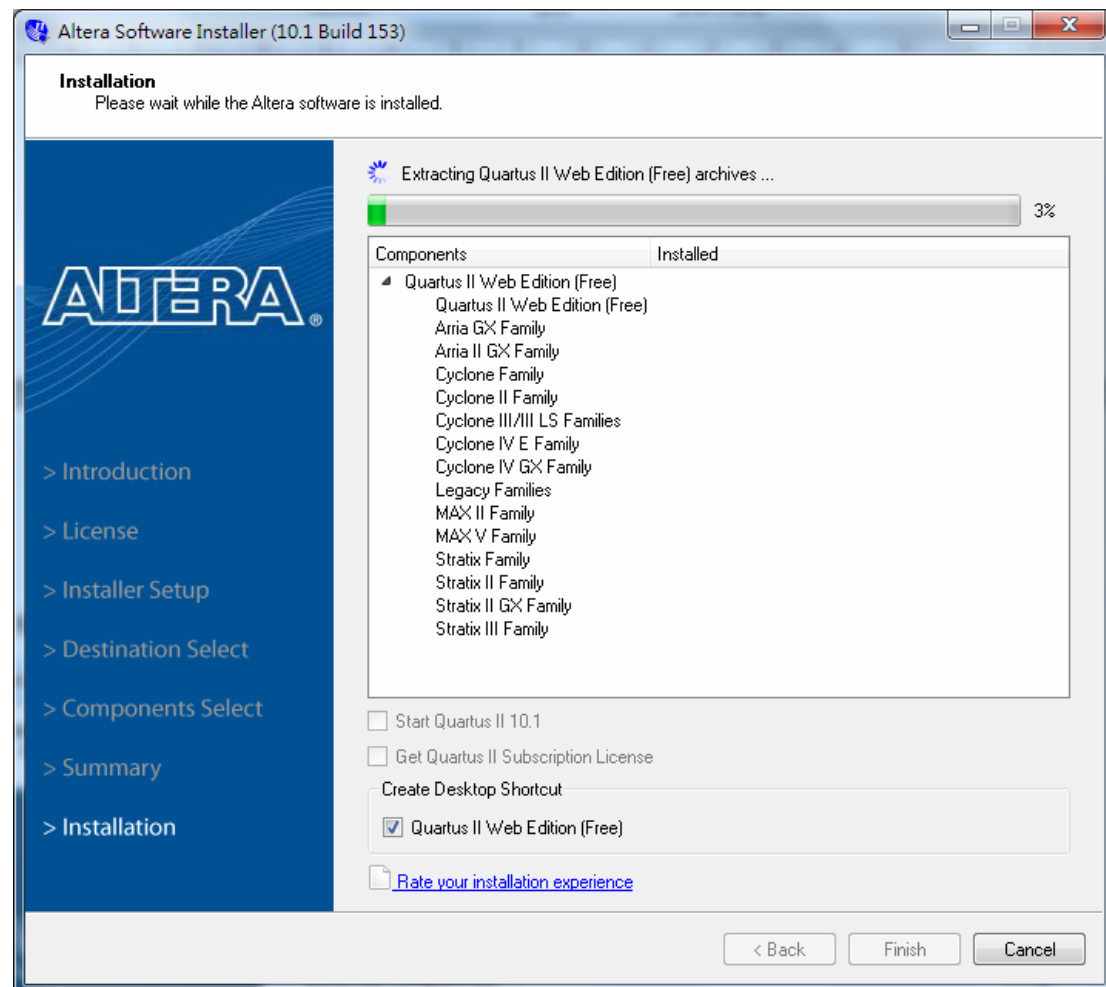
14. 按下 Next 後繼續安裝



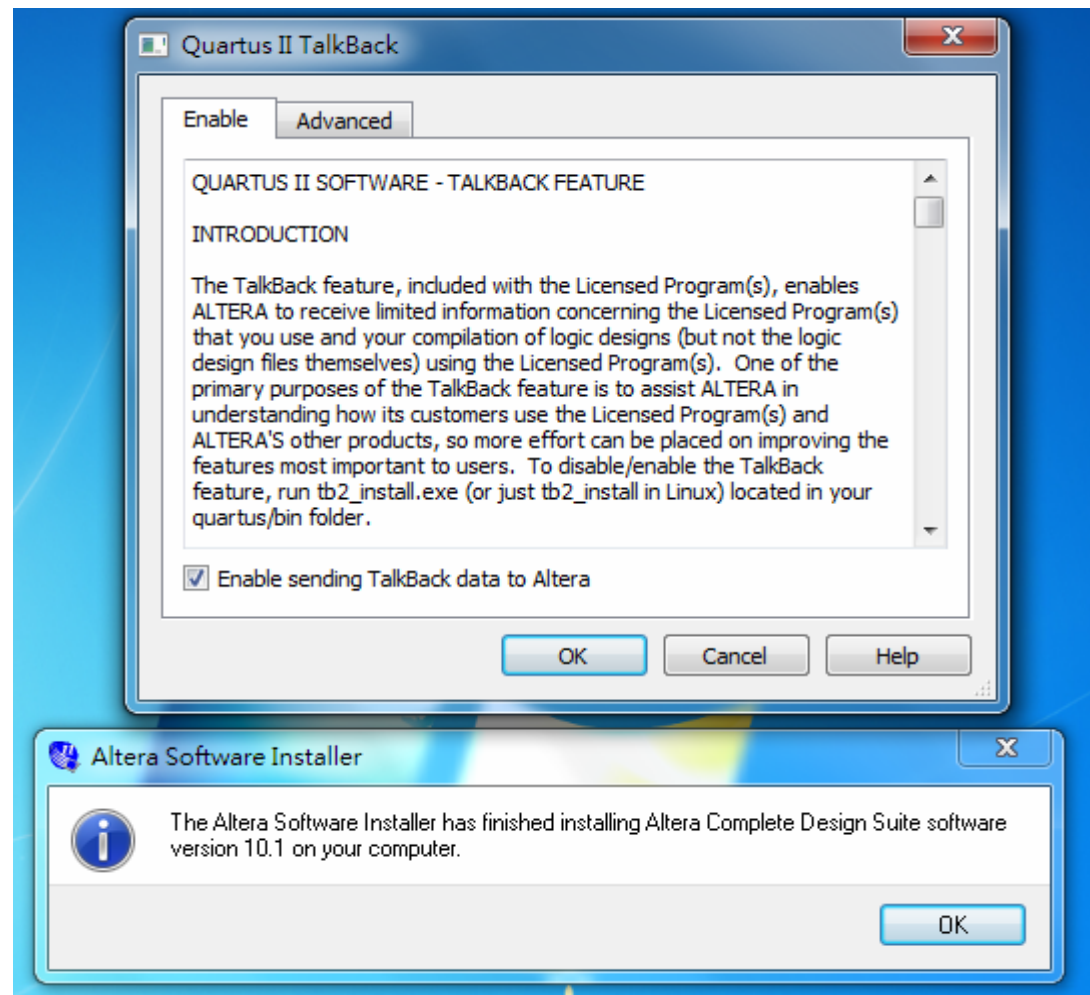
15. 按下 Next 後繼續安裝



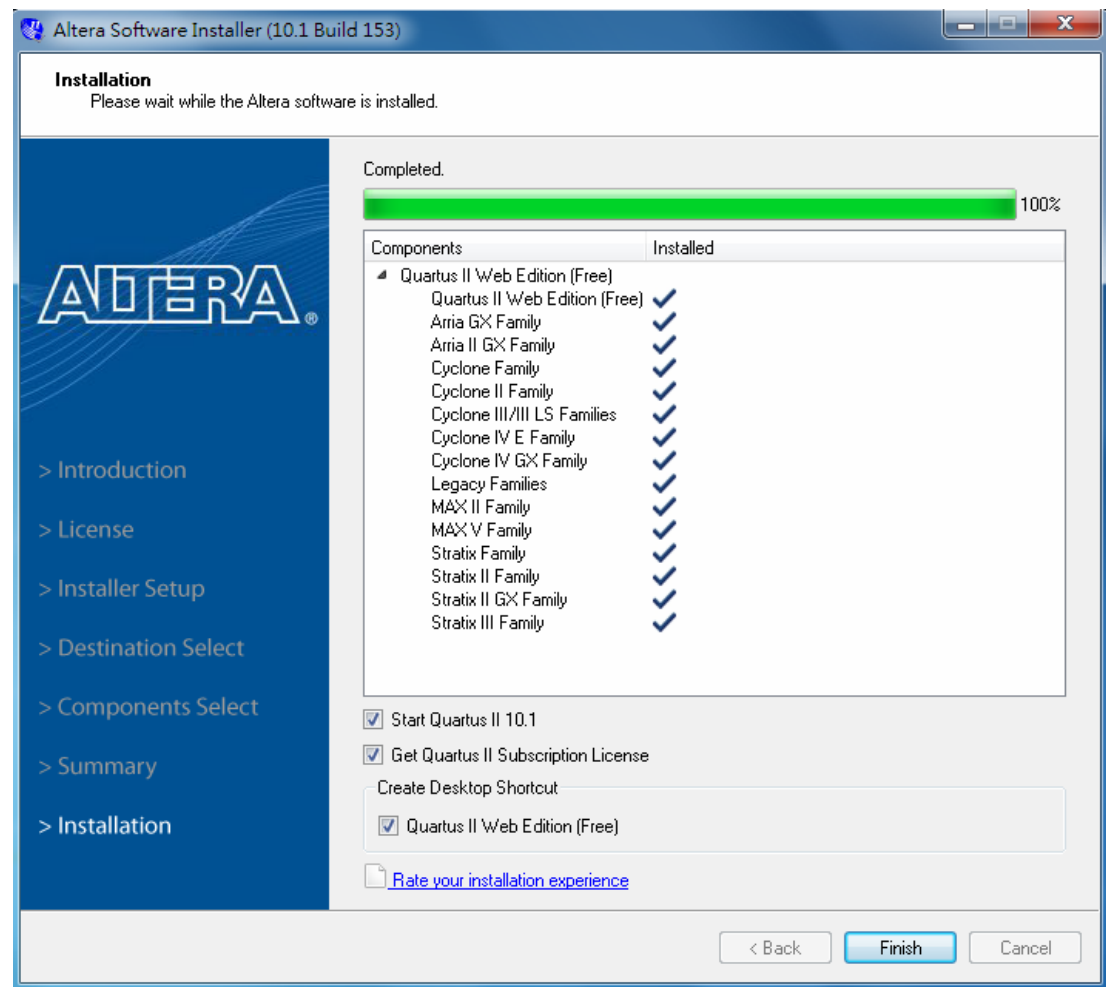
16. 出現安裝中的畫面



17. 安裝中出現這兩個畫面，都點選 OK



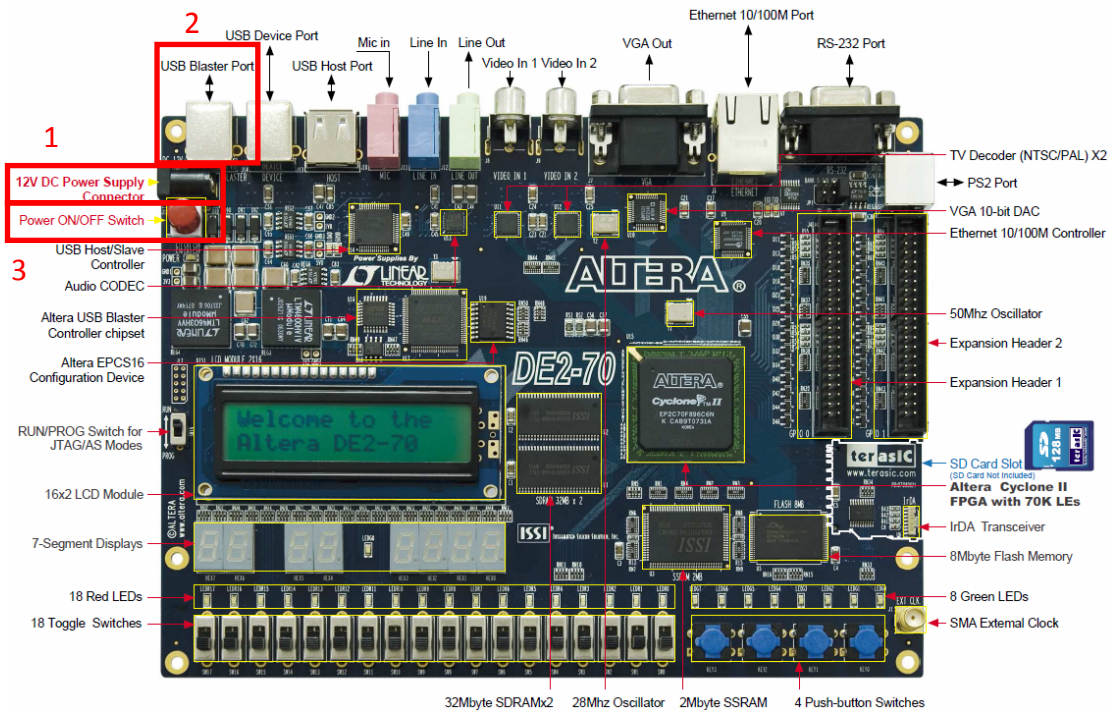
18. 按 Finish 結束安裝



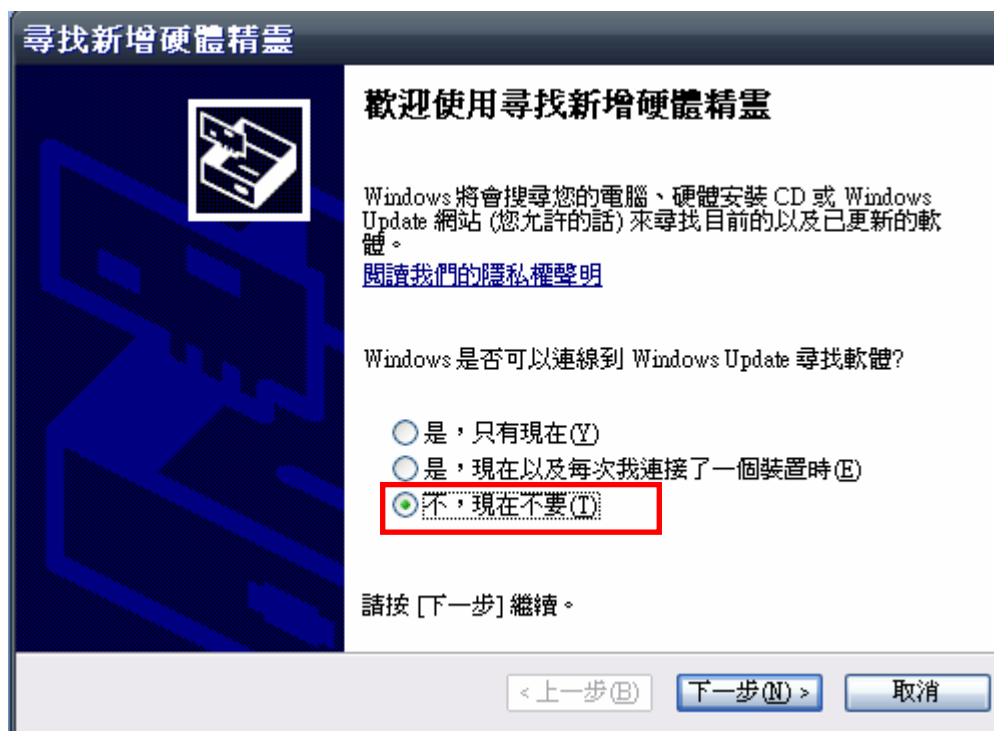
之後會自動開啓 Quartus II 軟體代表安裝成功！
(整個安裝過程約在半小時內結束)

二、安裝 USB-Blaster Driver 讓電腦可以透過 USB 與 FPGA 溝通

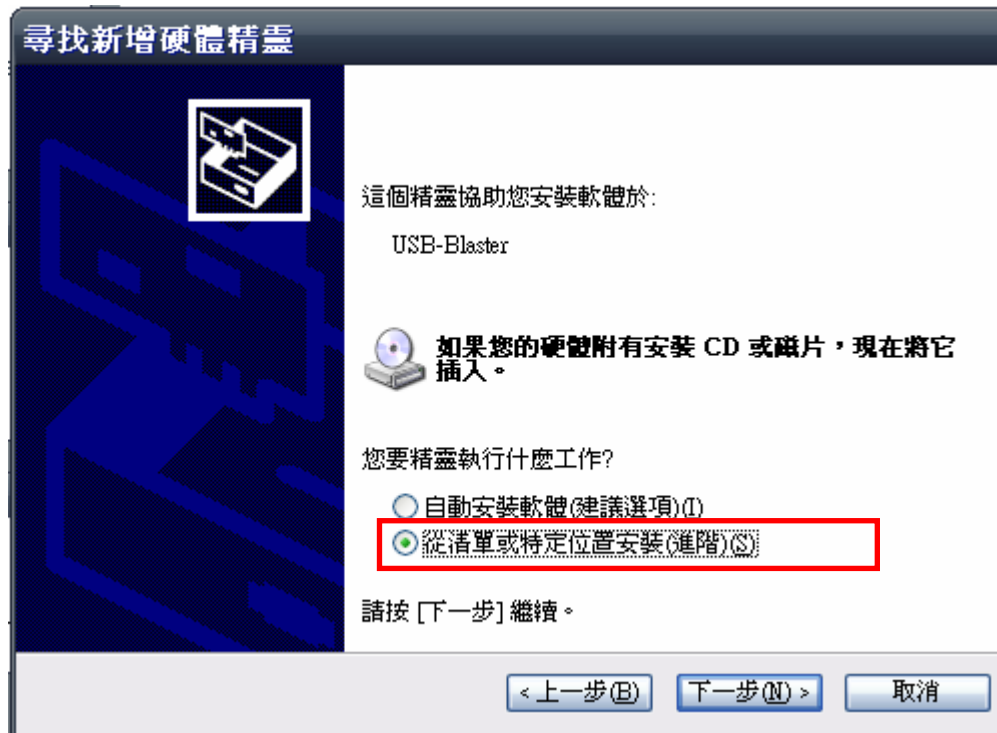
1. 接上電源線(1)與 USB(2)



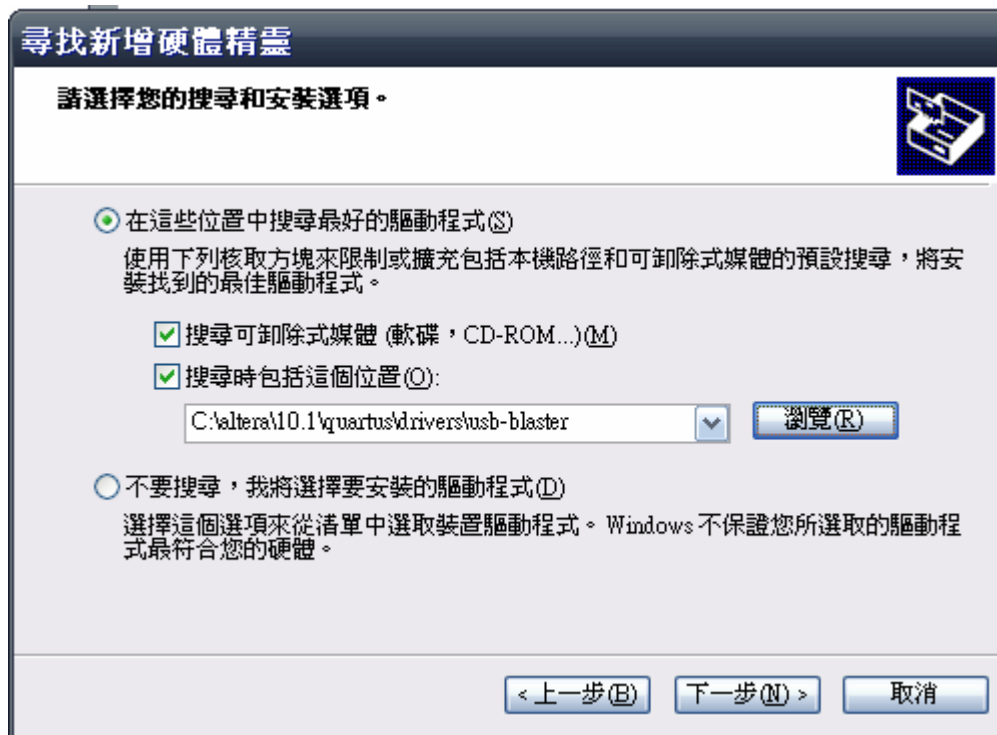
2. 打開 FPGA 的電源(3)後，將與 FPGA 相連的 USB 線插入電腦中，會出現找到新硬體的畫面，選擇「不，現在不要」後按下「下一步」



3. 選擇「從清單或特定位置安裝」後按下「下一步」



4. 根據以下畫面進行設定，並透過「瀏覽」設定 driver 所在的資料夾為 C:\altera\10.1\quartus\drivers\usb-blaster 最後按下「下一步」



5. 過程中會連續出現以下兩個畫面

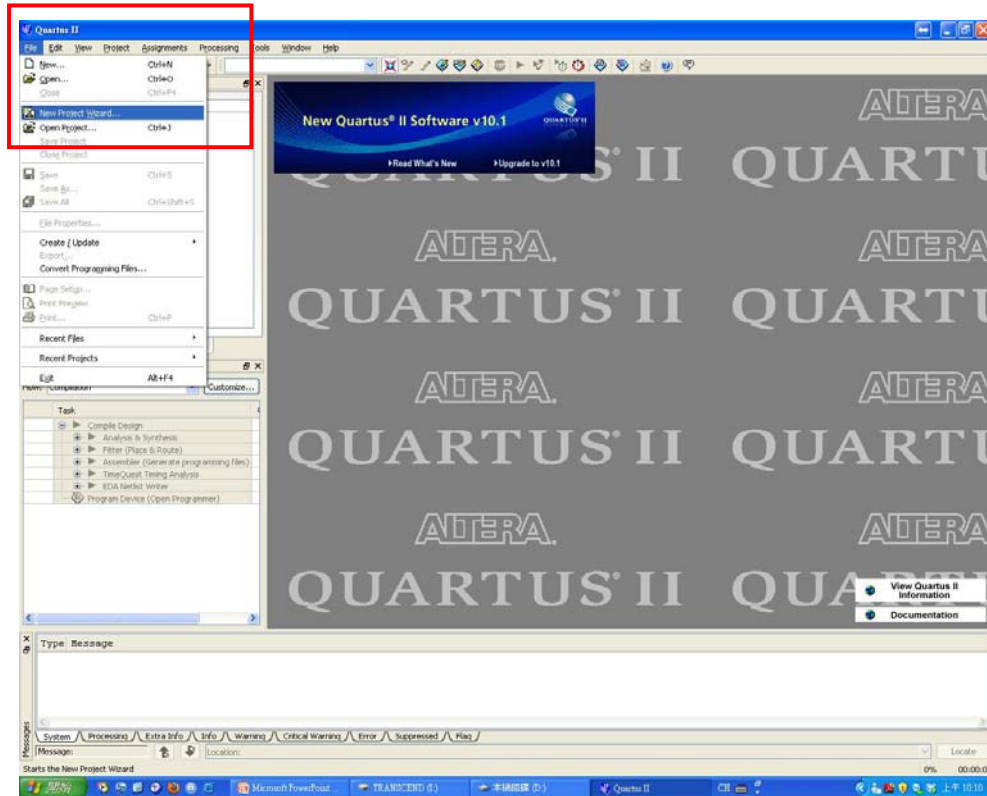


6. 最後按下「完成」完成安裝

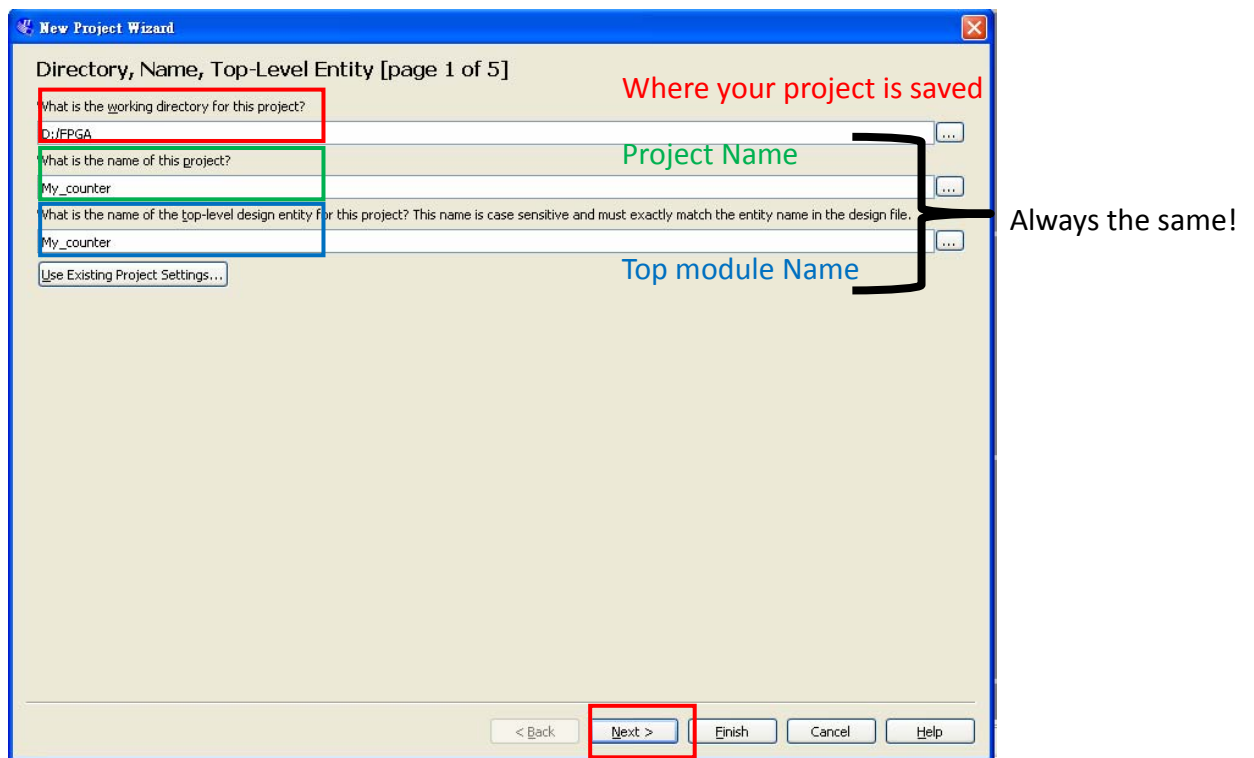


三、實驗步驟

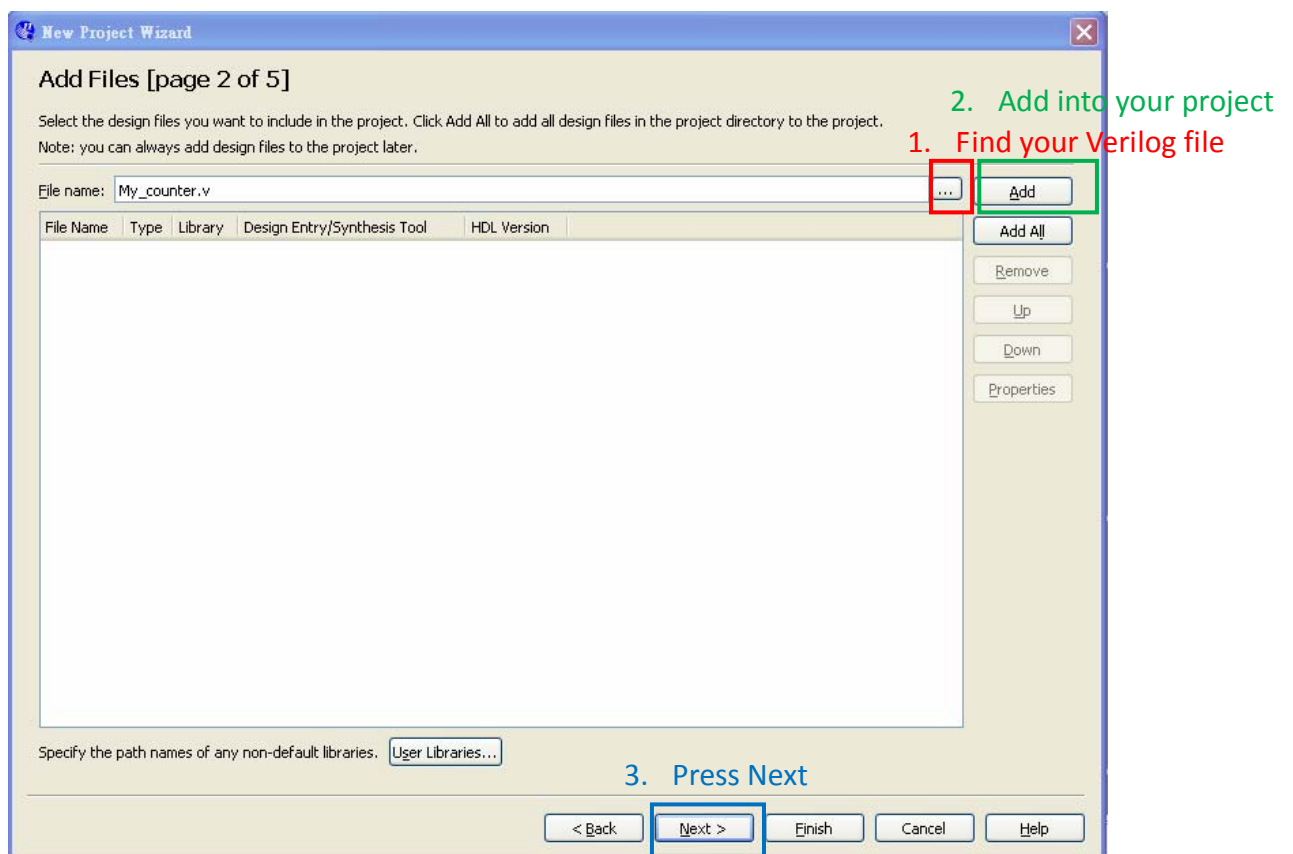
1. Open “Quartus II 10.1 Web Edition (32-Bit)”
2. File->New project wizard



3. The name of top module must be the **same** as your verilog code!



4.



5. Select the FPGA you are going to use

In this lab, choose "Family: Cyclone II", and for DE2-70 choose "EP2C70F896C6"

New Project Wizard

Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation.

Device family

Family: **Cyclone II**

Devices: All

Show in 'Available devices' list

Package: Any

Pin count: Any

Speed grade: Any

☒ Show advanced devices

☐ HardCopy compatible only

Target device

☐ Auto device selected by the Fitter

☒ Specific device selected in 'Available devices' list

☐ Other: n/a

Available devices:

Name	Core Voltage	LEs	User I/Os	Memory Bits	Embedded multiplier 9-bit elements	PLL
EP2C70F672C0	1.2V	68416	422	1152000	300	4
EP2C70F672C7	1.2V	68416	422	1152000	300	4
EP2C70F672C8	1.2V	68416	422	1152000	300	4
EP2C70F672C9	1.2V	68416	422	1152000	300	4
EP2C70F896C6	1.2V	68416	622	1152000	300	4
EP2C70F896C7	1.2V	68416	622	1152000	300	4
EP2C70F896C8	1.2V	68416	622	1152000	300	4
EP2C70F896I8	1.2V	68416	622	1152000	300	4

Companion device

HardCopy:

☐ Limit DSP & RAM to HardCopy device resources

< Back

Next >

Finish

Cancel

Help

New Project Wizard

EDA Tool Settings [page 4 of 5]

Specify the other EDA tools used with the Quartus II software to develop your project.

EDA tools:

Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entry/Synthesis	<None>	<None>	☐ Run this tool automatically to synthesize the current design
Simulation	<None>	<None>	☐ Run gate-level simulation automatically after compilation
Timing Analysis	<None>	<None>	☐ Run this tool automatically after compilation
Formal Verification	<None>	<None>	
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	
	Boundary Scan	<None>	

< Back

Next >

Finish

Cancel

Help

New Project Wizard

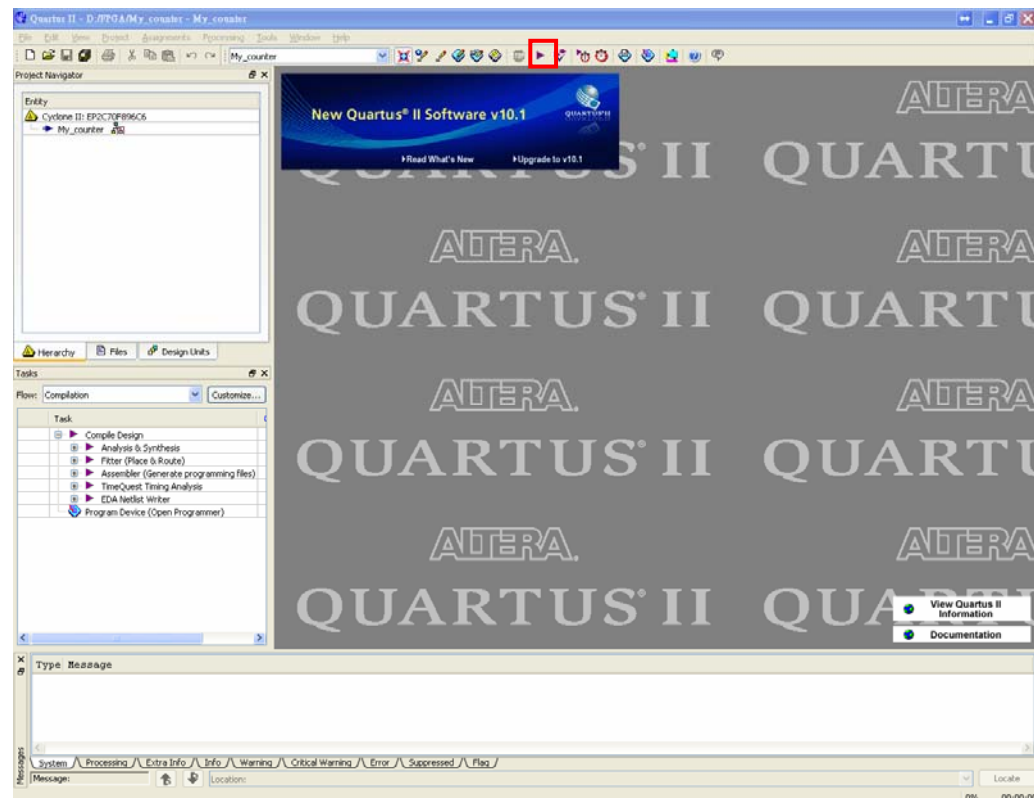
Summary [page 5 of 5]

When you click Finish, the project will be created with the following settings:

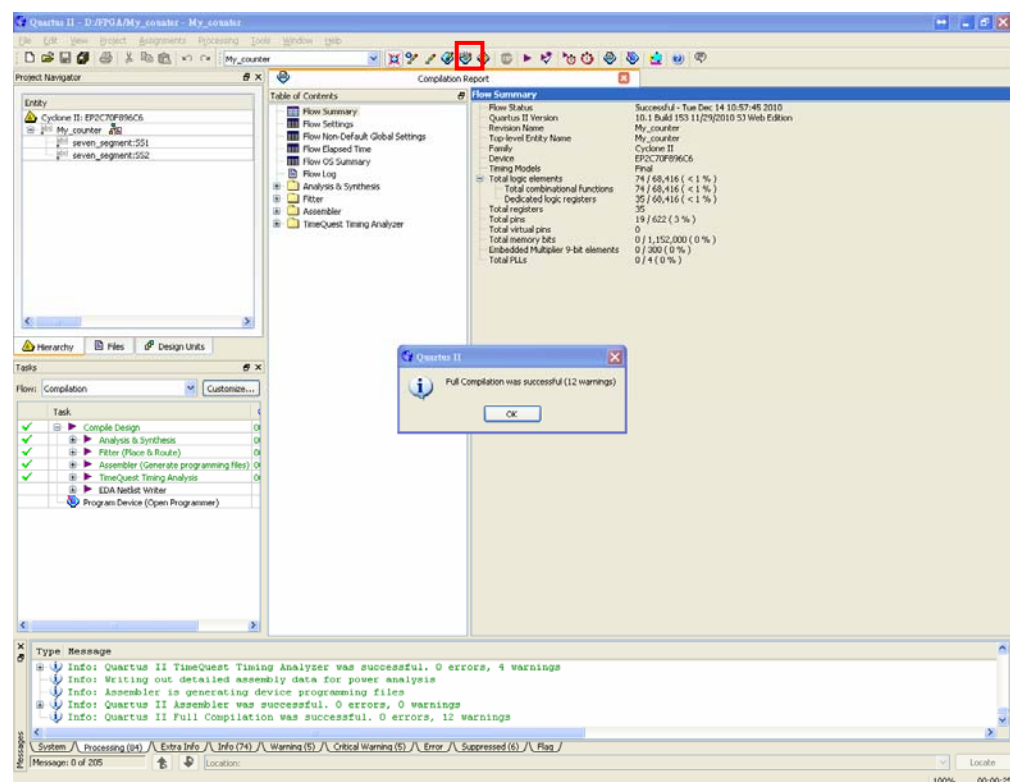
Project directory:	D:\FPGA
Project name:	My_counter
Top-level design entity:	My_counter
Number of files added:	1
Number of user libraries added:	0
Device assignments:	
Family name:	Cyclone II
Device:	EP2C70F896C6
EDA tools:	
Design entry/synthesis:	<None> (<None>)
Simulation:	<None> (<None>)
Timing analysis:	<None> (<None>)
Operating conditions:	
Core voltage:	1.2V
Junction temperature range:	0-85 °C

< Back Next > **Finish** Cancel Help

6. Press the start compilation (Ctrl+L)



7. Use "Pin Planner" to plan the input and output in your FPGA. In other words, connect your verilog code and FPGA by setting the location of each I/O according to the user manual of FPGA.



Pin Planner - D:/FPGA/My_counter - My_counter

Top View - Wire Bond
Cyclone II - EP2C70F696C6

Groups

Named: *

Node Name	Direction	Location
out1[7..0]	Output Group	
out2[7..0]	Output Group	
<new group>		

Plan the input and output in your FPGA

Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved
clk	Input				3.3-V LV...default	
out1[7]	Output				3.3-V LV...default	
out1[6]	Output				3.3-V LV...default	
out1[5]	Output				3.3-V LV...default	
out1[4]	Output				3.3-V LV...default	
out1[3]	Output				3.3-V LV...default	
out1[2]	Output				3.3-V LV...default	
out1[1]	Output				3.3-V LV...default	
out1[0]	Output				3.3-V LV...default	
out2[7]	Output				3.3-V LV...default	
out2[6]	Output				3.3-V LV...default	
out2[5]	Output				3.3-V LV...default	
out2[4]	Output				3.3-V LV...default	
out2[3]	Output				3.3-V LV...default	
out2[2]	Output				3.3-V LV...default	
out2[1]	Output				3.3-V LV...default	
out2[0]	Output				3.3-V LV...default	
pause	Input				3.3-V LV...default	
rst	Input				3.3-V LV...default	
<new node>						

Filter: Pins: all

0% 00:00:00

	DE2-70
Clk	PIN_D16
out1[7]	PIN_AE8
out1[6]	PIN_AF9
out1[5]	PIN_AH9
out1[4]	PIN_AD10
out1[3]	PIN_AF10
out1[2]	PIN_AD11
out1[1]	PIN_AD12
out1[0]	PIN_AF12
out2[7]	PIN_AG13
out2[6]	PIN_AE16
out2[5]	PIN_AF16
out2[4]	PIN_AG16
out2[3]	PIN_AE17
out2[2]	PIN_AF17
out2[1]	PIN_AD17
out2[0]	PIN_AC17
pause	PIN_AB26
rst	PIN_AA23

Example for DE2-70:

Top View - Wire Bond
Cyclone II - EP2C70F696C6

Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved
clk	Input	PIN_D16	4	B4_N0	3.3-V LV..default	
out1[7..0]	Output Group					
out1[7]	Output	PIN_AE8	8	B8_N0	3.3-V LV..default	
out1[6]	Output	PIN_AF9	8	B8_N2	3.3-V LV..default	
out1[5]	Output	PIN_AH9	8	B8_N1	3.3-V LV..default	
out1[4]	Output	PIN_AD10	8	B8_N2	3.3-V LV..default	
out1[3]	Output	PIN_AF10	8	B8_N2	3.3-V LV..default	
out1[2]	Output	PIN_AD11	8	B8_N2	3.3-V LV..default	
out1[1]	Output	PIN_AD12	8	B8_N1	3.3-V LV..default	
out1[0]	Output	PIN_AF12	8	B8_N1	3.3-V LV..default	
out2[7..0]	Output Group					
out2[7]	Output	PIN_AG13	8	B8_N0	3.3-V LV..default	
out2[6]	Output	PIN_AE16	7	B7_N3	3.3-V LV..default	
out2[5]	Output	PIN_AF16	7	B7_N3	3.3-V LV..default	
out2[4]	Output	PIN_AG16	7	B7_N3	3.3-V LV..default	
out2[3]	Output	PIN_AE17	7	B7_N3	3.3-V LV..default	
out2[2]	Output	PIN_AF17	7	B7_N2	3.3-V LV..default	
out2[1]	Output	PIN_AD17	7	B7_N2	3.3-V LV..default	
out2[0]	Output	PIN_AC17	7	B7_N2	3.3-V LV..default	
pause	Input	PIN_AB26	6	B6_N2	3.3-V LV..default	
rst	Input	PIN_AA23	6	B6_N2	3.3-V LV..default	

8. After pin planner, another compilation is required!

Compilation Report

Flow Summary

Flow Status	Successful - Tue Dec 14 10:57:45 2010
Quartus II Version	10.1 Build 153 11/29/2010 53 Web Edition
Revision Name	My_counter
Top-level Entity Name	My_counter
Family	Cyclone II
Device	EP2C70F696C6
Timing Models	Final
Total logic elements	74 / 68,416 (< 1 %)
Total combinational functions	74 / 68,416 (< 1 %)
Dedicated logic registers	35 / 68,416 (< 1 %)
Total registers	35
Total pins	19 / 622 (3 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Messages

Type: Message

- Info: Quartus II TimeQuest Timing Analyzer was successful. 0 errors, 4 warnings
- Info: Writing out detailed assembly data for power analysis
- Info: Assembler is generating device programming files
- Info: Quartus II Assembler was successful. 0 errors, 0 warnings
- Info: Quartus II Full Compilation was successful. 0 errors, 12 warnings

9. Next, use "Programmer" from "tool → programmer"

The image shows two screenshots of the Quartus II and Programmer software interface.

Top Screenshot: Quartus II - D:/FPGA/My_counter - My_counter

The main window displays the "Flow Summary" tab, which shows the compilation status as "Successful - Tue Dec 14 11:16:41 2010". The "Table of Contents" on the left lists various design steps, including "Compile Design", "Analysis & Synthesis", "Filter (Place & Route)", "Assembler (Generate programming files)", "TimeQuest Timing Analysis", and "EDA Netlist Writer". The "Messages" window at the bottom shows the following information:

- Info: Quartus II TimeQuest Timing Analyzer was successful. 0 errors, 4 warnings
- Info: Writing out detailed assembly data for power analysis
- Info: Assembler is generating device programming files
- Info: Quartus II Assembler was successful. 0 errors, 0 warnings
- Info: Quartus II Full Compilation was successful. 0 errors, 11 warnings

Bottom Screenshot: Programmer - D:/FPGA/My_counter - My_counter - [My_counter.edi]

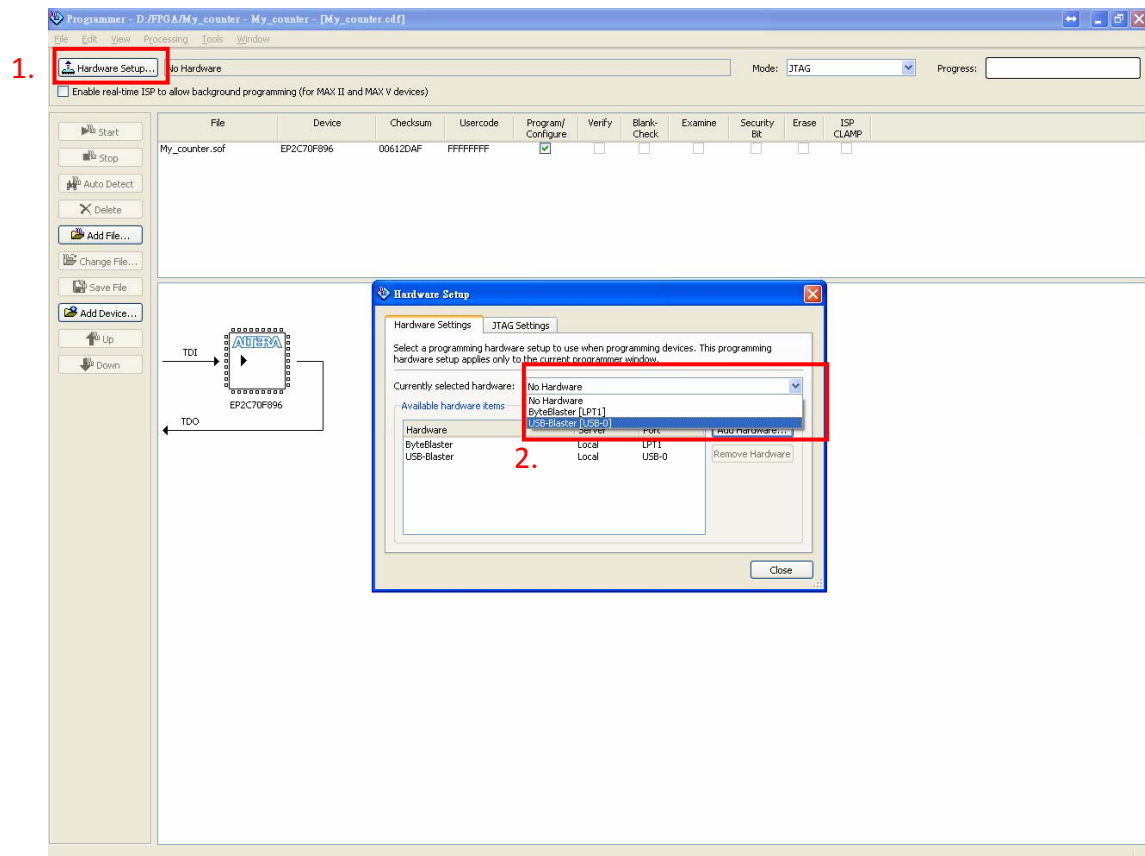
The Programmer window shows the hardware setup for the device. The "File" column lists "My_counter.sof". The "Device" column shows "EP2C70F896". The "Checksum" column shows "00612DAF". The "Usercode" column shows "FFFFFFF". The "Program/Configure" checkbox is checked. The "Verify" checkbox is unchecked. The "Blank-Check" checkbox is unchecked. The "Examine" checkbox is unchecked. The "Security Bit" checkbox is unchecked. The "Erase" checkbox is unchecked. The "ISP CLAMP" checkbox is unchecked.

The "Hardware Setup" section shows "No Hardware" selected. The "Mode" is set to "JTAG". The "Progress" bar is at 100%.

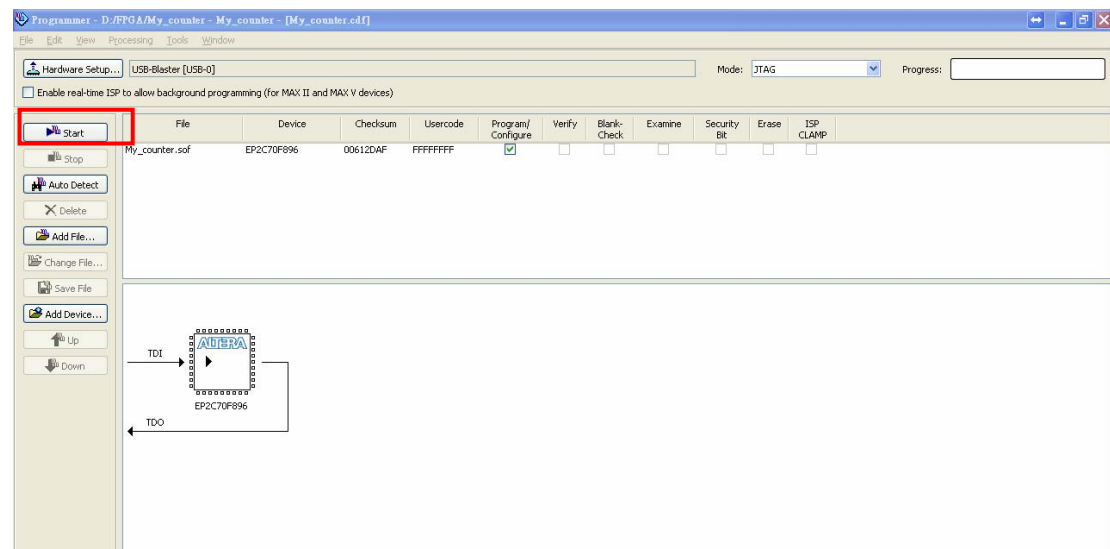
The "Start" button is highlighted. The "Stop" button is also visible. The "Auto Detect" button is visible. The "Delete" button is visible. The "Add File..." button is visible. The "Change File..." button is visible. The "Save File" button is visible. The "Add Device..." button is visible. The "Up" button is visible. The "Down" button is visible.

The "Start" button is highlighted. The "Stop" button is also visible. The "Auto Detect" button is visible. The "Delete" button is visible. The "Add File..." button is visible. The "Change File..." button is visible. The "Save File" button is visible. The "Add Device..." button is visible. The "Up" button is visible. The "Down" button is visible.

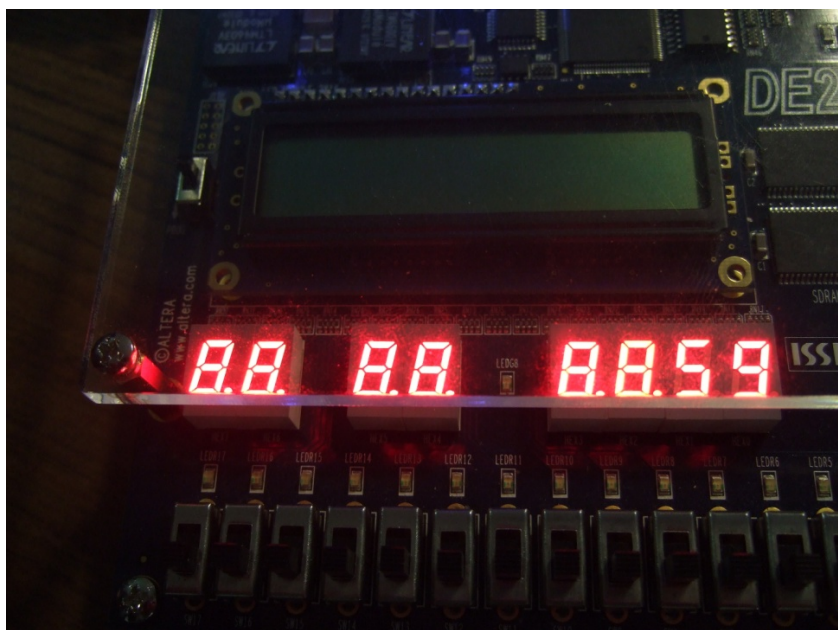
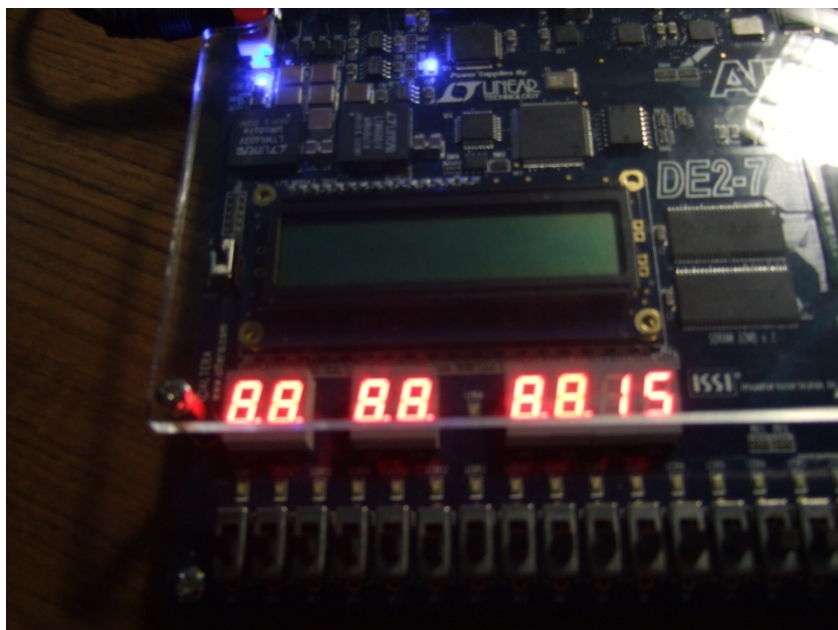
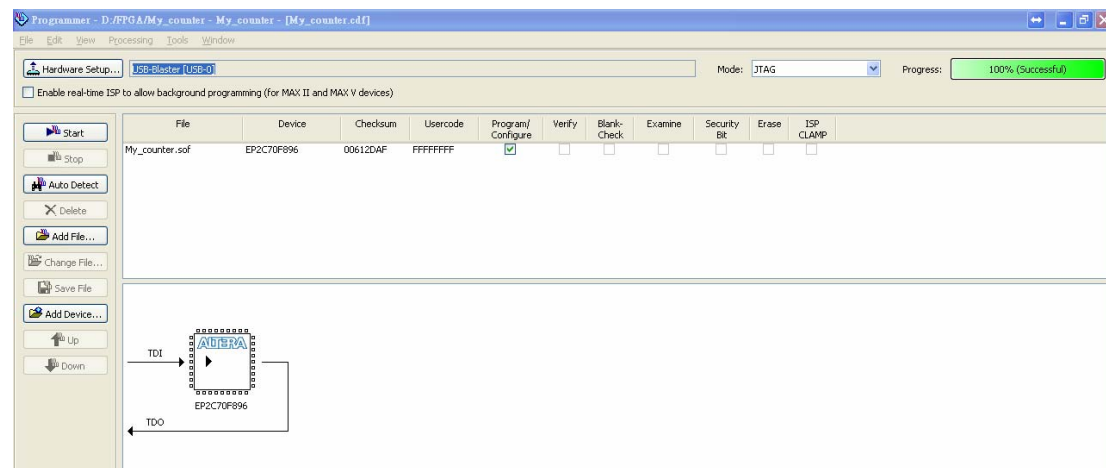
10. You must first connect your FPGA and choose “Hardware setup -> USB-Blaster”.



11. Press Start and FPGA will start to work!



12. Counter is counting ! (SW0-> reset, SW1-> pause)



Exercises

Add one output port which lights the LEDR0 when the counter is counting and turns off the LEDR0 when the counter is not counting.