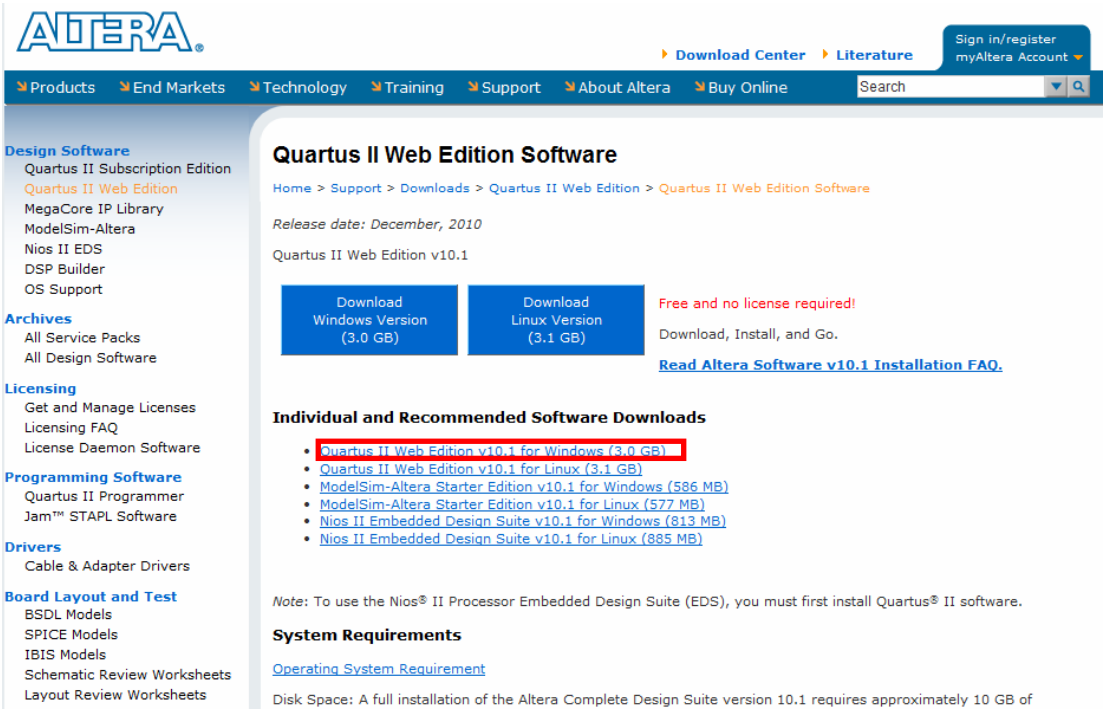
Computer-Aided VLSI System Design
FPGA Lab

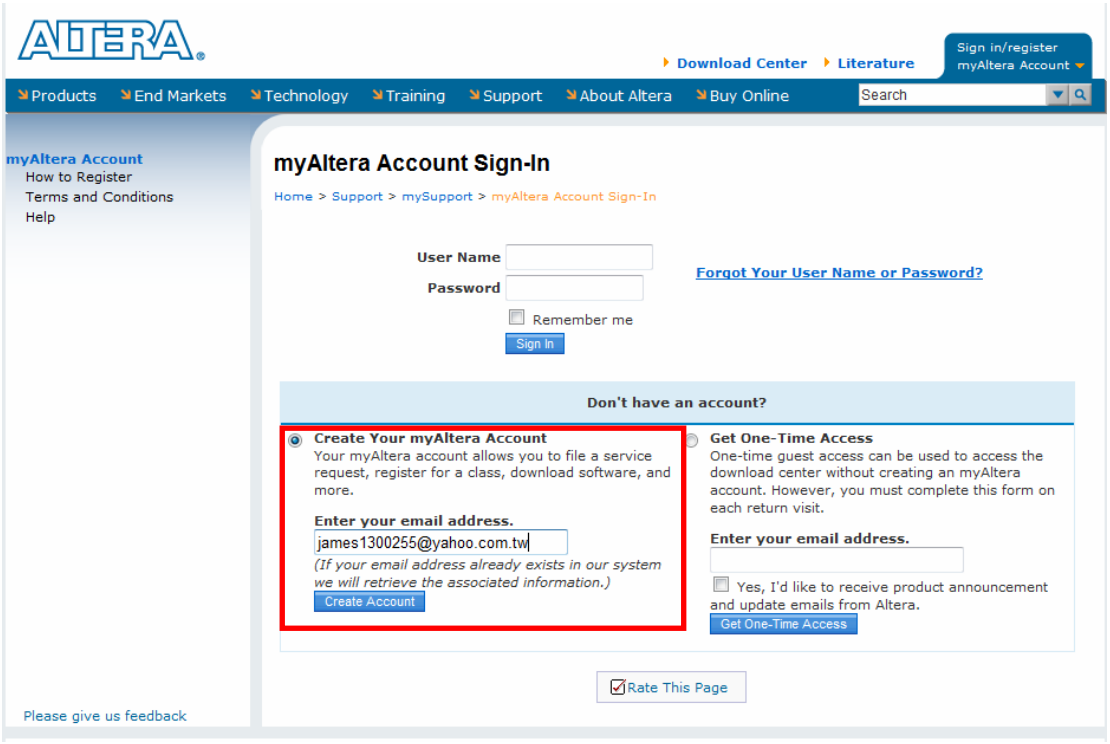
一、ALTERA Quartus II Web Edition Software 下載安裝過程
二、安裝 USB-Blaster Driver 讓電腦可以透過 USB 與 FPGA 溝通
三、實驗步驟

一、ALTERA Quartus II Web Edition Software 下載安裝過程

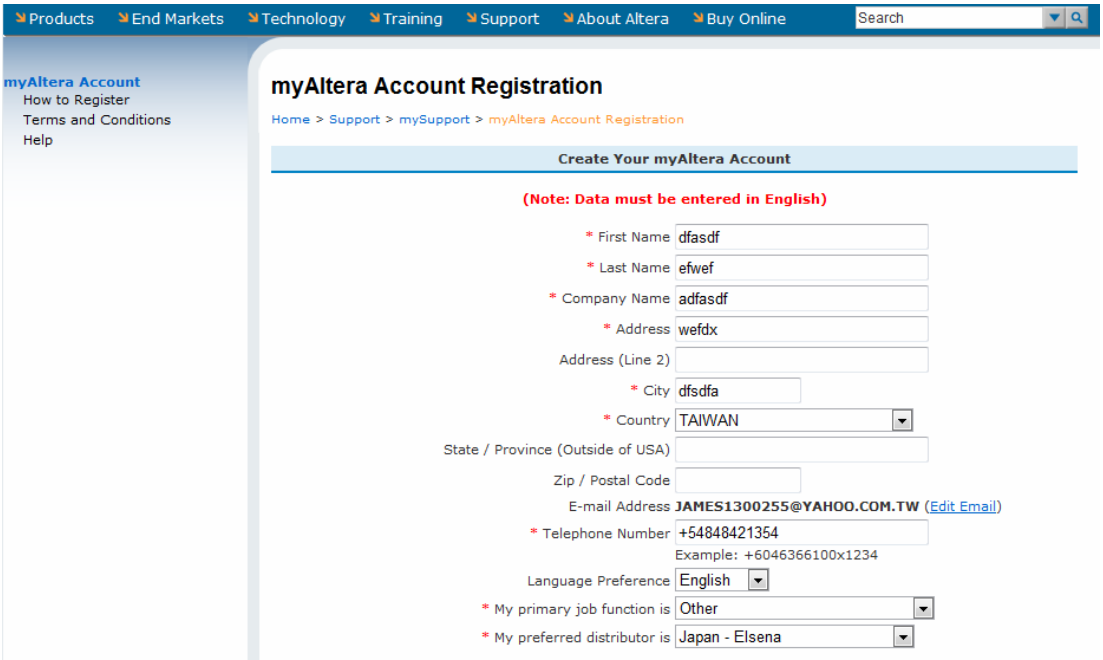
1. 打開 IE，進入 ALTERA Quartus II Web Edition Software 下載網址
https://www.altera.com/download/software/quartus-ii-we
點選 Quartus II Web Edition v10.1 for Windows (3.0 GB)軟體下載



2. 申請一個帳號，輸入 email address 後點選 Create Account



3. 填寫資料有「*」是必填的部分，其中 email address、帳號、密碼一定要設定正確。填完後按 Create Account



* **For what end applications do you design? (check all that apply)**

- [ ] Academic/Research
- [ ] Automotive
- [ ] Computing and Office Automation
- [ ] Consumer Electronics or Digital Entertainment
- [ ] Digital Broadcast
- [ ] Industrial
- [ ] Medical Equipment
- [ ] Military or Aerospace
- [ ] Semiconductors
- [ ] Storage Systems
- [ ] Test and Measurement Equipment
- [ ] Wireless Communications
- [ ] Wireline Communications
- [x] Other

* **Please check all topics that interest you:**

- [x] CPLDs
- [ ] Digital signal processing
- [ ] Embedded processors
- [ ] HardCopy ASICs
- [ ] High-density FPGAs
- [ ] Low-cost FPGAs

* **When was the last time you designed with an Altera® product?**

- ( ) I'm currently designing with Altera products
- ( ) More than 1 year ago
- (•) Never

- [ ] Yes, I'd like to receive product announcement and update emails from Altera.
- [ ] Yes, I'd like to receive the Inside Edge-Altera's Monthly eNewsletter.

* **Create User Name** twusatw0 (3-20 characters, no spaces)

* **Create Password** •••••• (Minimum 6 characters)

* **Confirm password** ••••••

* [x] I agree to the Terms of Service

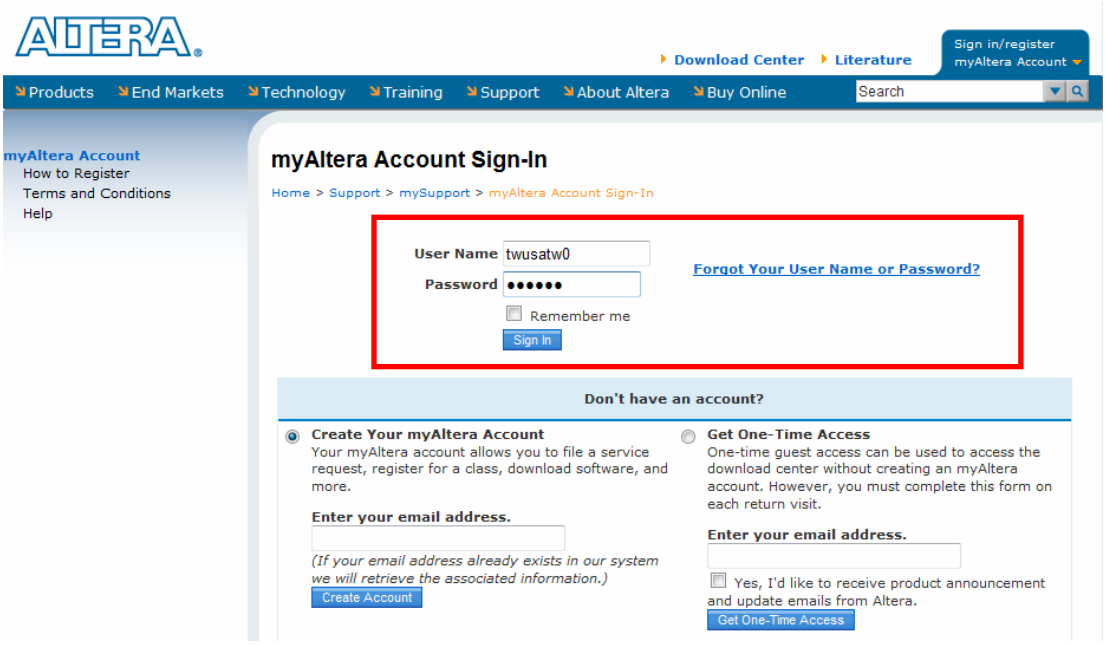
- [ ] Remember me

Create Account

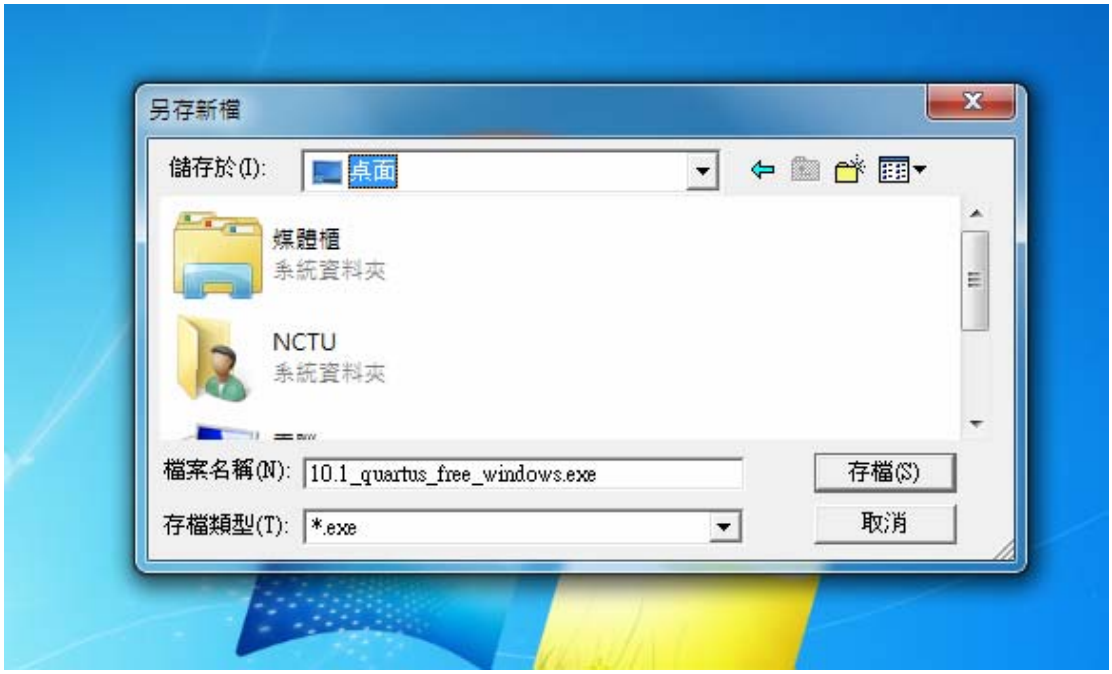
* Indicates required field.

4. 出現訊息告知系統有送出 email 到您信箱，按下 Continue 可開始下載檔案

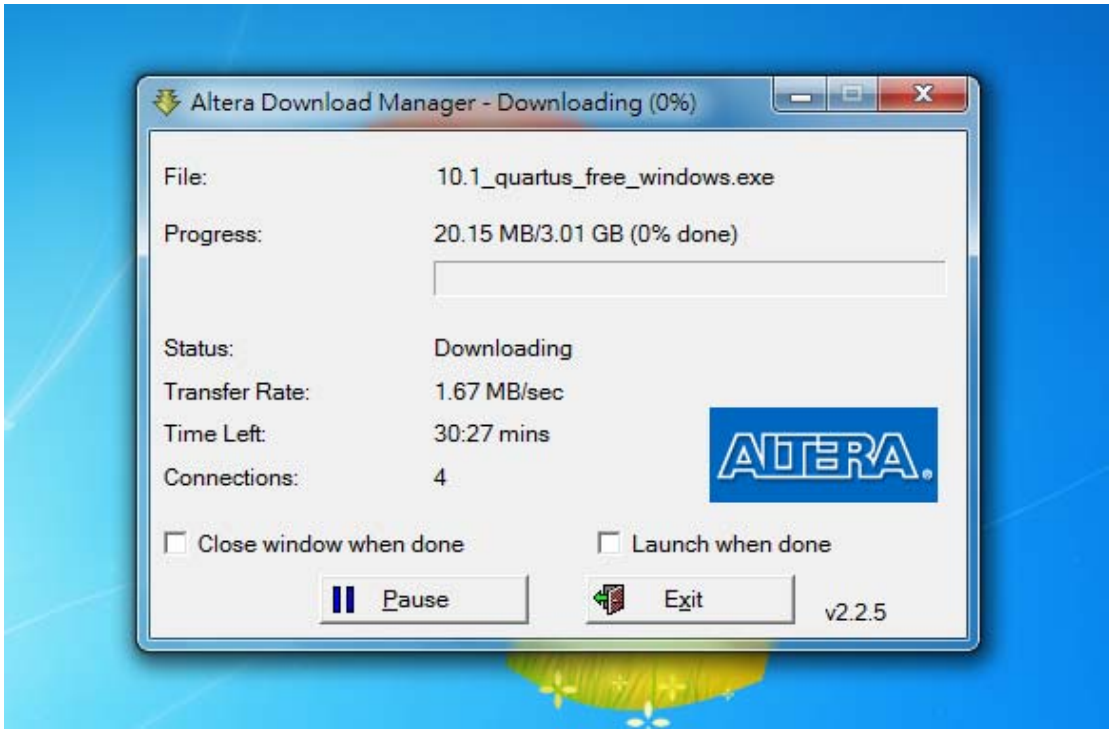
5. 如果之後想重新下載檔案，可以回到之前的申請帳號頁面，填入剛剛申請的帳號密碼後按下 Sign In 下載檔案



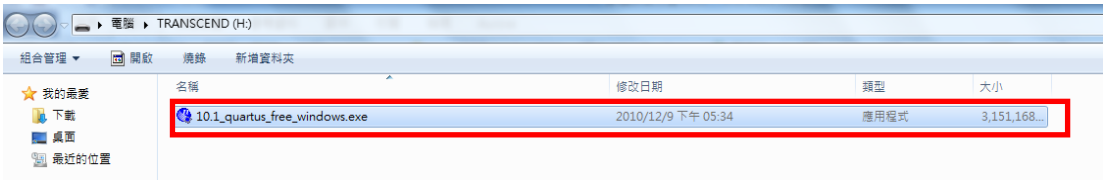
6. 剛剛按下 Sign In 後會詢問安裝檔要存在哪裡，選擇一個資料夾後按存檔



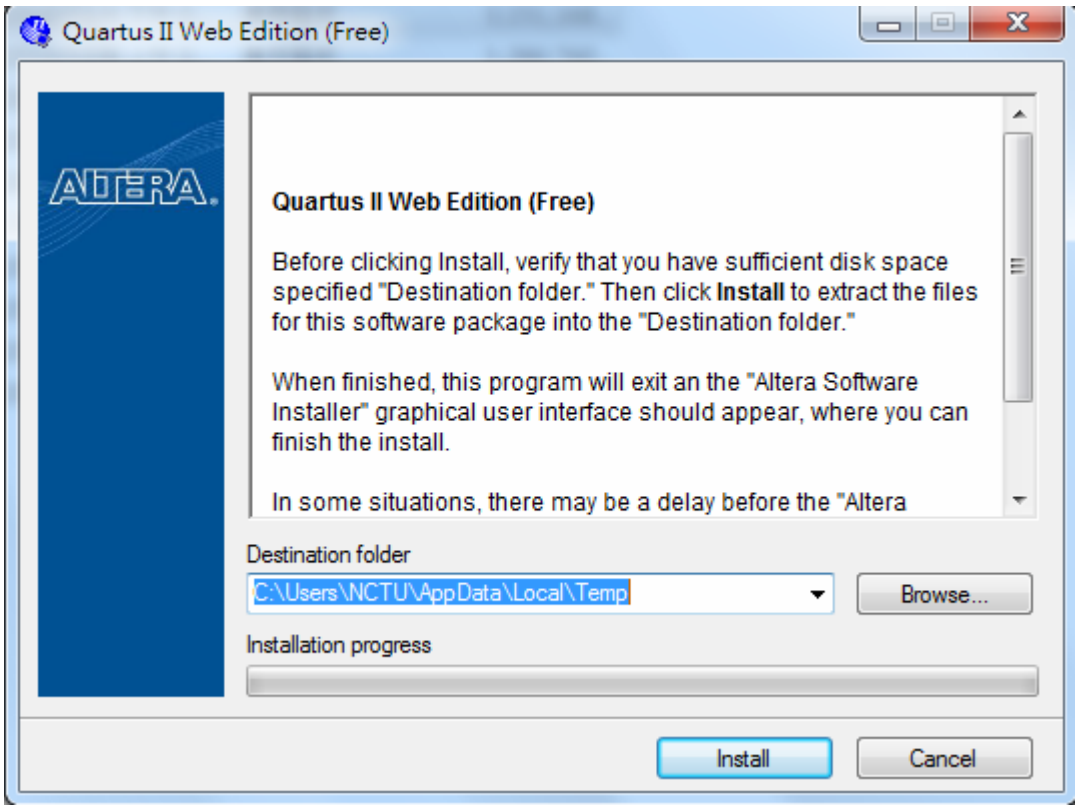
7. 按下存檔後會跳出下載畫面，等待一段時間直到下載結束



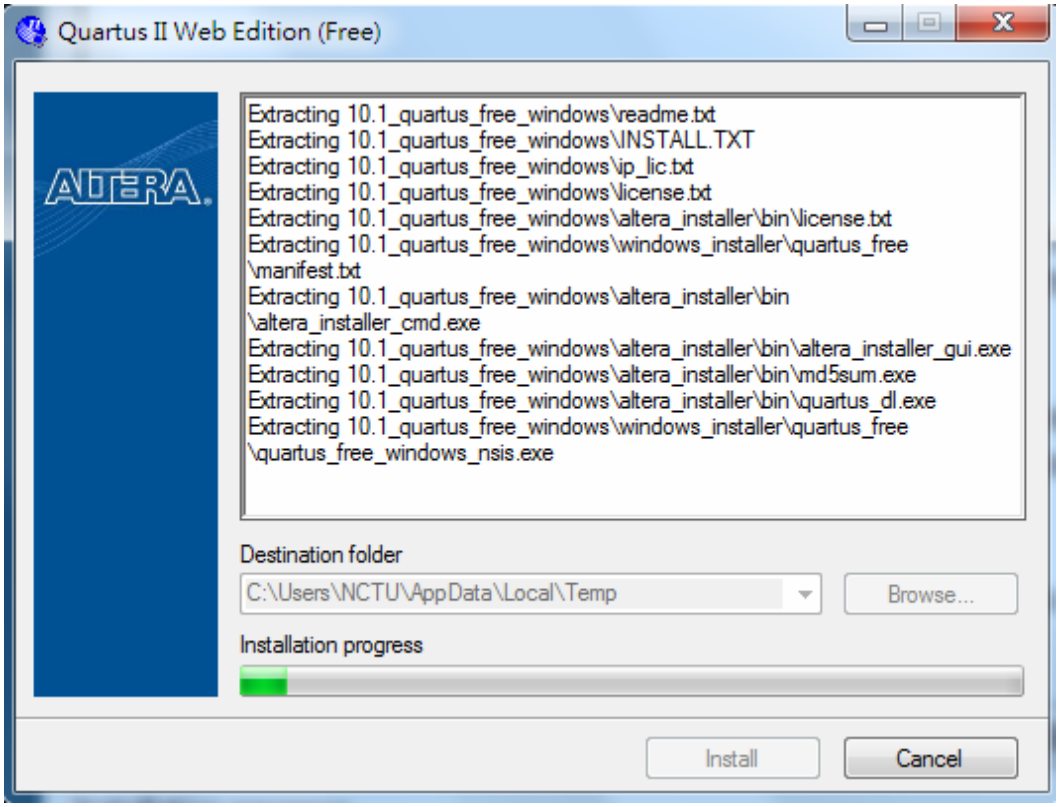
8. 點兩下執行檔進行安裝



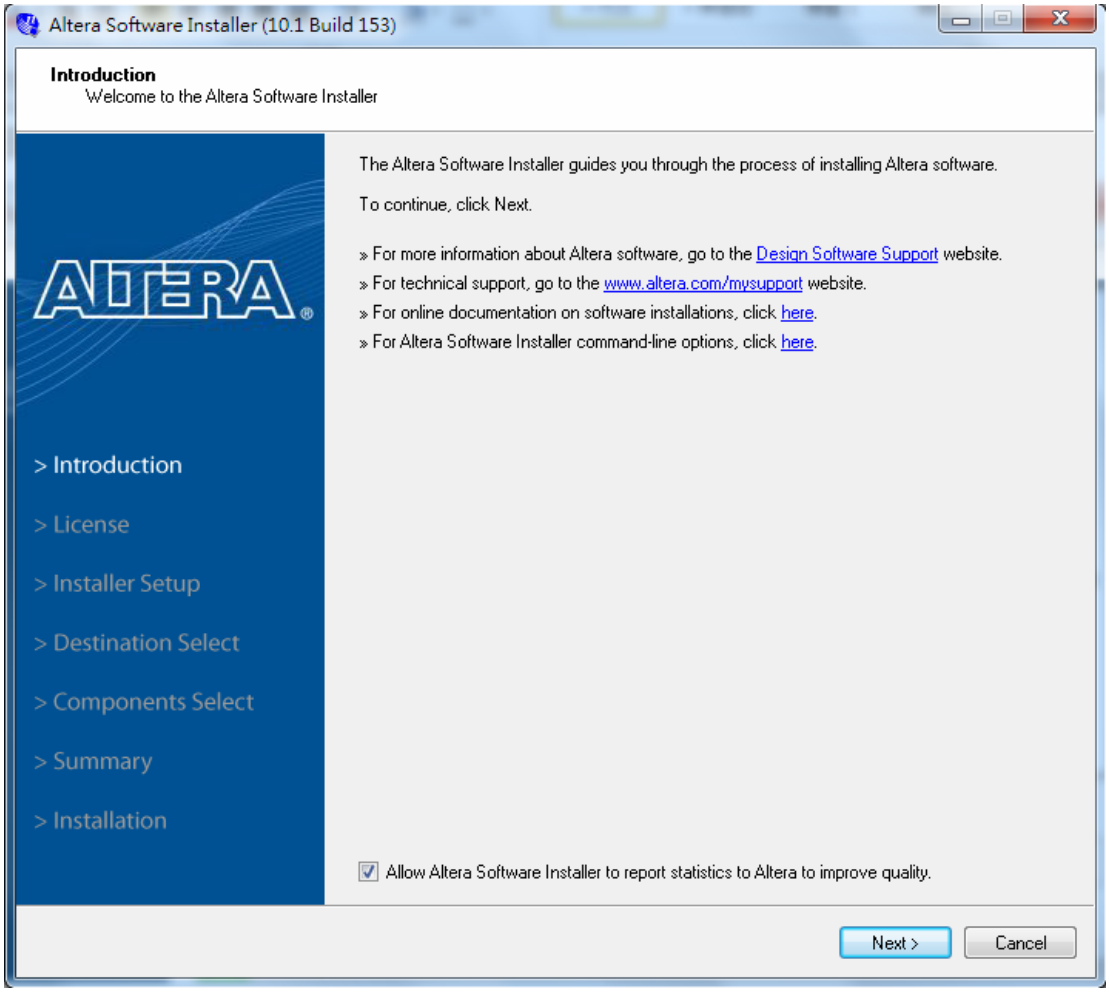
9. 出現第一個安裝畫面，點選 Install



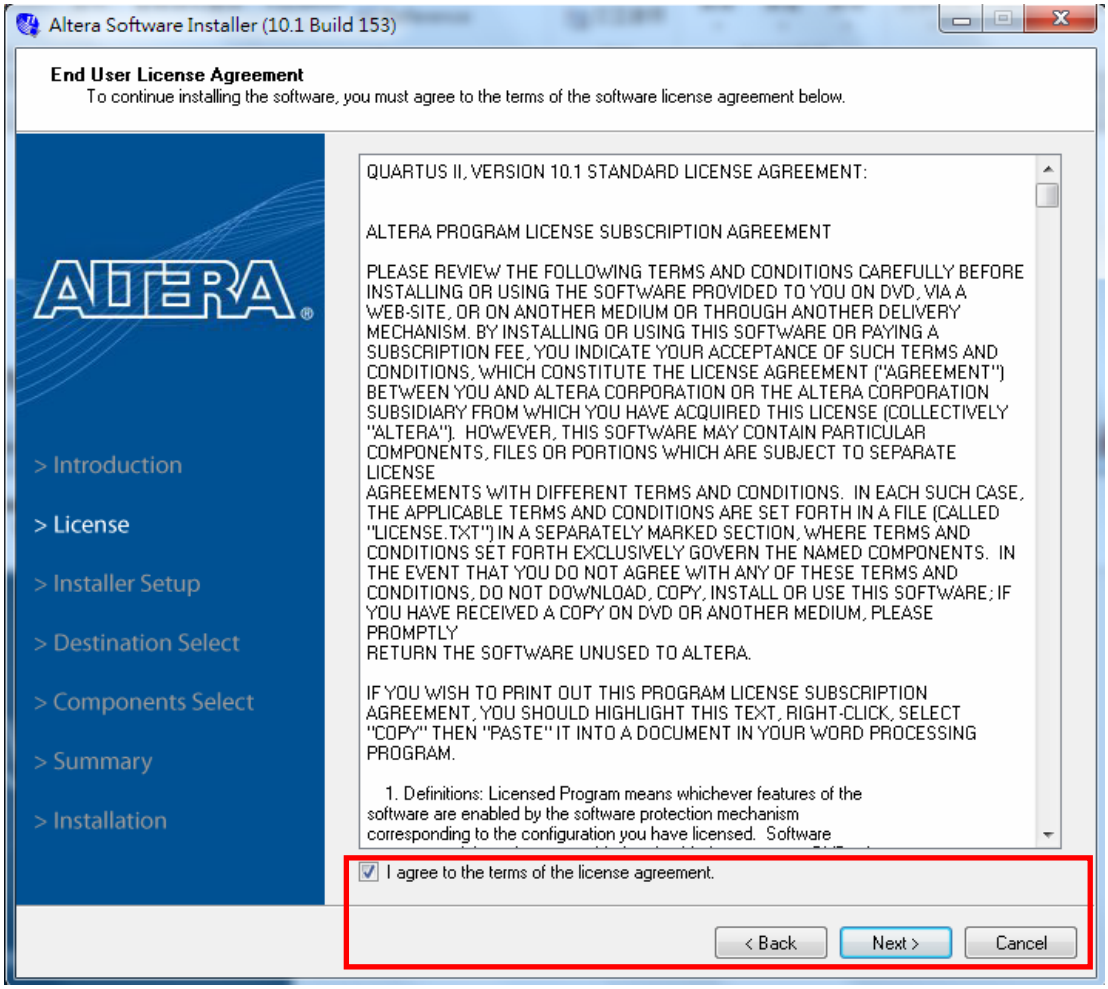
10. 出現 Extracting 的畫面


Quartus II Web Edition (Free)
ALTERA
Extracting 10.1_quartus_free_windows\readme.txt
Extracting 10.1_quartus_free_windows\INSTALL.TXT
Extracting 10.1_quartus_free_windows\ip_lic.txt
Extracting 10.1_quartus_free_windows\license.txt
Extracting 10.1_quartus_free_windows\altera_installer\bin\license.txt
Extracting 10.1_quartus_free_windows\windows_installer\quartus_free
\manifest.txt
Extracting 10.1_quartus_free_windows\altera_installer\bin
\altera_installer_cmd.exe
Extracting 10.1_quartus_free_windows\altera_installer\bin\altera_installer_gui.exe
Extracting 10.1_quartus_free_windows\altera_installer\bin\md5sum.exe
Extracting 10.1_quartus_free_windows\altera_installer\bin\quartus_dl.exe
Extracting 10.1_quartus_free_windows\windows_installer\quartus_free
\quartus_free_windows_nsis.exe
Destination folder
C:\Users\NCTU\AppData\Local\Temp
Browse...
Installation progress
Install
Cancel

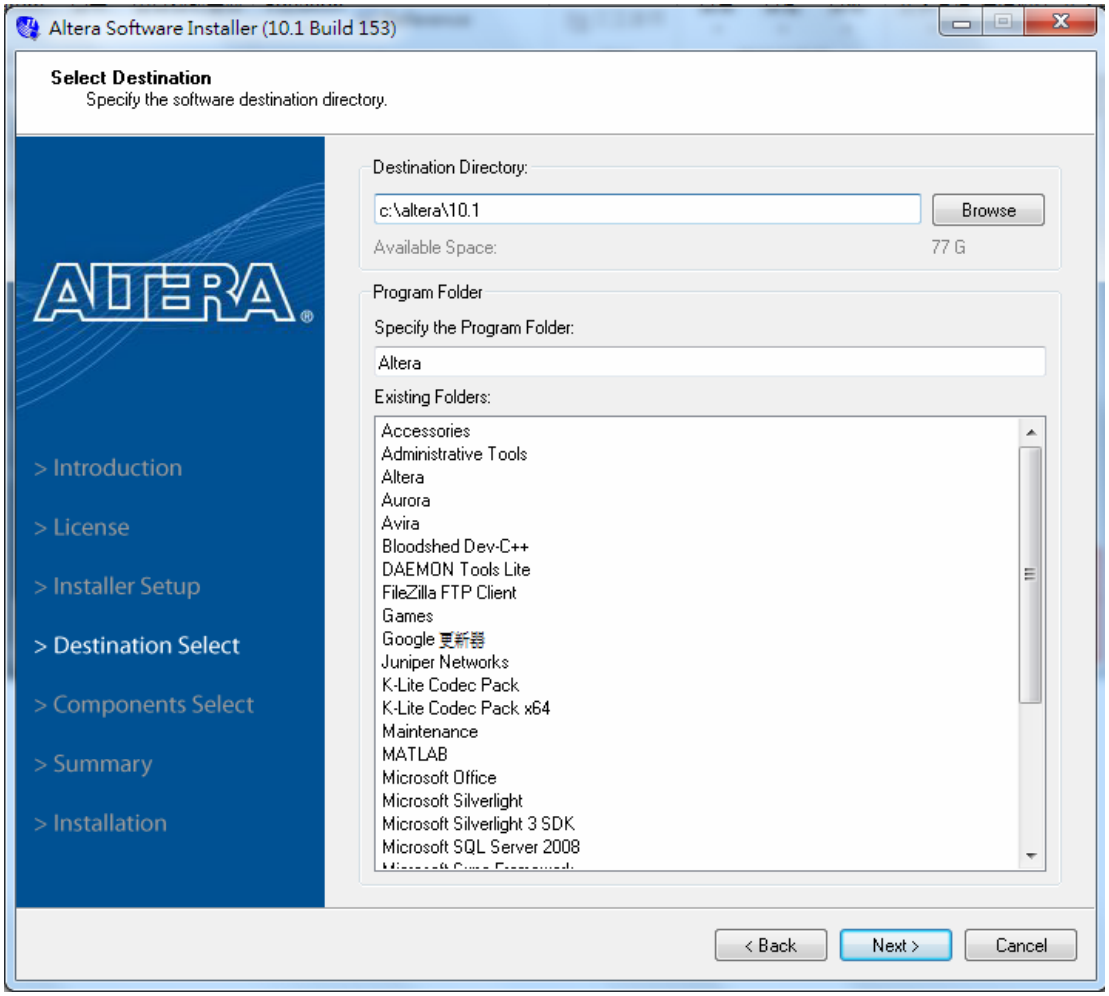
11. Extracting 完後，點選 Next 繼續安裝



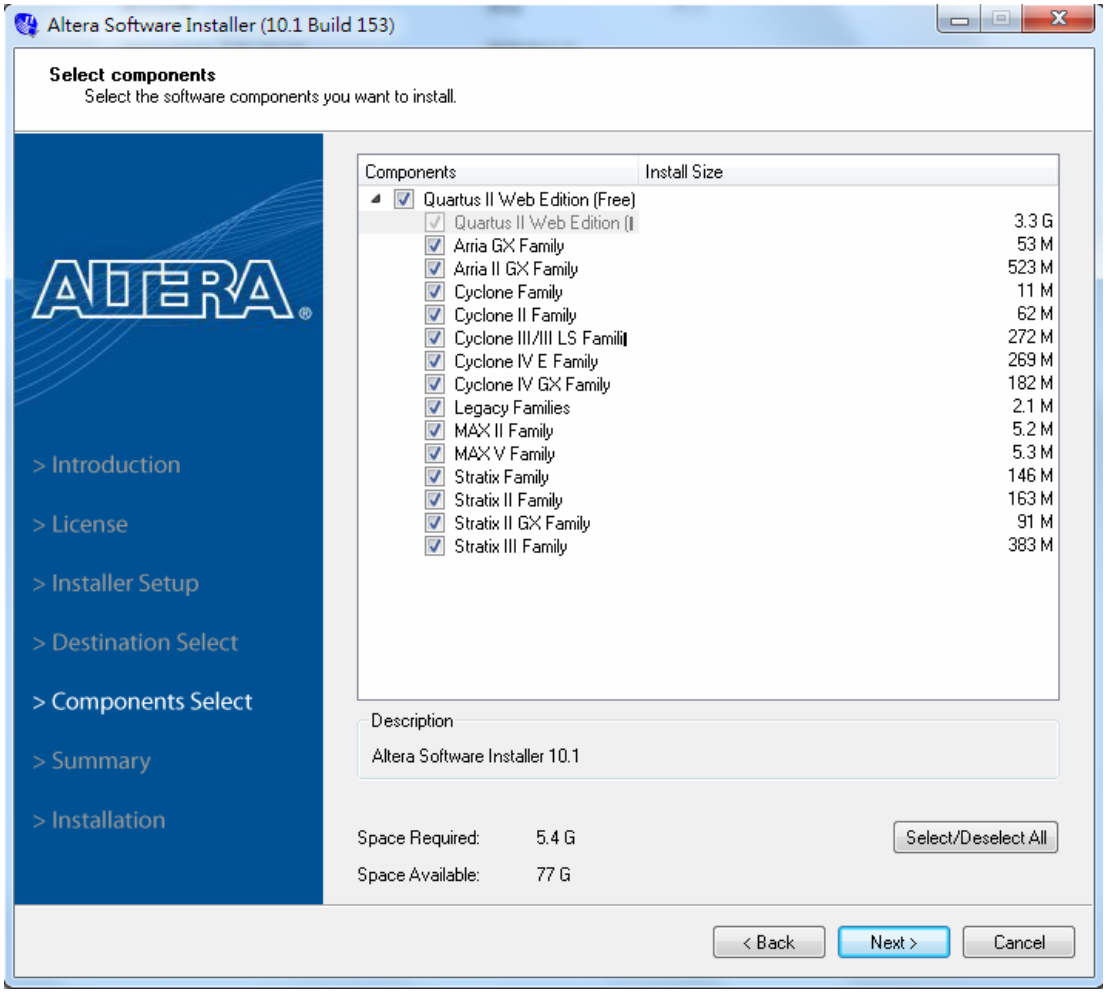
12. 勾選 I agree to the terms of the license agreement 並按下 Next 繼續安裝



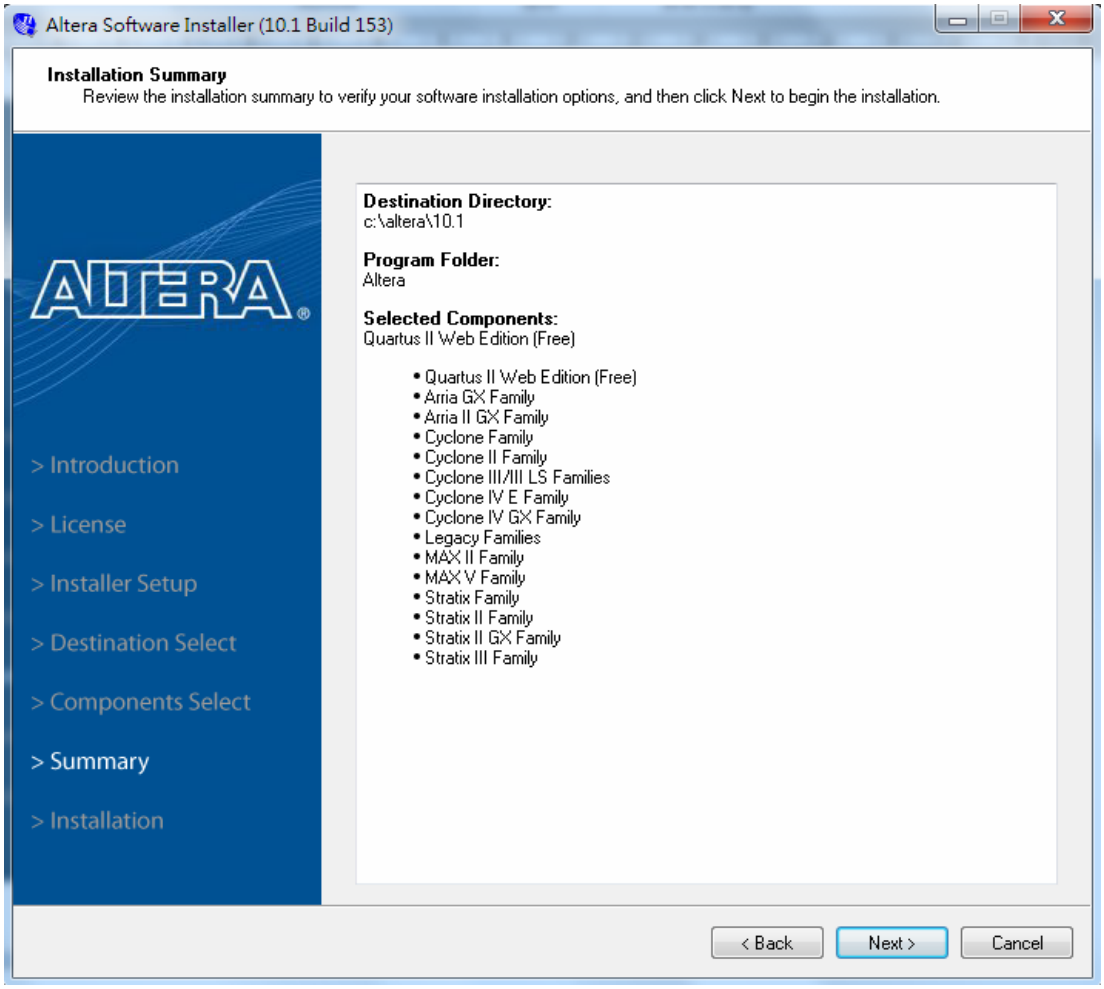
13. 按下 Next 繼續安裝



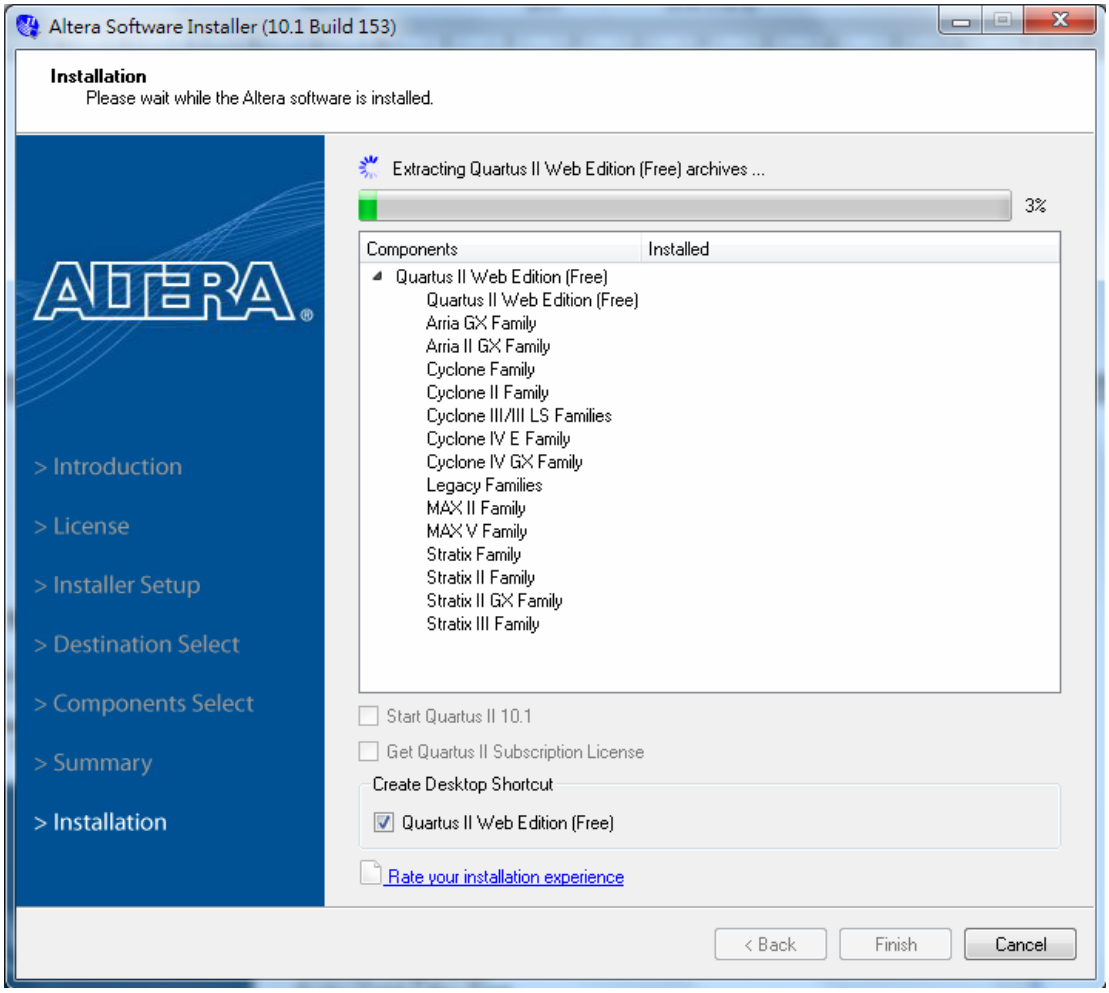
14. 按下 Next 後繼續安裝



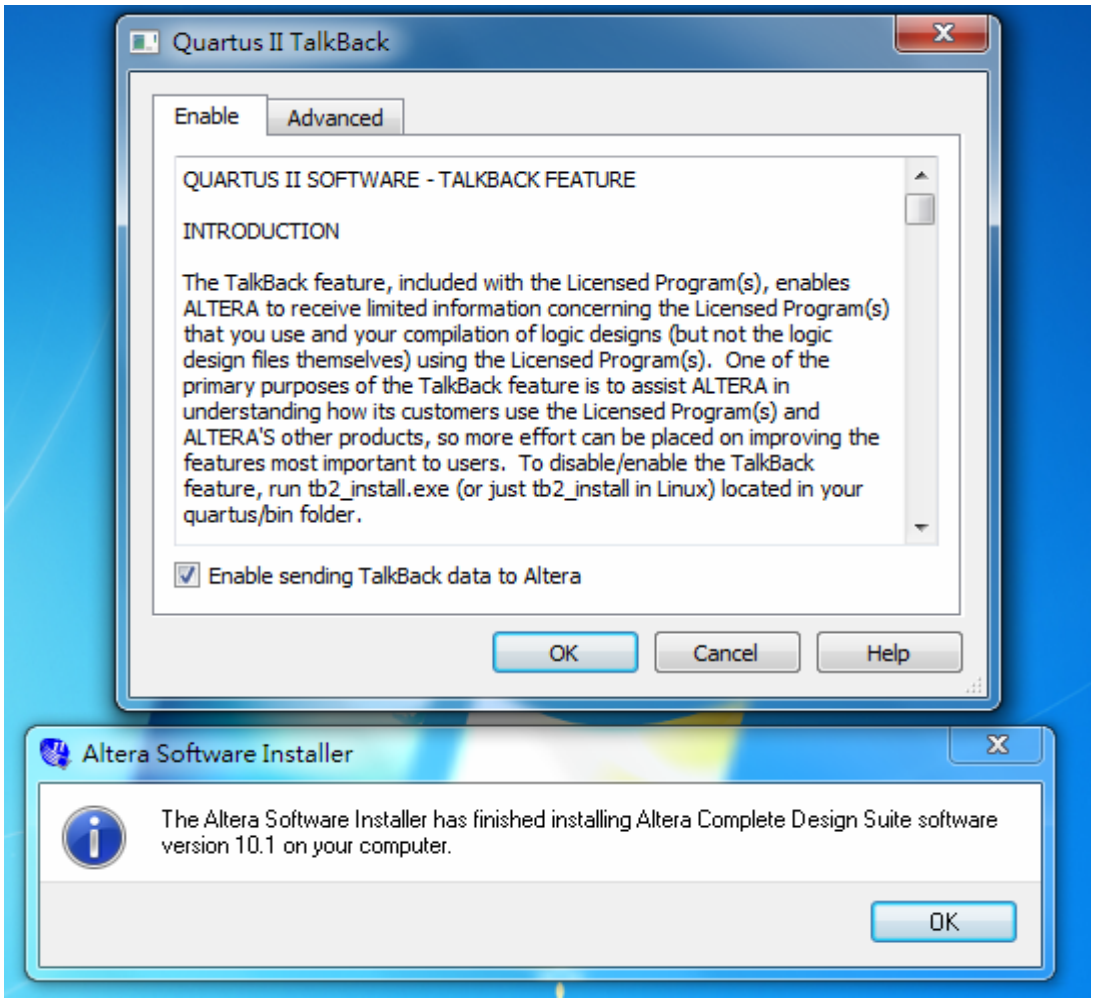
15. 按下 Next 後繼續安裝



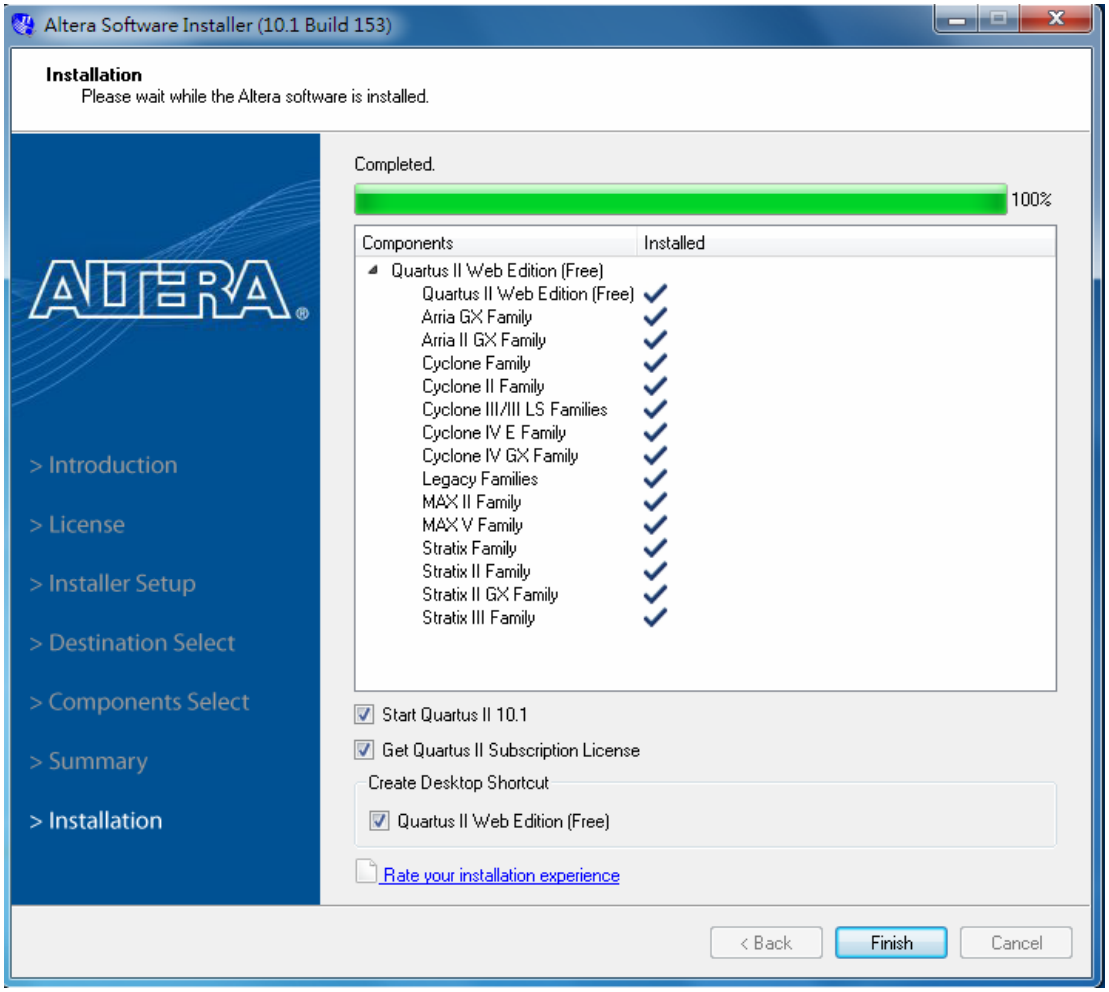
16. 出現安裝中的畫面


Altera Software Installer (10.1 Build 153)
Installation
Please wait while the Altera software is installed.
Extracting Quartus II Web Edition (Free) archives ...
3%
Components
Installed
Quartus II Web Edition (Free)
Quartus II Web Edition (Free)
Arria GX Family
Arria II GX Family
Cyclone Family
Cyclone II Family
Cyclone III/III LS Families
Cyclone IV E Family
Cyclone IV GX Family
Legacy Families
MAX II Family
MAX V Family
Stratix Family
Stratix II Family
Stratix II GX Family
Stratix III Family
> Introduction
> License
> Installer Setup
> Destination Select
> Components Select
> Summary
> Installation
Start Quartus II 10.1
Get Quartus II Subscription License
Create Desktop Shortcut
Quartus II Web Edition (Free)
Rate your installation experience
< Back
Finish
Cancel

17. 安裝中出現這兩個畫面，都點選 OK



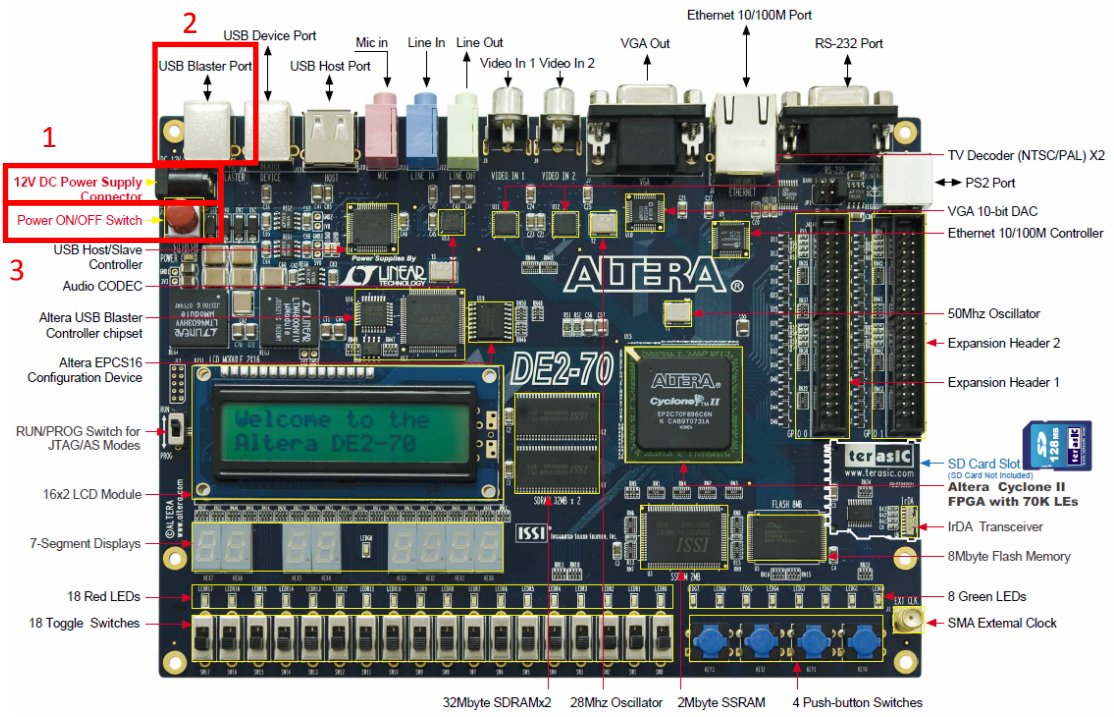
18. 按 Finish 結束安裝



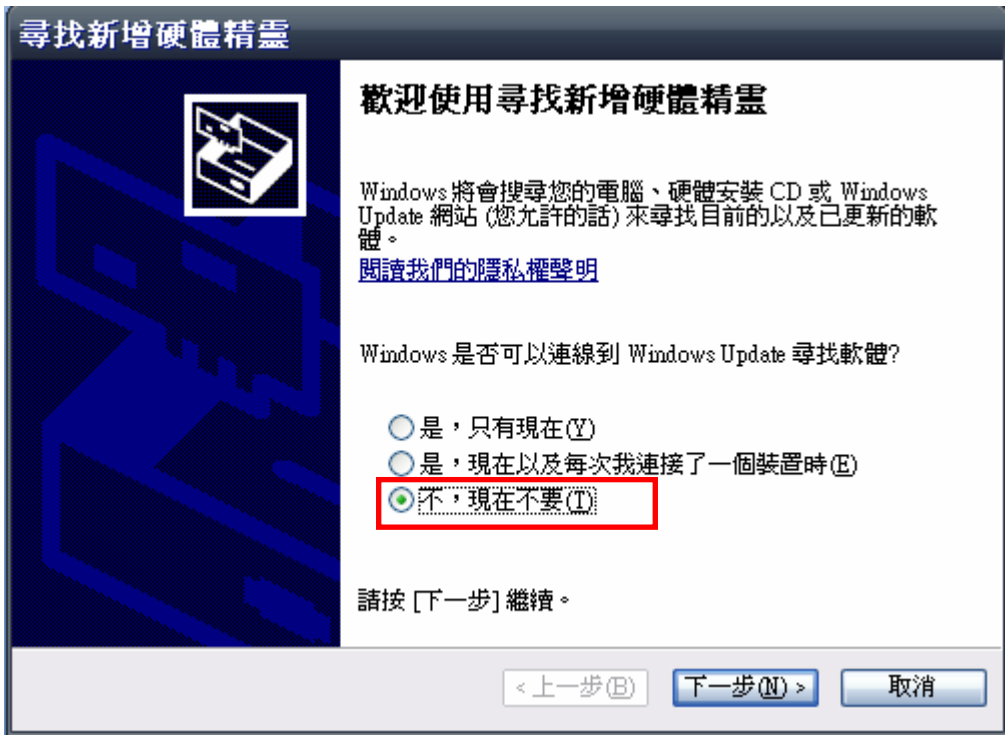
之後會自動開啓 Quartus II 軟體代表安裝成功！
(整個安裝過程約在半小時內結束)

二、安裝 USB-Blaster Driver 讓電腦可以透過 USB 與 FPGA 溝通

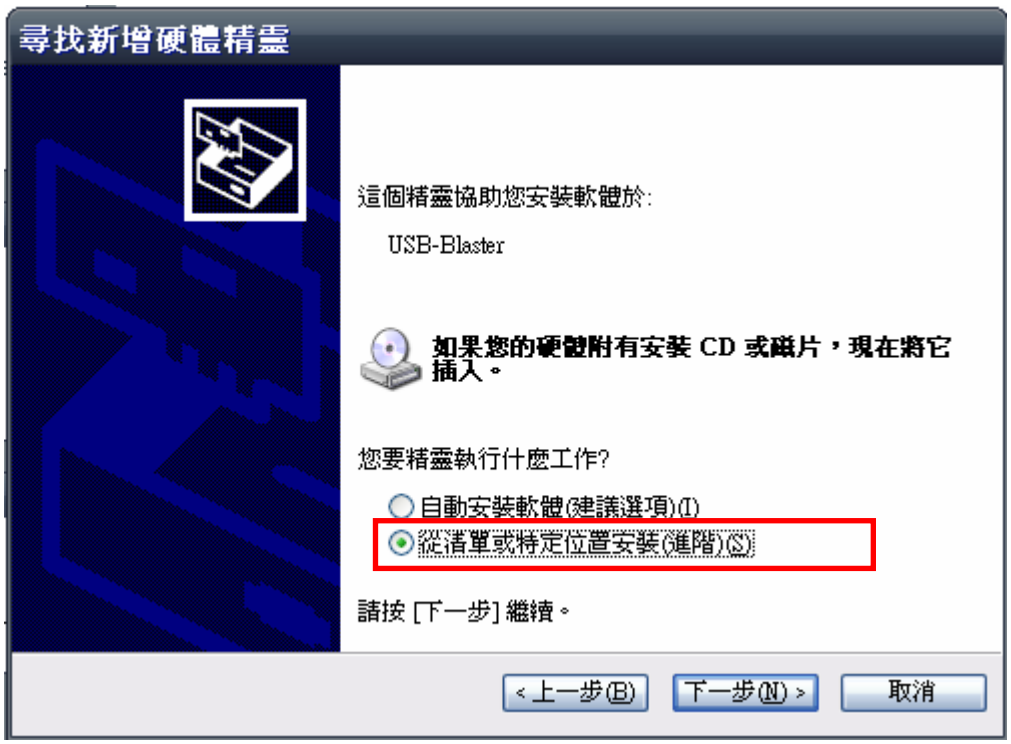
1. 接上電源線(1)與 USB(2)



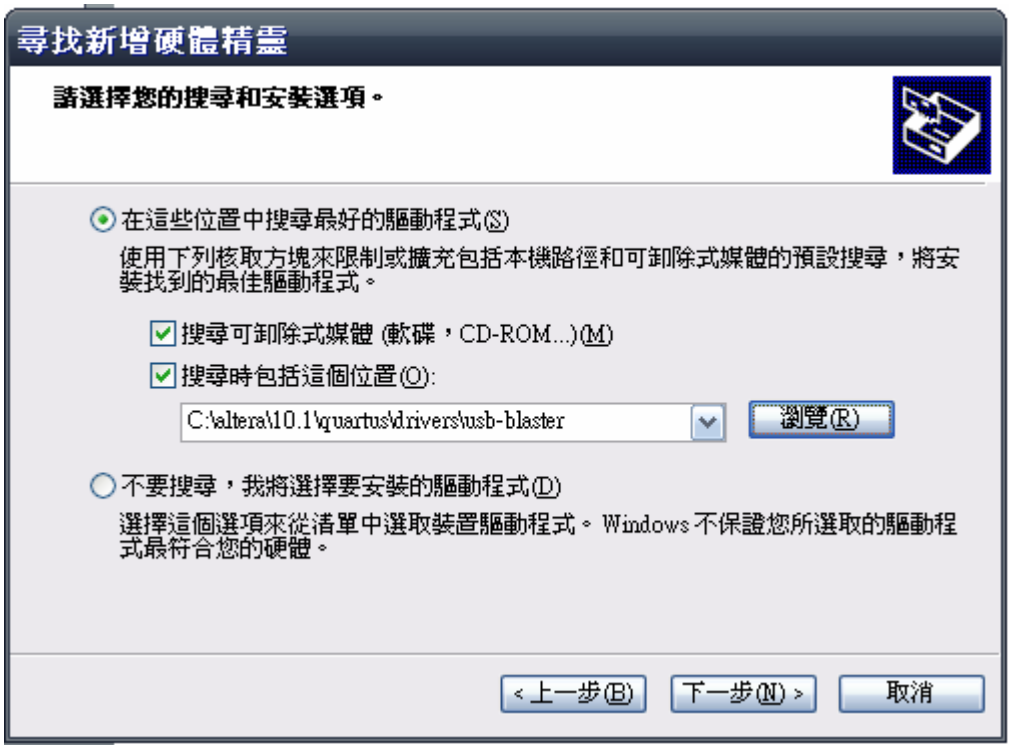
2. 打開 FPGA 的電源(3)後，將與 FPGA 相連的 USB 線插入電腦中，會出現找到新硬體的畫面，選擇「不，現在不要」後按下「下一步」



3. 選擇「從清單或特定位置安裝」後按下「下一步」



4. 根據以下畫面進行設定，並透過「瀏覽」設定 driver 所在的資料夾爲 C:\altera\10.1\quartus\drivers\usb-blaster 最後按下「下一步」

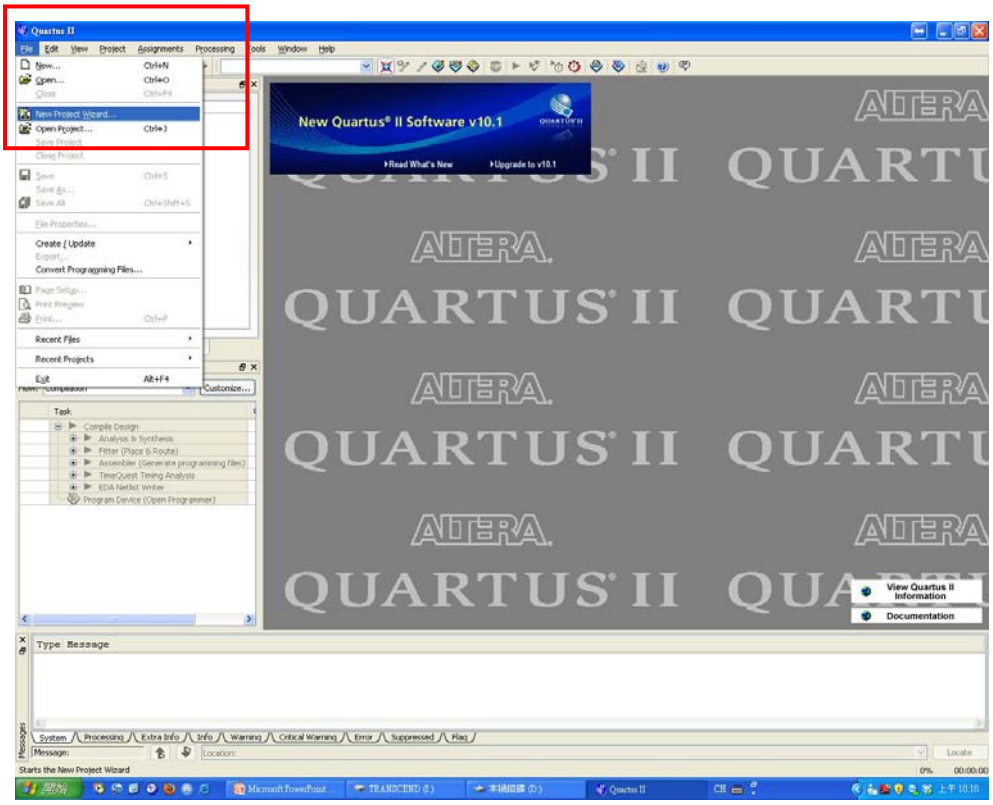


5. 過程中會連續出現以下兩個畫面

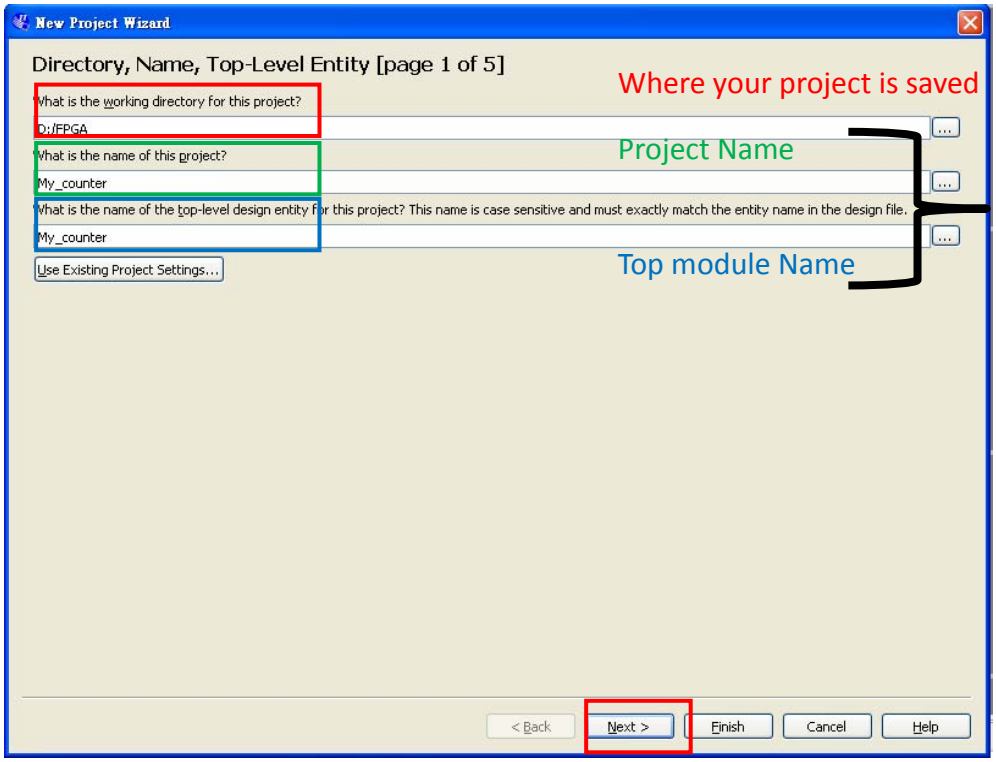
6. 最後按下「完成」完成安裝

三、實驗步驟

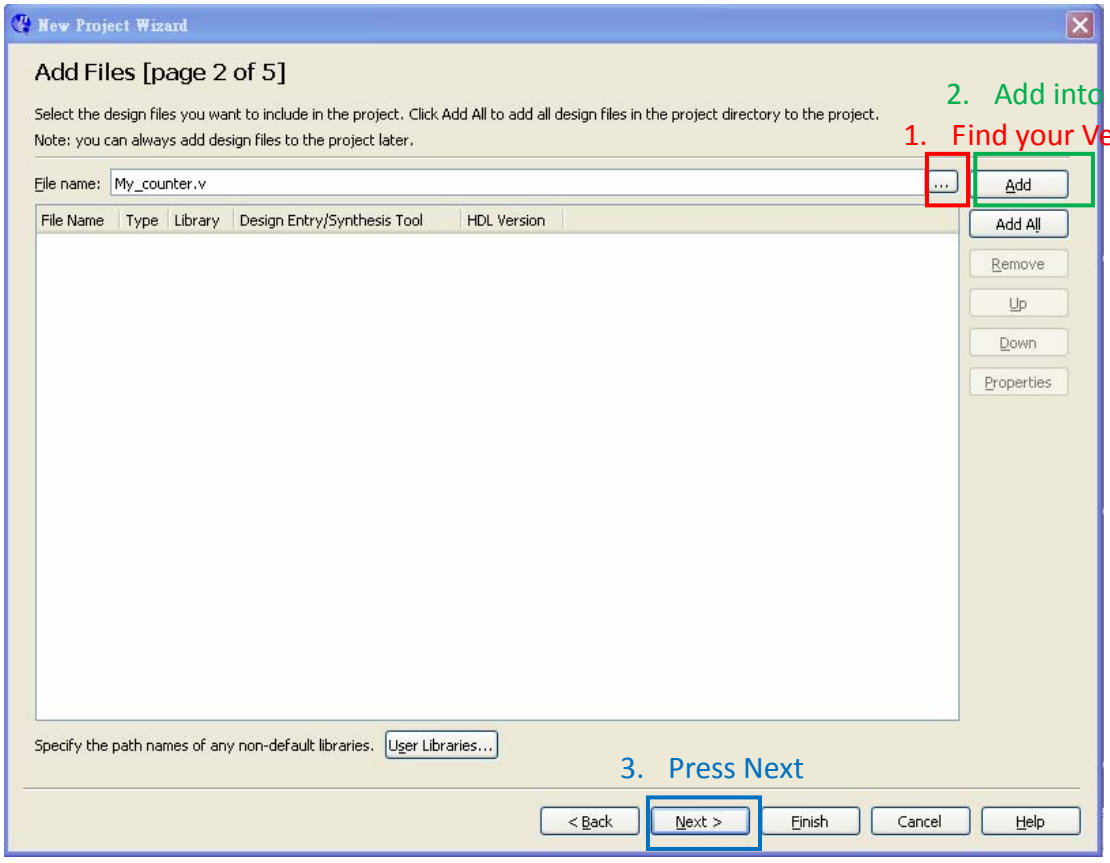
1. Open “Quartus II 10.1 Web Edition (32-Bit)”
2. File->New project wizard



3. The name of top module must be the same as your verilog code!

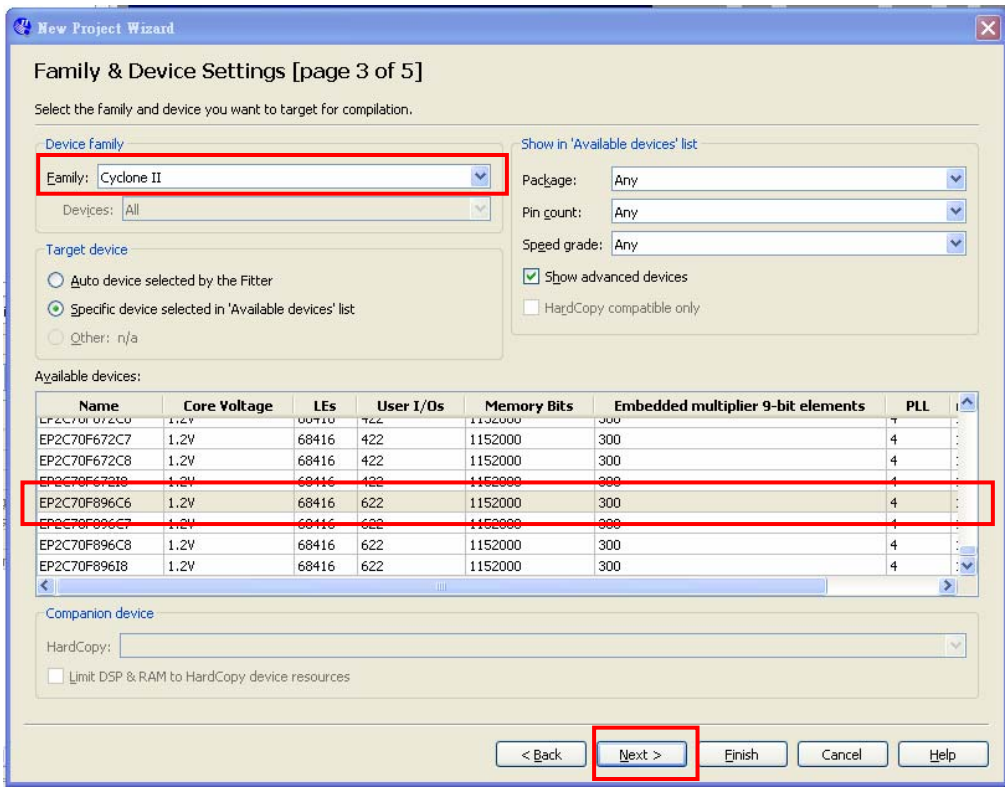


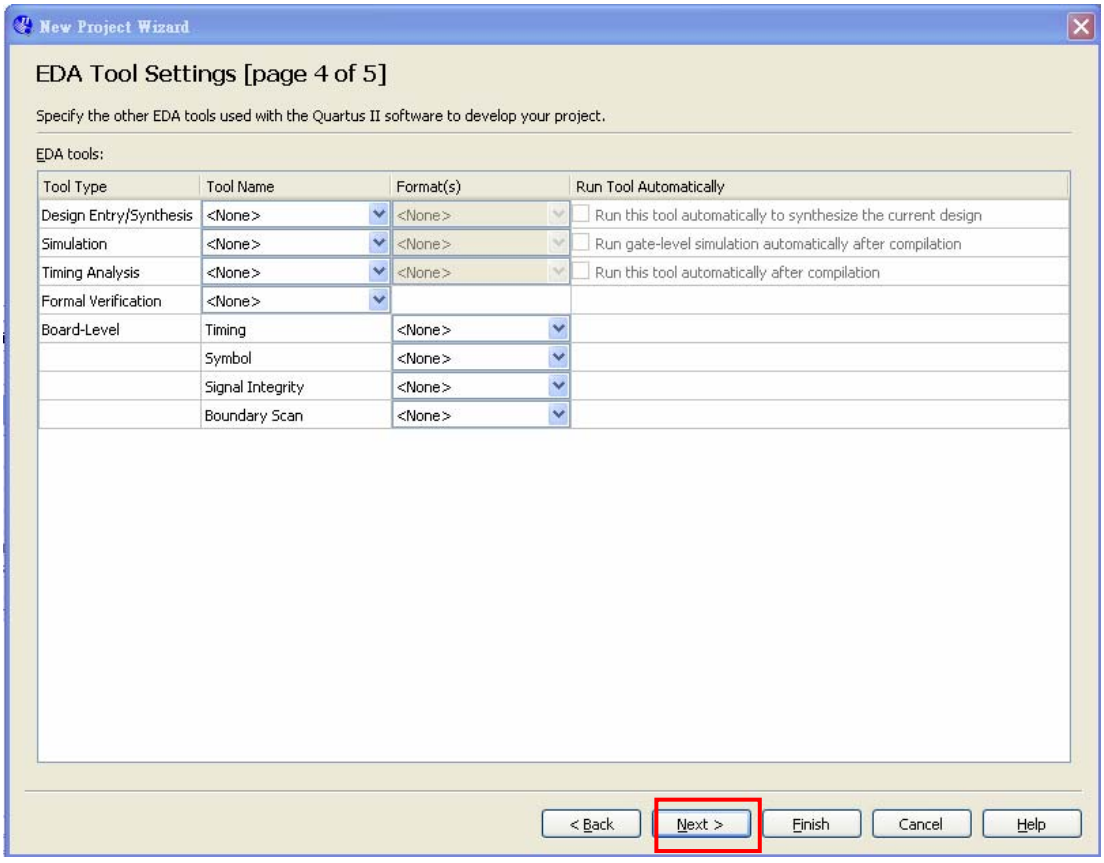
4.

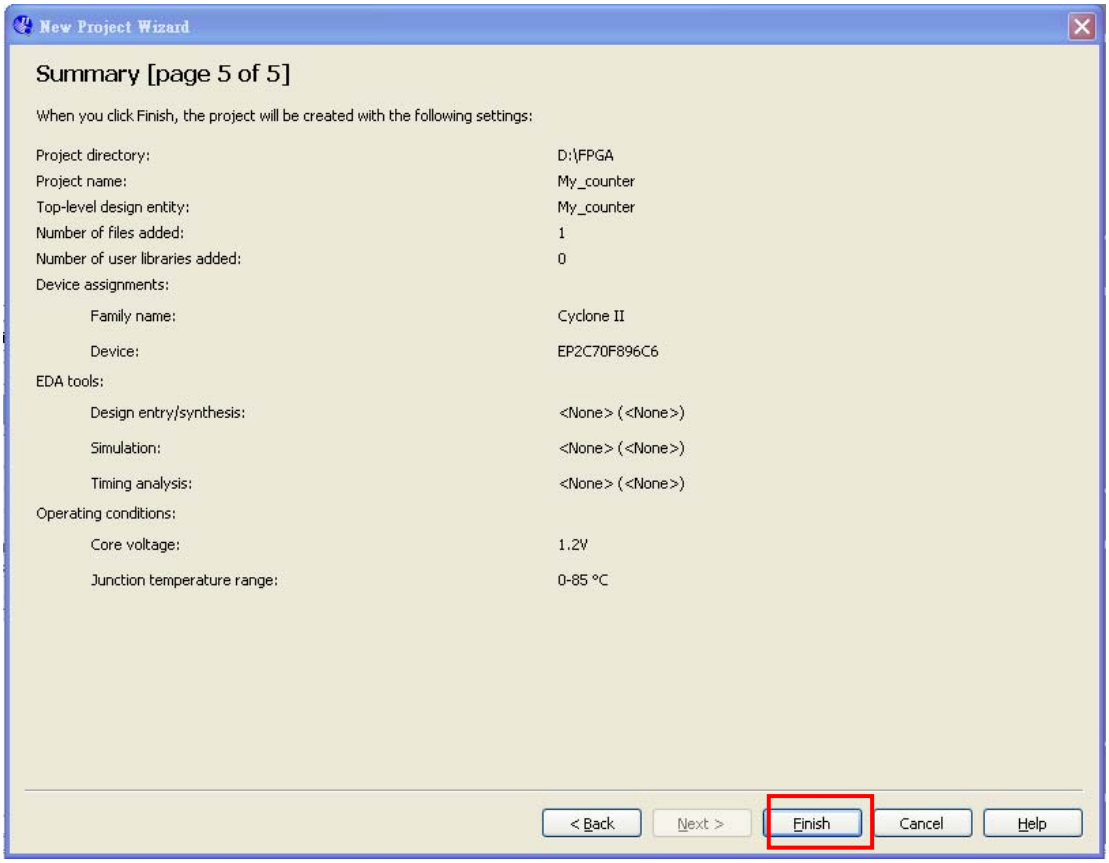


5. Select the FPGA you are going to use

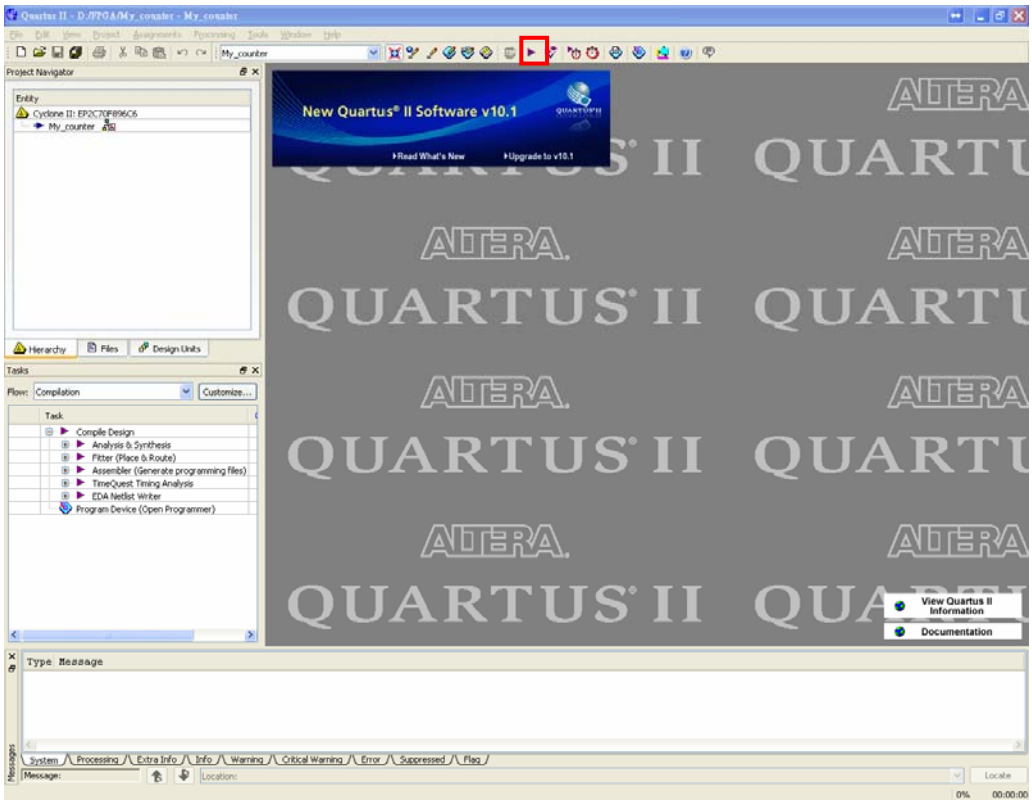
In this lab, choose “Family: Cyclone II”, and for DE2-70 choose “EP2C70F896C6”


New Project Wizard
Family & Device Settings [page 3 of 5]
Select the family and device you want to target for compilation.
Device family
Family: Cyclone II
Devices: All
Target device
Auto device selected by the Fitter
Specific device selected in 'Available devices' list
Other: n/a
Show in 'Available devices' list
Package: Any
Pin count: Any
Speed grade: Any
Show advanced devices
HardCopy compatible only
Available devices:
Name | Core Voltage | LEs | User I/Os | Memory Bits | Embedded multiplier 9-bit elements | PLL
EP2C70F672C7 | 1.2V | 68416 | 422 | 1152000 | 300 | 4
EP2C70F672C8 | 1.2V | 68416 | 422 | 1152000 | 300 | 4
EP2C70F896C6 | 1.2V | 68416 | 622 | 1152000 | 300 | 4
EP2C70F896C8 | 1.2V | 68416 | 622 | 1152000 | 300 | 4
EP2C70F896I8 | 1.2V | 68416 | 622 | 1152000 | 300 | 4
Companion device
HardCopy:
Limit DSP & RAM to HardCopy device resources
< Back
Next >
Finish
Cancel
Help

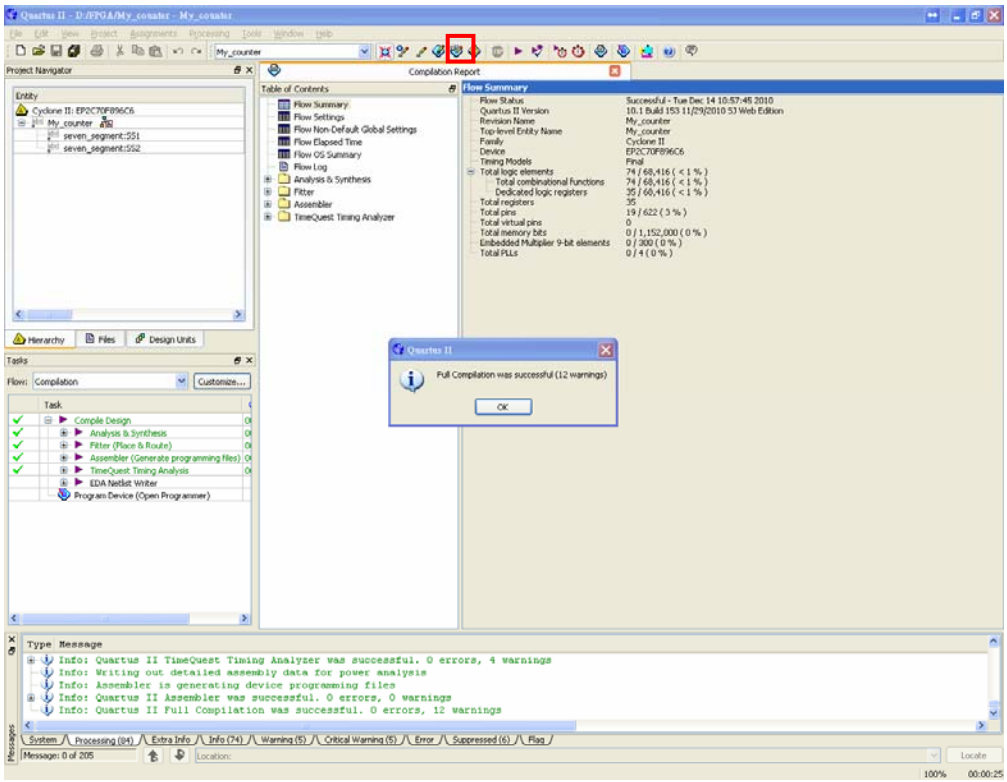

New Project Wizard
EDA Tool Settings [page 4 of 5]
Specify the other EDA tools used with the Quartus II software to develop your project.
EDA tools:
Tool Type | Tool Name | Format(s) | Run Tool Automatically
Design Entry/Synthesis | <None> | <None> | Run this tool automatically to synthesize the current design
Simulation | <None> | <None> | Run gate-level simulation automatically after compilation
Timing Analysis | <None> | <None> | Run this tool automatically after compilation
Formal Verification | <None>
Board-Level | Timing | <None>
Symbol | <None>
Signal Integrity | <None>
Boundary Scan | <None>
< Back
Next >
Finish
Cancel
Help

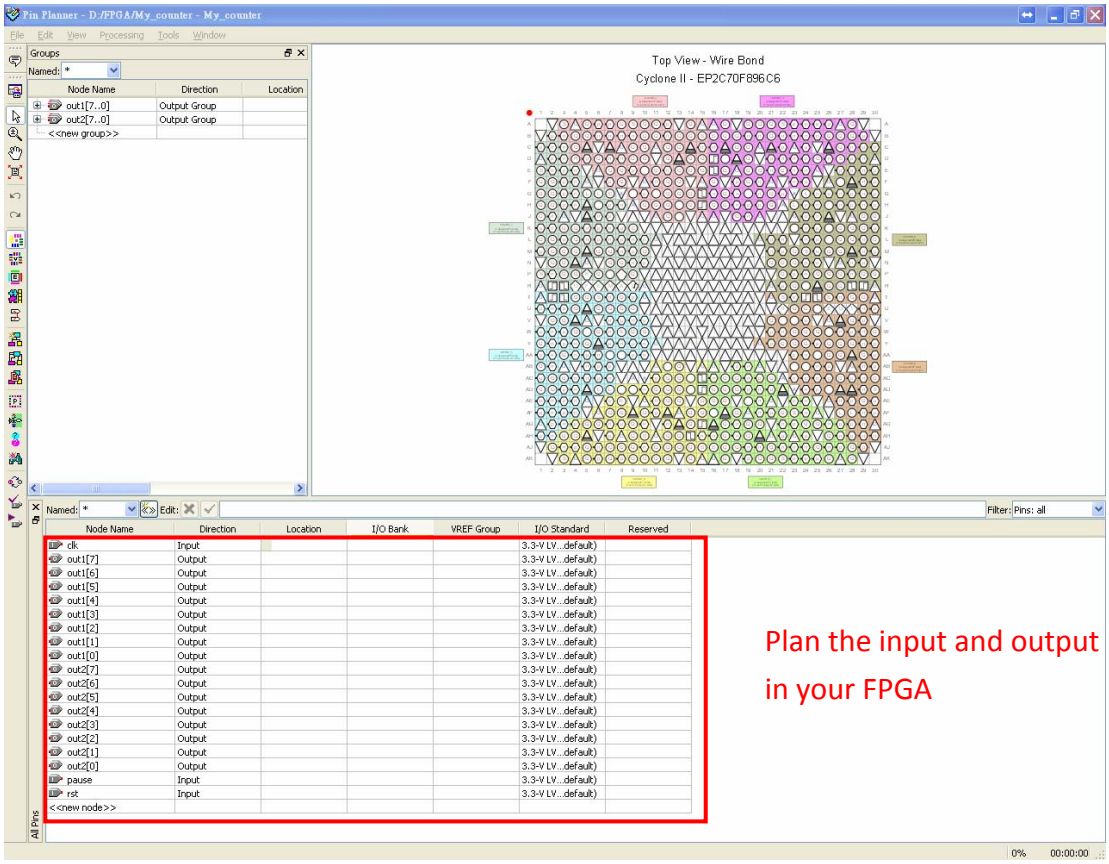

New Project Wizard
Summary [page 5 of 5]
When you click Finish, the project will be created with the following settings:
Project directory: D:\FPGA
Project name: My_counter
Top-level design entity: My_counter
Number of files added: 1
Number of user libraries added: 0
Device assignments:
Family name: Cyclone II
Device: EP2C70F896C6
EDA tools:
Design entry/synthesis: <None> (<None>)
Simulation: <None> (<None>)
Timing analysis: <None> (<None>)
Operating conditions:
Core voltage: 1.2V
Junction temperature range: 0-85 °C
< Back
Next >
Finish
Cancel
Help

6. Press the start compilation (Ctrl+L)



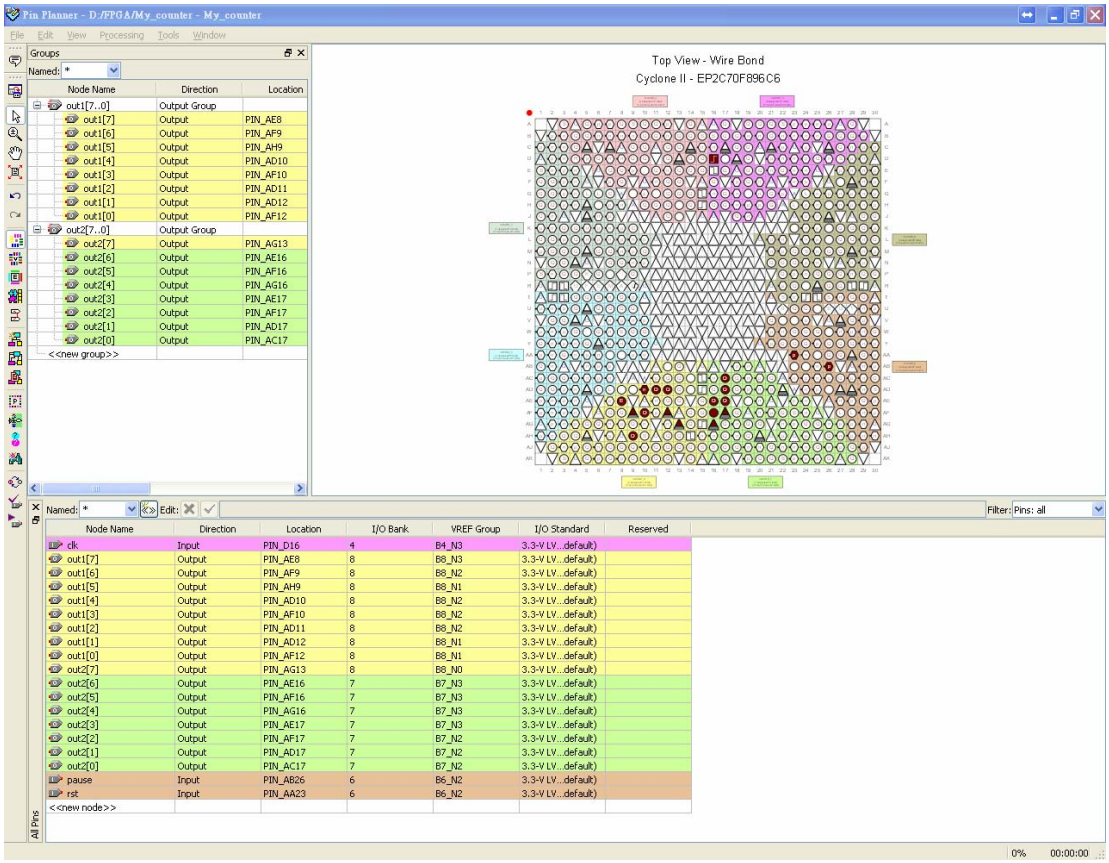
7. Use “Pin Planner” to plan the input and output in your FPGA. In other words, connect your verilog code and FPGA by setting the location of each I/O according to the user manual of FPGA.



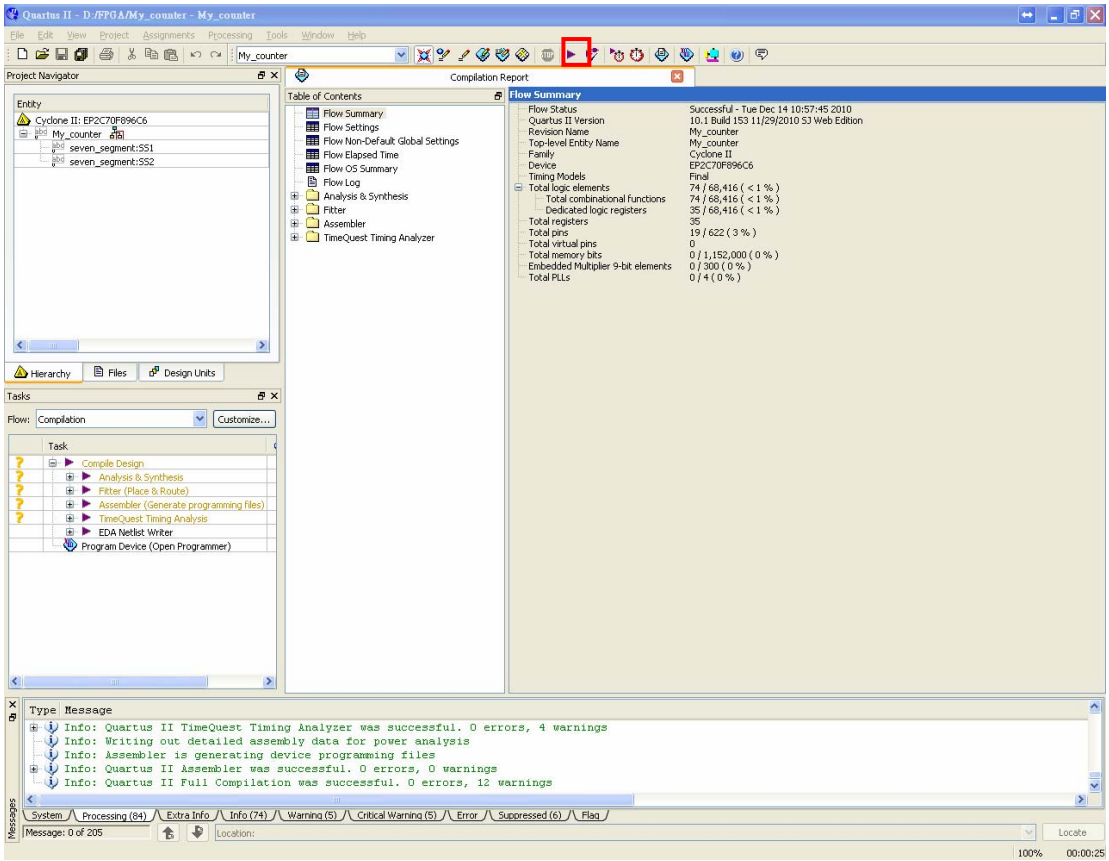


	DE2-70
Clk	PIN_D16
out1[7]	PIN_AE8
out1[6]	PIN_AF9
out1[5]	PIN_AH9
out1[4]	PIN_AD10
out1[3]	PIN_AF10
out1[2]	PIN_AD11
out1[1]	PIN_AD12
out1[0]	PIN_AF12
out2[7]	PIN_AG13
out2[6]	PIN_AE16
out2[5]	PIN_AF16
out2[4]	PIN_AG16
out2[3]	PIN_AE17
out2[2]	PIN_AF17
out2[1]	PIN_AD17
out2[0]	PIN_AC17
pause	PIN_AB26
rst	PIN_AA23

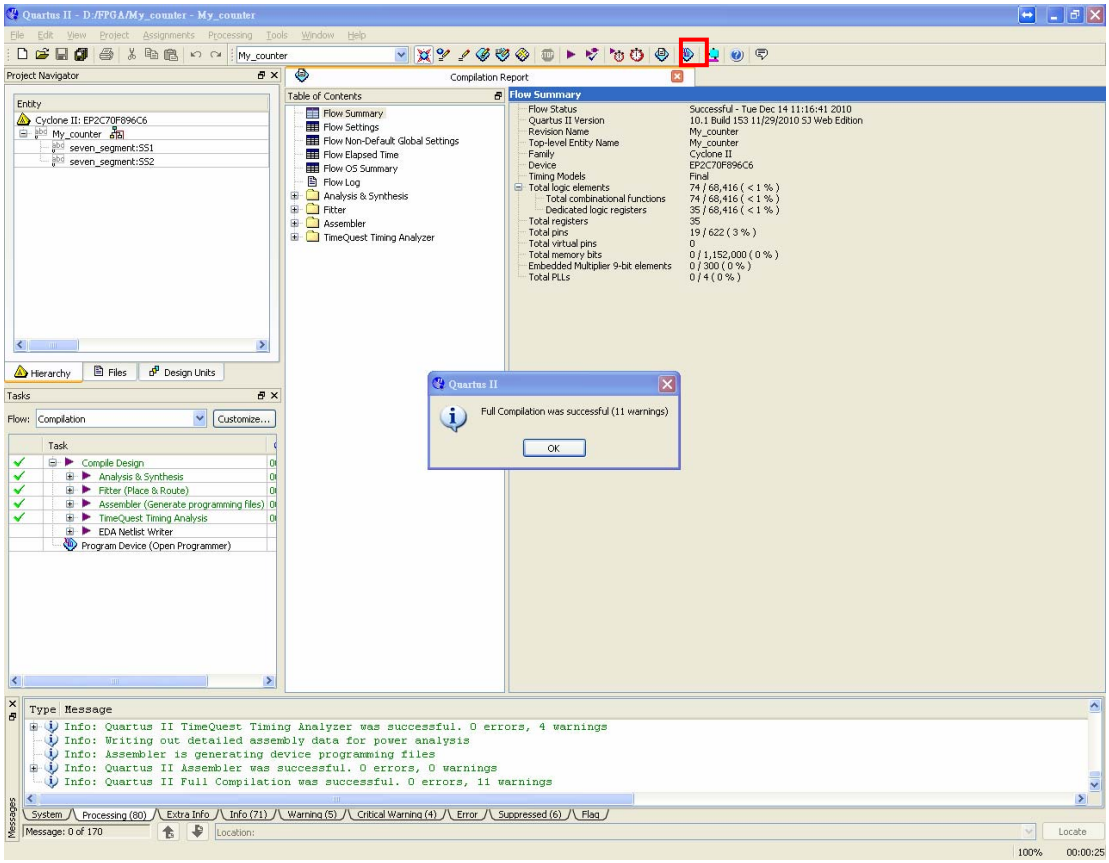
Example for DE2-70:

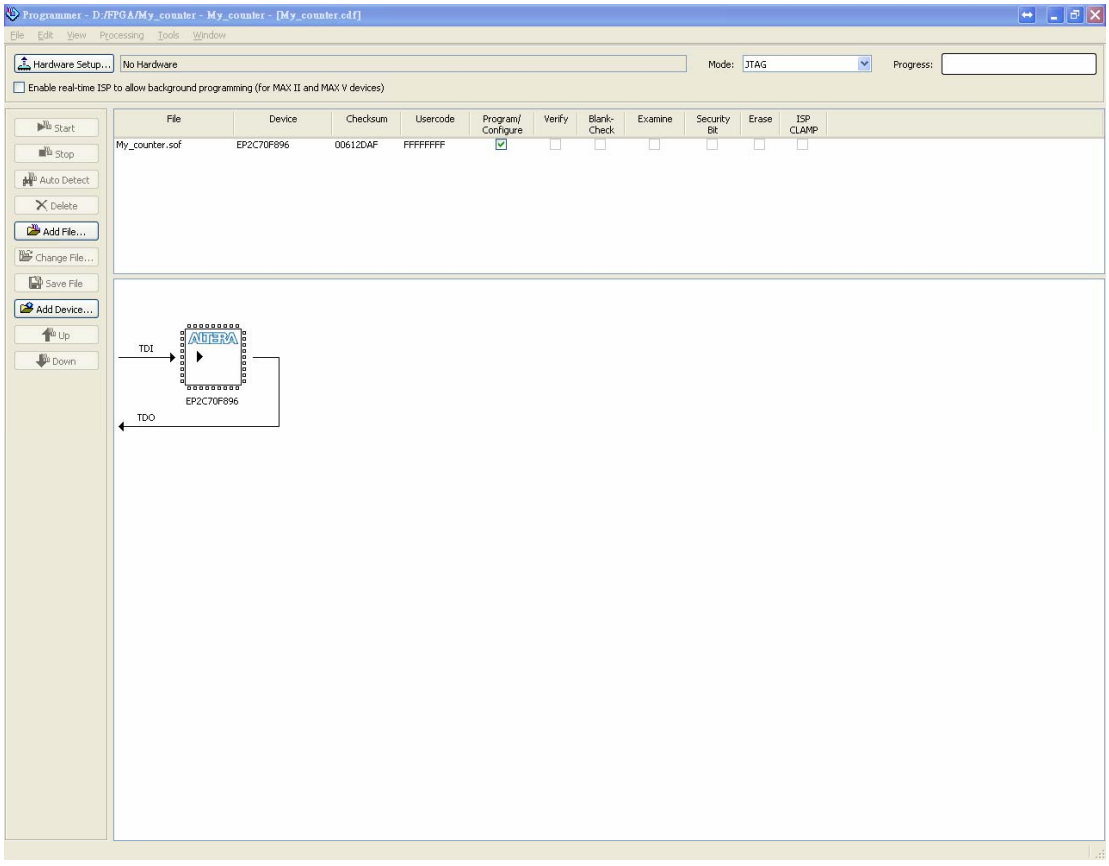


8. After pin planner, another compilation is required!

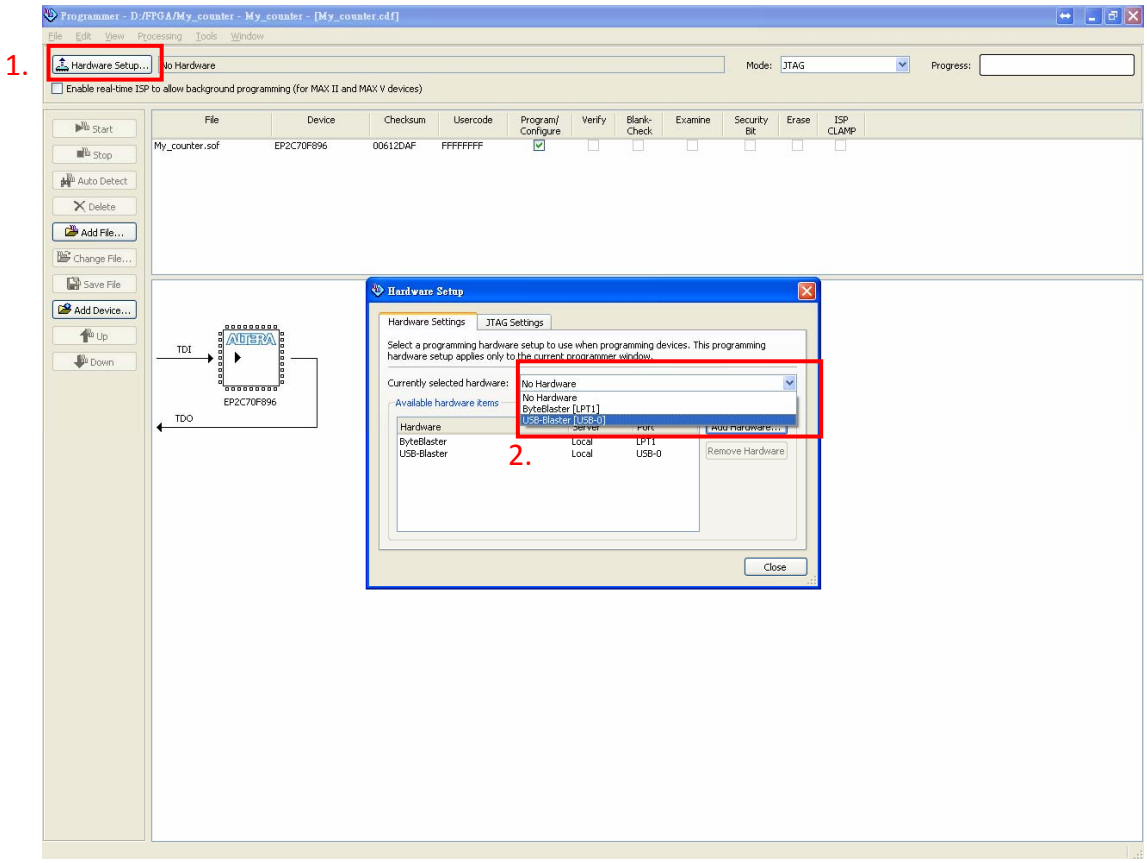


9. Next, use “Programmer” from "tool → programmer"

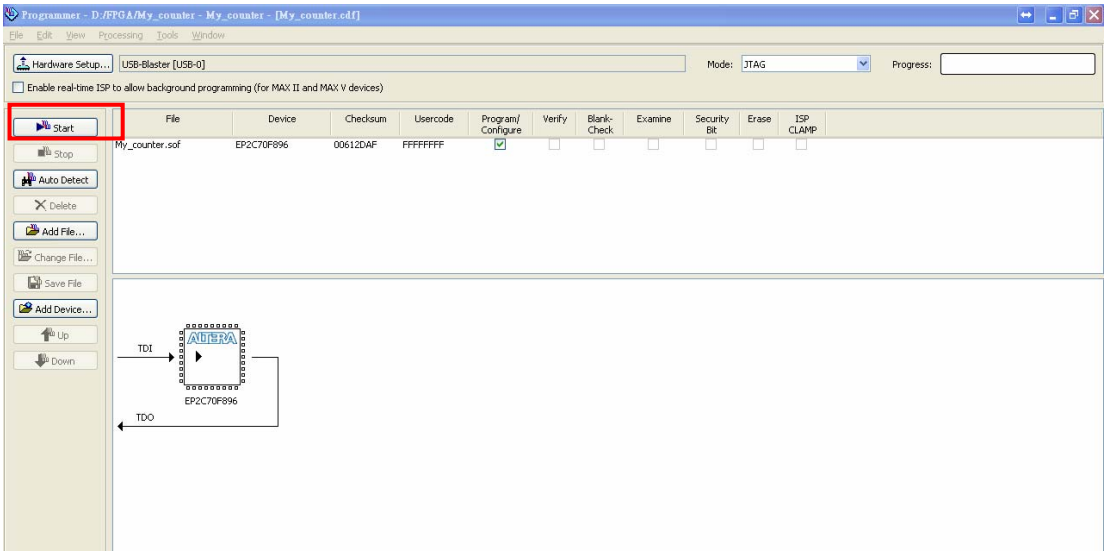




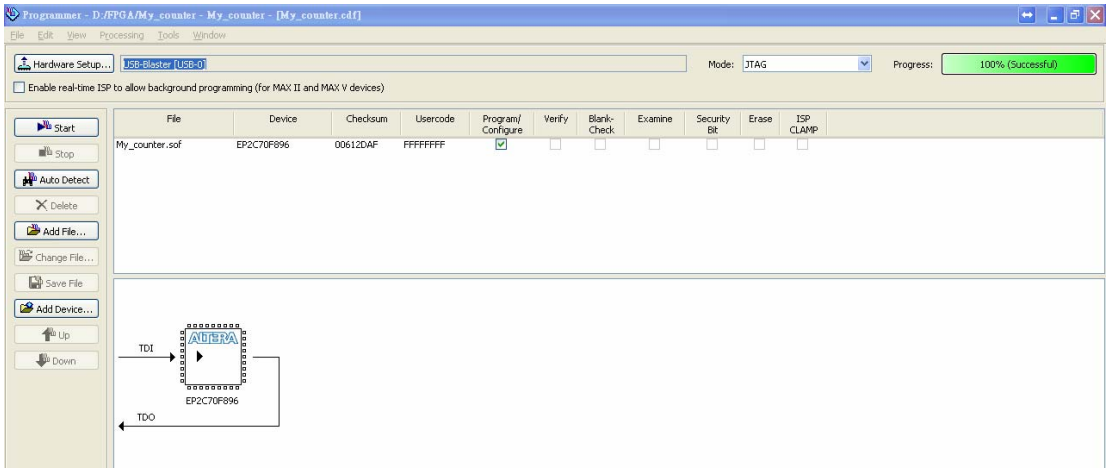
10. You must first connect your FPGA and choose “Hardware setup -> USB-Blaster”.

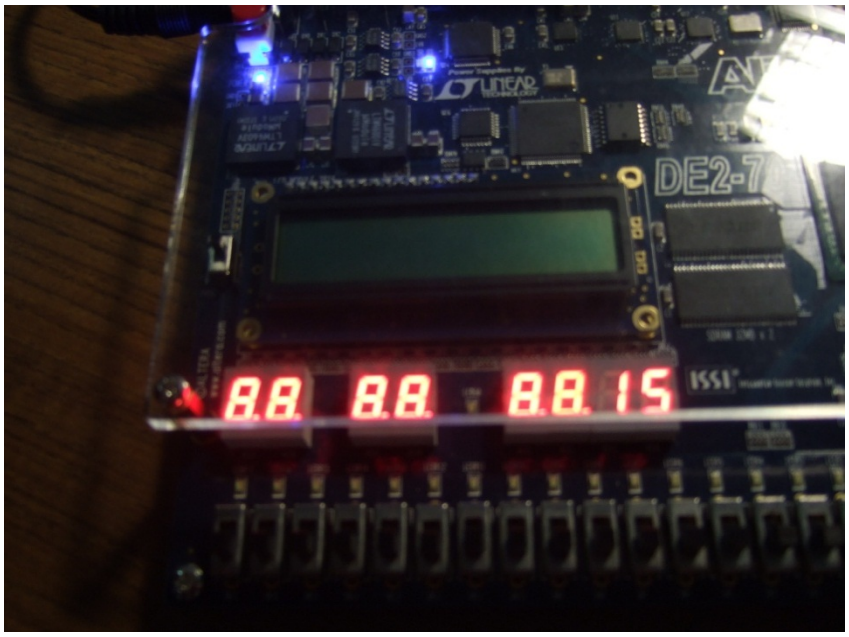


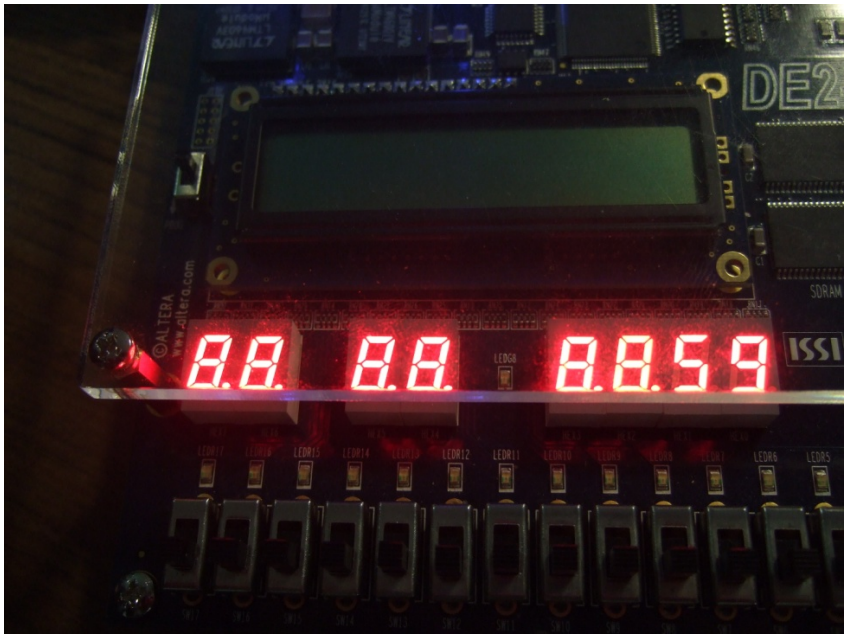
11. Press Start and FPGA will start to work!



12. Counter is counting！ (SW0-> reset, SW1-> pause)







Exercises

Add one output port which lights the LEDR0 when the counter is counting and turns off the LEDR0 when the counter is not counting.