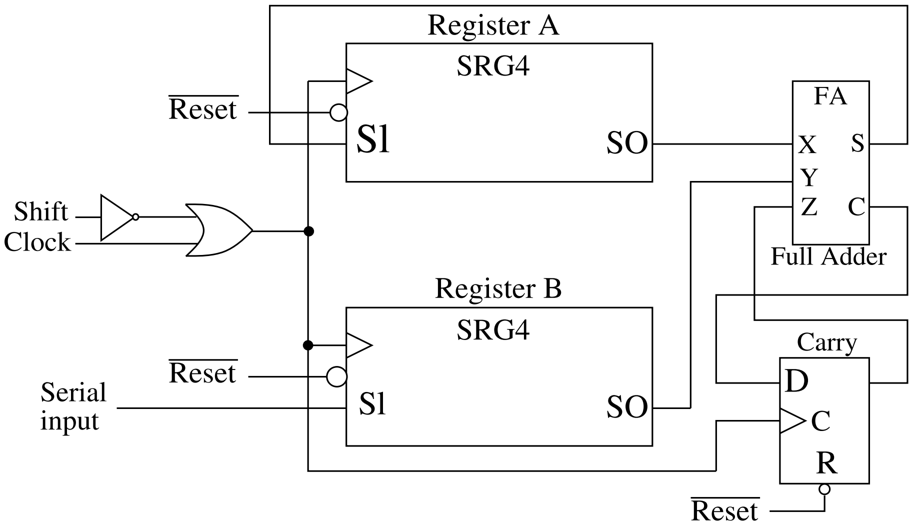
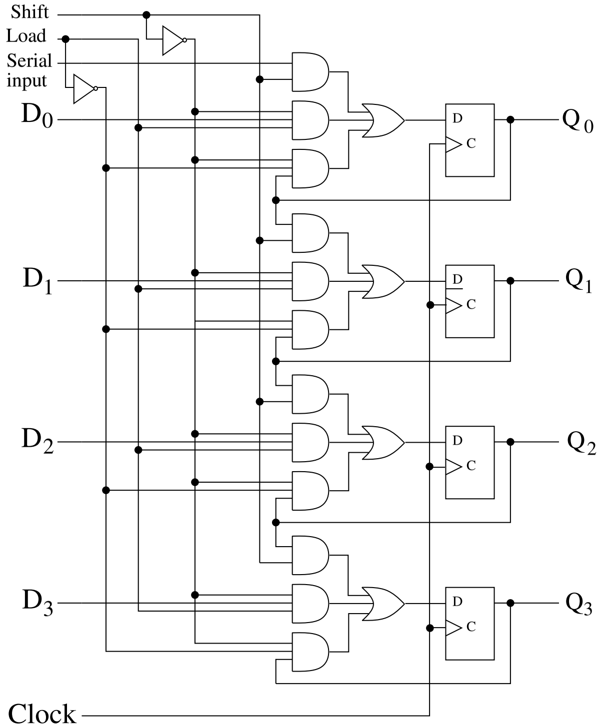
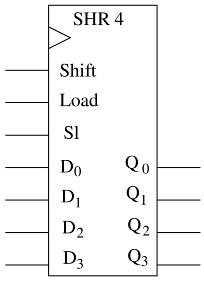
Serial Addition

- Add two numbers (held in registers A and B) serially, starting at the least significant bit.
- The serial adder is slower but smaller than the parallel (ripple-carry) adder.



Shift Register with Parallel Load





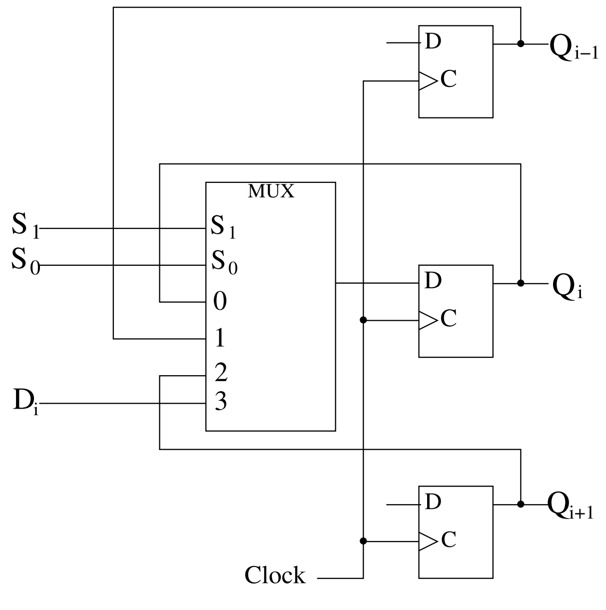
(b) Symbol

Shift	Load	Operation
0	0	No change
0	1	Load parallel data
1	X	Shift down from Q_0 to Q_3

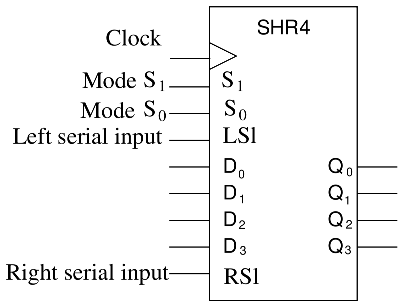
- Application: Load an n-bit data in parallel into a shift register and then transmit the data serially.

Bidirectional Shift Register

- By feeding a 4-input multiplexer to each D flip-flop in a shift register, we can implement a device which **shifts right, shifts left, holds, parallel loads**.



(a) Logic diagram of one typical stage



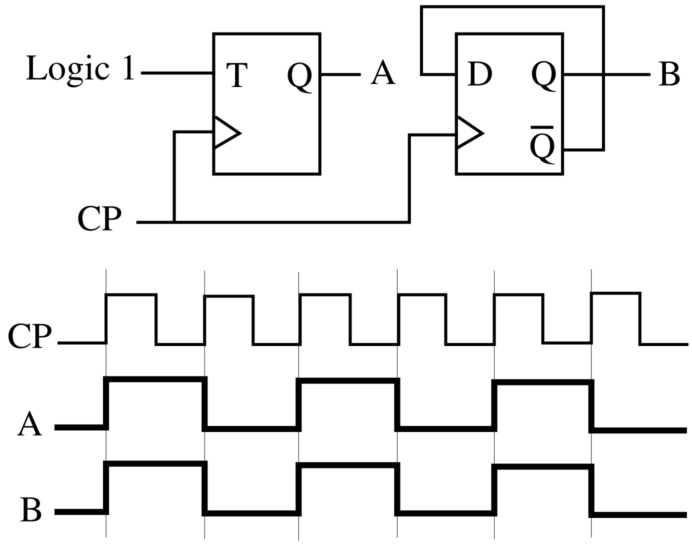
(b)Symbol

Mode control		Register Operation
S_1	S_0	
0	0	No change
0	1	Shift down
1	0	Shift up
1	1	Parallel load

Counter

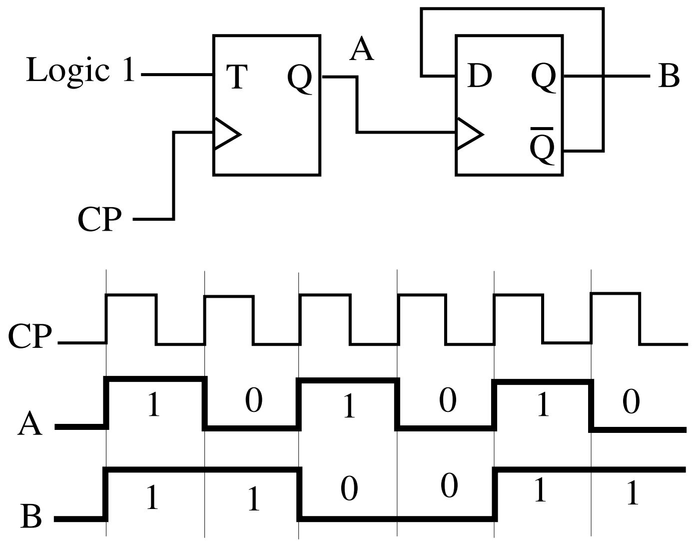
- **Counter:** A register that goes through a prescribed sequence of states upon the application of input pulses.
- An n-bit **binary counter** consists of n flip-flops and can count in binary from 0 through $2^n - 1$.
- Two types of counters
  - **Ripple counters:** The flip-flop output transition serves as a source for triggering other flip-flops.
  - **Synchronous counters:** The Clk inputs of all flip-flops receive the common clock pulse, and the change of state is determined from the present state of the counter.

A "Divide-by-2" Counter



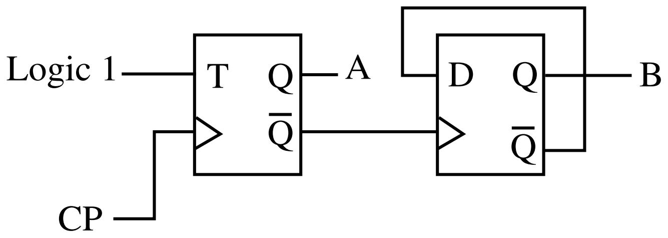
- The frequency of the output waveform is half the clock CP ("divide-by-2").

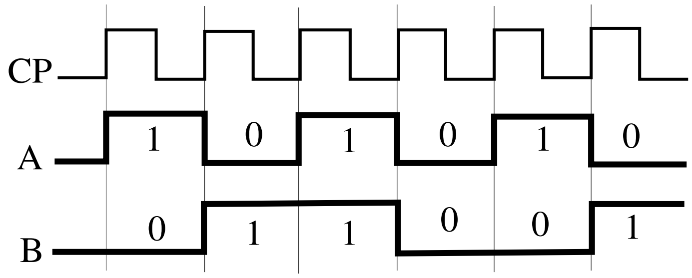
Down Ripple Counter



- B "divides" the frequency in A by 2 (doubles the period).
- Count (B, A) base 2: $3 \longrightarrow 2 \longrightarrow 1 \longrightarrow 0 \longrightarrow 3 \longrightarrow 2 \longrightarrow ...$.

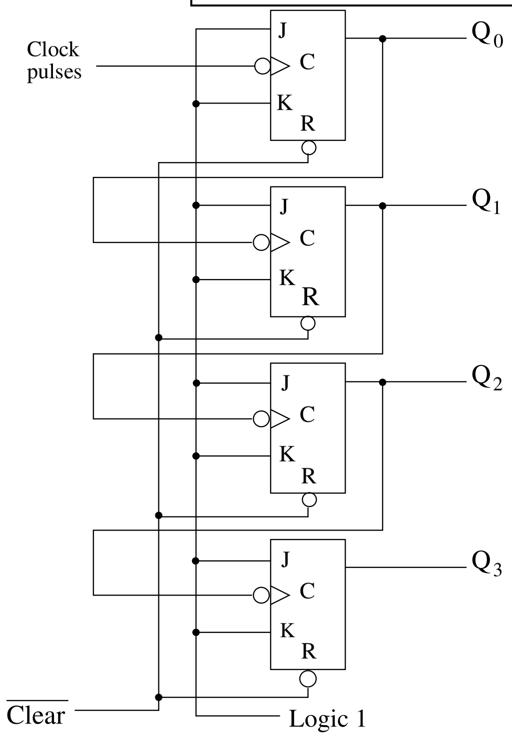
Up Ripple Counter





- B "divides" the frequency in A by 2 (doubles the period).
- Count (B, A) base 2: $0 \longrightarrow 1 \longrightarrow 2 \longrightarrow 3 \longrightarrow 0 \longrightarrow 1 \longrightarrow \ldots$

4-Bit Up Ripple Counter



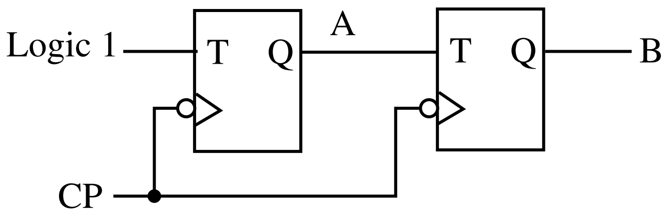
Upward Couting Sequence

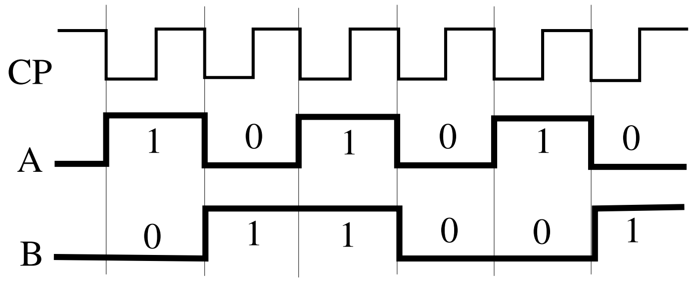
Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

- Each edge sensitive transition causes a change in the next flip-flop's state.

Synchronous Counter

- The common clock pulse triggers all flip-flops simultaneously.
- A 2-bit synchronous up counter made with two T flip-flops.





Synchronous Binary Counter with JK Flip-Flops

Present state				Next state				Flip–flop inputs							
Q_3	Q_2	Q_1	Q_0	Q_3	Q_2	Q_1	Q_0	J_{Q3}	K_{Q3}	J_{Q2}	K_{Q2}	J_{Q1}	K_{Q1}	J_{Q0}	K_{Q0}
0	0	0	0	0	0	0	1	0	X	0	X	0	X	1	X
0	0	0	1	0	0	1	0	0	X	0	X	1	X	X	1
0	0	1	0	0	0	1	1	0	X	0	X	X	0	1	X
0	0	1	1	0	1	0	0	0	X	1	X	X	1	X	1
0	1	0	0	0	1	0	1	0	X	X	0	0	X	1	X
0	1	0	1	0	1	1	0	0	X	X	0	1	X	X	1
0	1	1	0	0	1	1	1	0	X	X	0	X	0	1	X
0	1	1	1	1	0	0	0	1	X	X	1	X	1	X	1
1	0	0	0	1	0	0	1	X	0	0	X	0	X	1	X
1	0	0	1	1	0	1	0	X	0	0	X	1	X	X	1
1	0	1	0	1	0	1	1	X	0	0	X	X	0	1	X
1	0	1	1	1	1	0	0	X	0	1	X	X	1	X	1
1	1	0	0	1	1	0	1	X	0	X	0	0	X	1	X
1	1	0	1	1	1	1	0	X	0	X	0	1	X	X	1
1	1	1	0	1	1	1	1	X	0	X	0	X	0	1	X
1	1	1	1	0	0	0	0	X	1	X	1	X	1	X	1

- 16 states from 0000 to 1111.
- $J_{Q0} = K_{Q0} = 1$; $J_{Q1} = K_{Q1} = Q_0$; $J_{Q2} = K_{Q2} = Q_0Q_1$; $J_{Q3} = K_{Q3} = Q_0Q_1Q_2$.
- In general, $J_{Qi} = K_{Qi} = Q_0Q_1 \dots Q_{i-1}$.