Universal Switch Blocks for Three-Dimensional FPGA Design

Guang-Ming Wu, Michael Shyu, and Yao-Wen Chang
Department of Computer and Information Science
National Chiao Tung University
Hsinchu, Taiwan ROC

Abstract

Universal switch blocks for conventional FPGAs were first studied in [3]. In this paper, we consider the switch-block design problem for three-dimensional FPGAs. A three-dimensional switch block M with W terminals on each face is said to be universal *if every set of nets satisfying the dimension constraint (i.e., the number of nets on each face of M is at most W) is simultaneously routable through M. In this paper, we present a class of universal switch blocks for three-dimensional FPGAs. Each of our switch blocks has $15W$ switches and* switch-block flexibility *5 (i.e., $F_S = 5$). We prove that no switch block with less than $15W$ switches can be universal. We also compare our switch blocks with others of the topology associated with those used in the Xilinx XC4000 FPGAs. Experimental results demonstrate that our universal switch blocks improve routabilty at the chip level.*

1 Introduction

A conventional FPGA (see Figure 1(a)) consists of an array of logic blocks that can be connected by routing resources [2]. The logic blocks contain circuits used to implement logic functions. The routing resources consist of wire segments and switch blocks. An intersection of a horizontal and a vertical channels is referred to as a switch block; the switch block serves to connect wire segments, and this requires using programmable switches inside it. Figure 1(b) illustrates a switch block in which the programmable switches, denoted by dashed lines between terminals, are shown.

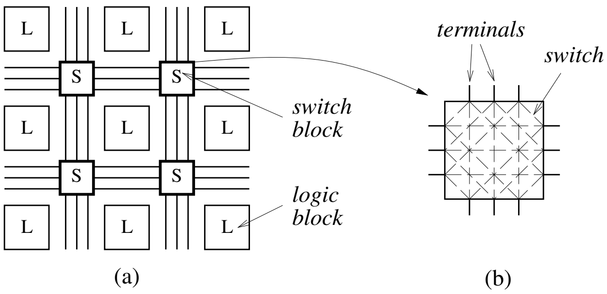

Figure 1: A conventional FPGA and its switch block. (a) A conventional FPGA architecture. (b) A conventional 4-sided switch block.

For the work on conventional switch blocks (4-sided blocks), Rose and Brown defined the flexibility of a switch block, represented by F_S, as the number of programming switches between a terminal and others [8]. They investigated the effects of different switch-block flexibilities on routing and suggested that $F_S = 3$ often be sufficient for high routability. Chang, Wong, and Wong first presented a class of *universal switch blocks* [3]. A switch block M with W terminals on each side is said to be *universal* if every set of nets satisfying the dimension constraint (i.e., the number of nets on each side of M is at most W) is simultaneously routable through M [3]. They proved that each of the universal switch blocks can accommodate significantly more routing instances than the Xilinx XC4000-type one of the same size. Recently, a report on the layout implementations of the universal switch blocks and the XC4000-type ones has also concluded that the universal switch blocks are a better switch component [11]. Another switch-module architecture called *switch matrices* was modeled and investigated by Zhu, Wong, and Chang [13] and Sun, Wang, Wong, and Liu [9]. Chang, Wong, and Wong later proposed a network-flow based algorithm for switch-matrix design. Wu and Chang recently showed the nonexistence of universal switch *matrices* and presented a class of quasi-universal switch matrices with almost the same routing capacity as universal switch *blocks* [12].

MCM fabrication techniques for multiple FPGAs have been studied recently [1, 5]. An MCM-based field programmable architecture for prototyping large designs using multiple FPGAs was proposed in [6]. A three-dimensional (3D) FPGA architecture by stacking together a number of two-dimensional (2D) FPGAs was studied in [1]. A three-dimensional FPGA architecture (see Figure 2(a)) is a generalization based on the conventional 2D FPGA; it stacks a number of 2D FPAG blocks together by MCM fabrication techniques, where each logic block has six adjacent neighbors, as opposed to four in the 2D case [1]. The 3D switch blocks are not the same as the conventional switch blocks (see Figure 2(b)). Each switch block is connected with six adjacent switch blocks. Therefore, they enable each channel segment to connect to some subset of the channel segments incident on the other five faces of the 3D switch block. This unique architecture motivates our study of the 3D switch blocks.

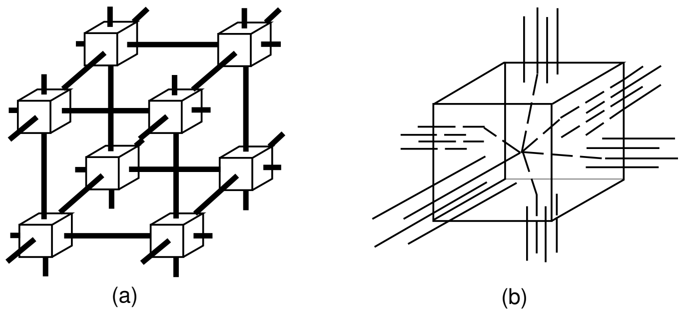

Figure 2: (a) 3D FPGA, (b) 3D switch block.

In this paper, we consider the switch-block design problem for three-dimensional FPGAs. A three-dimensional switch block M with W terminals on each *face* is said to be *universal* if every set of nets satisfying the dimension constraint (i.e., the number of nets on each *face* of M is at most W) is simultaneously routable through M. In this paper, we present a class of universal switch blocks for three-dimensional FPGAs. Each of our switch blocks has $15W$ switches and *switch-block flexibility* 5 (i.e., $F_S = 5$). We prove that no switch block with less than $15W$ switches can be universal. We also compare our switch blocks with others of the topology associated with those used in the Xilinx XC4000 FPGAs. Experimental results demonstrate that our universal switch blocks improve routabilty at the chip level.

The remainder of this article is organized as follows. Section 2 introduces the modeling for 3D switch blocks and their routing. Section 3 presents a class of 3D universal switch blocks and explore their properties. Section 4 considers clique-based switch blocks and compare them with universal switch blocks. Experimental results are reported in Section 5.

2 Switch-Block Modeling

In this section, we present the modeling for 3D switch blocks and their routing. We show that the 3D switch-block design problem can be transformed into the 6-sided one.

A three-dimensional switch block is a cubic block with W terminals on each face of the block. We refer to the *size* of the 3D switch block as W. Some pairs of terminals, on different faces of the block, may have programmable switches and thus can be connected by programming the switches to be "ON." Moreover, these switches are electrically *non-interacting*, unless they share a terminal. We represent a 3D switch block by $M_{3d}(T, S)$, where T is the set of terminals, and S the set of switches. Let the faces F_1, F_2, F_3, F_4, F_5, and F_6 represent the front, hind, left, right, top, and bottom faces, respectively (see Figure 3). Label the terminals $t_{1,1}, t_{1,2}, \ldots, t_{1,W}, t_{2,1}, t_{2,2}, \ldots, t_{2,W}, \ldots, t_{6,1}, t_{6,2}, \ldots, t_{6,W}$ starting from the terminals on F_1 to those on F_6. Let $T(F) = \{t_{1,1}, \ldots, t_{1,W}\}$ *(front terminals)*, $T(H) = \{t_{2,1}, \ldots, t_{2,W}\}$ *(hind terminals)*, $T(L) = \{t_{3,1}, \ldots, t_{3,W}\}$ *(left terminals)*, $T(R) = \{t_{4,1}, \ldots, t_{4,W}\}$ *(right terminals)*, $T(T) = \{t_{5,1}, \ldots, t_{5,W}\}$ *(top terminals)*, and $T(B) = \{t_{6,1}, \ldots, t_{6,W}\}$*(bottom terminals)*. Figure 3(b) shows the labeling of the terminals on F_i. Therefore, $S = \{(t_{i,j}, t_{p,q})|$ there exists a programmable switch between $t_{i,j}$ and $t_{p,q}\}$, and $T = \bigcup_{i \in \{F,H,L,R,T,B\}} T(i)$. For convenience, we often refer to a switch block $M_{3d}(T, S)$ simply as M_{3d}, omitting T and S, if there is no ambiguity about T and S, or T and S are not of concern in the context.

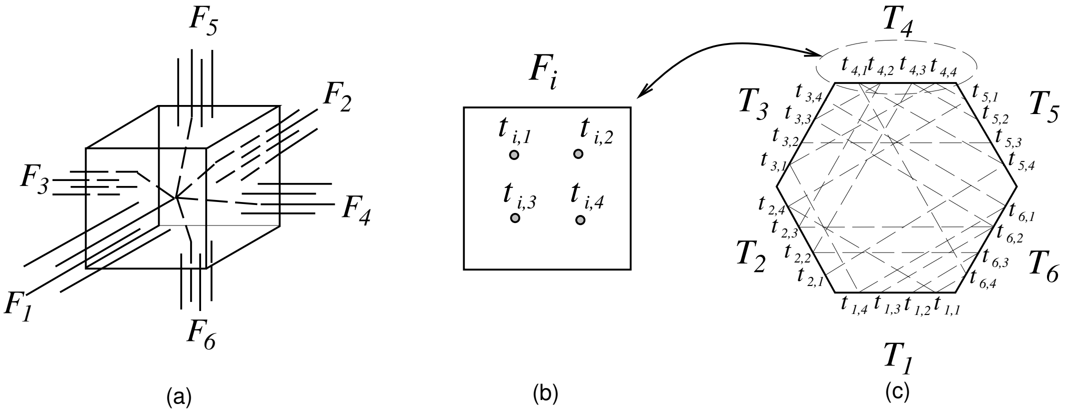

Figure 3: (a) A model of a 3D switch block. (b) One face on the 3D switch block and its terminals. (c) The corresponding 6-sided switch block.

A *hexagonal switch block (HSB)* is a 6-sided switch block with V terminals on each side of the block. We say that the HSB is of *size* V. We represent an HSB by $M_h(T_h, S_h)$, where T_h is the set of terminals, and S_h the set of programming switches. Label the terminals $t_{1,1}, t_{1,2}, \ldots, t_{1,V}$, $t_{2,1}, t_{2,2}, \ldots, t_{2,V}$, $\ldots$, $t_{6,1}, t_{6,2}, \ldots, t_{6,V}$ starting from the rightmost terminal on the bottom side and proceeding clockwise. (See Figure 3(c).) Let $T_h(i) = \{t_{i,1}, \ldots, t_{i,V}\}$, where $i = 1, 2, 3, 4, 5$, or 6. Therefore, $S_h = \{(t_{m,n}, t_{u,v})|$ there exists a programmable switch between terminal $t_{m,n}$ and terminal $t_{u,v}\}$, where $m \neq u$, $m, u = 1, 2, \ldots, 6$, $n, v = 1, 2, \ldots, V$, and $T_h = \cup T_h(i)$, where $i = 1, 2, \ldots, 6$. For convenience, we often refer to $M_h(T_h, S_h)$ simply as M_h, omitting T_h and S_h, if there is no ambiguity about T_h and S_h, or T_h and S_h are not of concern in the context.

In the following, we transform the design problem for the 3D switch blocks into that for the HSBs. For convenience, we modify the terminology *isomorphism* used in [3] as follows. Let $M(T, S)$ $(M'(T', S'))$ be a 3D or a hexagonal switch block. We have the following definition.

Definition 1 *Two switch blocks $M(T, S)$ and $M'(T', S')$ are isomorphic if there exists a bijection f: $T \to T'$ such that $(t_{m,n}, t_{u,v}) \in S$ if and only if $(f(t_{m,n}), f(t_{u,v})) \in S'$ and, for any two terminals $t_{m,n}$, and $t_{u,v}$, $t_{m,n}, t_{u,v} \in T$ if and only if $f(t_{m,n}), f(t_{u,v}) \in T'$.*

In other words, $M(T, S)$ and $M'(T', S')$ are isomorphic if we can relabel the terminals of M to be the terminals of M', maintaining the corresponding switches in M and M'; and for terminals on the same side (face) of M, their corresponding terminals are also on the same side (face) of M'. For any two isomorphic switch blocks, we have the following theorems.

Theorem 1 *[3] Any two isomorphic switch blocks have the same routing capacity.*

Theorem 2 *For any M_{3d} of size W, there exists an M_h of the same size such that M_{3d} and M_h are isomorphic, and vice versa.*

Proof: For an $M_{3d}(S,T)$ of size W, we can construct an $M_h(S_h,T_h)$ of the same size such that $(t_{m,n}, t_{u,v}) \in S_h$ if $(t_{m,n}, t_{u,v}) \in S$, where $m \neq u, m, u = 1, 2, \ldots, 6$ and $n, v = 1, 2, \ldots, W$. Let the mapping function f: $T \rightarrow T_h$ be $f(t_{m,n}) = t_{m,n}$. Obviously, $(t_{m,n}, t_{u,v}) \in S$ if and only if $(f(t_{m,n}), f(t_{u,v})) = (t_{m,n}, t_{u,v}) \in S_h$. Therefore, by Definition 1, M_{3d} and M_h are isomorphic.

For an $M_h(S_h,T_h)$ of size V, we can construct an $M_{3d}(S,T)$ of the same size such that $(t_{m,n}, t_{u,v}) \in S$ if $(t_{m,n}, t_{u,v}) \in S_h$, where $m \neq u, m, u = 1, 2, \ldots, 6$ and $n, v = 1, 2, \ldots, V$. Similarly, there exists the bijection f': $T_h \rightarrow T$ such that $f(t_{m,n}) = t_{m,n}$ and $(t_{m,n}, t_{u,v}) \in S_h$ if and only if $(f(t_{m,n}), f(t_{u,v})) = (t_{m,n}, t_{u,v}) \in S$. Therefore, M_{3d} and M_h are isomorphic $\square$

By Theorems 1 and 2, the design problem for the 3D switch block is equivalent to that for the 6-sided switch block. Therefore, we shall focus on the 6-sided switch block in the rest of the paper.

In an HSB, the switches are electrically *non-interacting* unless they share a terminal. A *connection* is an electrical path between two terminals (say $t_{m,n}$ and $t_{u,v}$) on different sides of a switch block. If the switch ($t_{m,n}$, $t_{u,v}$) is programmed to be "ON," then a connection between these two terminals is established. Because each connection is characterized by two sides of a block, we can classify all connections passing through a switch block into a number of categories. For an HSB, connections can be of 15 types. See Figure 4 for the type definition.

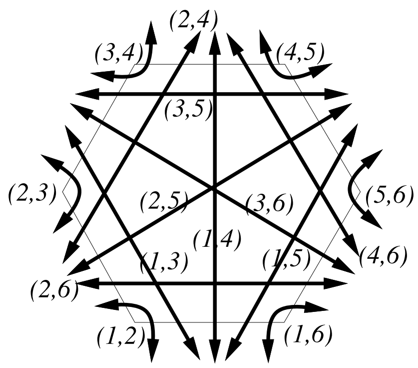

Figure 4: 15 types of connections in an HSB.

A *routing requirement vector* (*RRV*) $\vec{n}$ for an HSB is a 15-tuple ($n_{1,2}, \ldots, n_{1,6}, n_{2,3}, \ldots, n_{2,6}$, $n_{3,4}, \ldots, n_{3,6}$ $, n_{4,5}, n_{4,6}, n_{5,6}$), where $n_{i,j}$ is the number of type-(i,j) connections required to be routed through an HSB, $0 \leq n_{i,j} \leq V$, $i, j = 1, 2, \ldots, 6, i \neq j$. An RRV $\vec{n}$ is said to be *routable* on an HSB M_h if there exists a routing for $\vec{n}$ on M_h. For example, Figure 5(a) shows a routing instance with three nets and the RRV $\vec{n} = (0,0,0,0,0,1,1,0,0,1,0,0,0,0,0)$, and Figures 5(b) and (c) show two HSBs with the same flexibility ($F_S = 5$). The RRV $\vec{n}$ is routable on the HSB shown in Figure 5(b), and a routing solution is illustrated by the thick lines. In Figure 5(c), however, there is always one net that cannot be routed into M_b. Thus the RRV $\vec{n}$ is not routable on the HSB shown in Figure 5(c).

The *routing capacity* of a switch block M is referred to as the number of distinct routable vectors on M; that is, the routing capacity of M is the cardinality $|\{\vec{n}|\vec{n}$ is routable on $M\}|$. A switch block M with V terminals on each side is called *universal* if every set of nets satisfying the dimension constraint (i.e., the number of nets on each side of M is at most V) is simultaneously routable through M. We have the following definition.

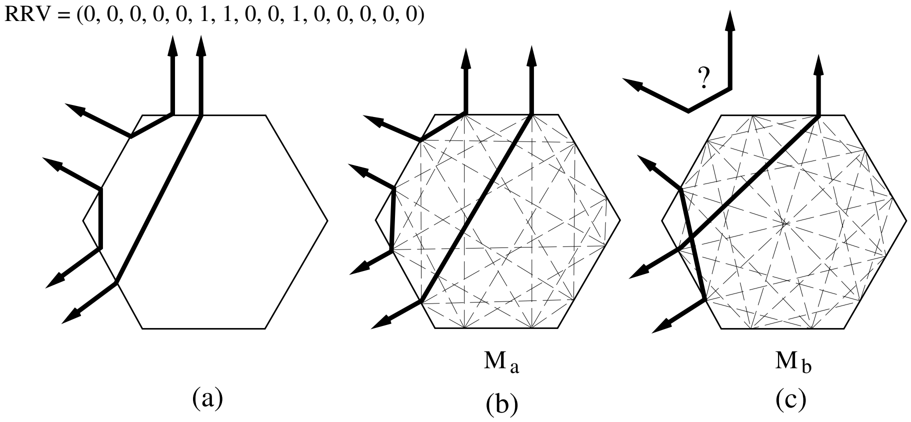

Figure 5: An example of routing on two HSBs of the same size and same flexibility. (a) A routing instance $\vec{n} = (0,0,0,0,0,1,1,0,0,1,0,0,0,0,0)$. (b) $\vec{n}$ is routable on M_a. (c) $\vec{n}$ is not routable on M_b.

Definition 2 *An HSB M_h of size V is called universal if the following set of inequalities is the necessary and sufficient conditions for an RRV $\vec{n} = (n_{1,2}, \ldots, n_{1,6},\ n_{2,3}, \ldots, n_{2,6}, n_{3,4}, \ldots, n_{3,6}, n_{4,5},\ n_{4,6},\ n_{5,6})$ to be routable on M_h:*

$$\begin{aligned}
n_{1,2} + n_{1,3} + n_{1,4} + n_{1,5} + n_{1,6} &\leq V && (1)\\
n_{1,2} + n_{2,3} + n_{2,4} + n_{2,5} + n_{2,6} &\leq V && (2)\\
n_{1,3} + n_{2,3} + n_{3,4} + n_{3,5} + n_{3,6} &\leq V && (3)\\
n_{1,4} + n_{2,4} + n_{3,4} + n_{4,5} + n_{4,6} &\leq V && (4)\\
n_{1,5} + n_{2,5} + n_{3,5} + n_{4,5} + n_{5,6} &\leq V && (5)\\
n_{1,6} + n_{2,6} + n_{3,6} + n_{4,6} + n_{5,6} &\leq V && (6)
\end{aligned}$$

We refer to the *dimension constraint* as the set of inequalities which characterizes a 6-sided universal switch block of size V. Therefore, the dimension constraint for an HSB is the set of Inequalities (1)–(6) listed in Definition 2. Note that the number of nets routed through each side of a switch block can not exceed V; therefore, a universal switch block has the maximum routing capacity.

3 Universal Switch Blocks

In this section, we present an algorithm for constructing symmetric HSBs and prove that the symmetric HSBs are universal. The symmetric HSB of size V has only $15V$ switches. We prove that no HSB with less than $15V$ switches can be universal. Based on isomorphism operations (Theorem 1), we can identify a whole class of universal switch blocks.

3.1 Symmetric Switch Blocks

Algorithm Symmetric_Switch_Block shown in Figure 6 constructs a 6-sided switch block M_h of size V. We refer to the topology of the switch block constructed by the algorithm as the *symmetric topology* and the switch block as the *symmetric switch block*. Figure 7 shows two examples of symmetric switch blocks. For a symmetric switch block, it has the flexibility (F_S) of 5; thus, the total number of switches in the symmetric switch block of size V is equal to $\frac{6 \times V \times F_s}{2} = 3 \times V \times F_s = 15V$.

For a symmetric switch block with an even V terminals on each side, it can be partitioned into $V/2$ sub-blocks of size two; and for an odd V, it can be partitioned into $\lfloor V/2 \rfloor$ sub-blocks of size two and one sub-block of size one. Thus, we have the following property.

Algorithm: Symmetric_Switch_Block(V)
Input: V—size of the hexagonal switch block.
Output: $M_h(T_h, S_h)$—the hexagonal switch block of size V;
T_h: set of terminals; S_h: set of switches.
/* See Figure 3(c) for the terminal labeling. */

1 $T_h \leftarrow t_{i,j}, \quad \forall i = 1, 2, \ldots, 6, \quad \forall j = 1, 2, \ldots, V;$
2 $S_h \leftarrow \emptyset;$
3 **for** $k = 1$ **to** $\lfloor \frac{V}{2} \rfloor$ **do**
4 **for** $i = 1$ **to** 6 **do**
5 **for** $j = 1$ **to** 6 **do**
6 $S_h \leftarrow S_h \cup \{(t_{i,k}, t_{j,V-k+1})\}, \ i \neq j;$
7 **if** V is odd
8 **for** $i = 1$ **to** 6 **do**
9 **for** $j = 1$ **to** 6 **do**
10 $S_h \leftarrow S_h \cup \{(t_{i,\lceil \frac{V}{2} \rceil}, t_{j,\lceil \frac{V}{2} \rceil})\}, \ i \neq j;$
11 **Output** $M_h(T_h, S_h)$.

Figure 6: Algorithm for constructing a 6-sided symmetric switch block of size V.

Lemma 1 *(Switch-Block Decomposition Property) A symmetric switch block of size V can be partitioned into $\lfloor V/2 \rfloor$ symmetric sub-blocks of size two and (V mod 2) symmetric sub-block of size one.*

Proof: Consider Algorithm Symmetric_Switch_Block. For each k in line 3, we construct a symmetric sub-block of size two in lines 4–6. Therefore, we will have $\lfloor V/2 \rfloor$ sub-blocks of size two after $\lfloor V/2 \rfloor$ iterations (see line 3). Further, all these symmetric switch blocks of size two constructed in lines 4–6 have the same topology. Lines 7–10, just for an odd V, construct a clique of six nodes (i.e., a sub-block of size one) from the middle terminal of each side of the switch block. Thus we will have (V mod 2) such sub-block of size one (see lines 7–10). See Figure 8 for illustrations. ∎

Note that these sub-blocks are non-interacting to each other; thus, each sub-block can be considered independently.

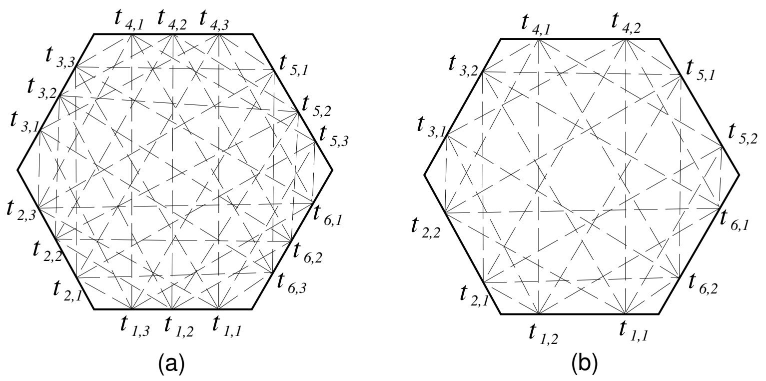

Figure 7: Two symmetric hexagonal switch blocks. (a) A symmetric HSB of $V = 3$. (b) A symmetric HSB of $V = 2$.

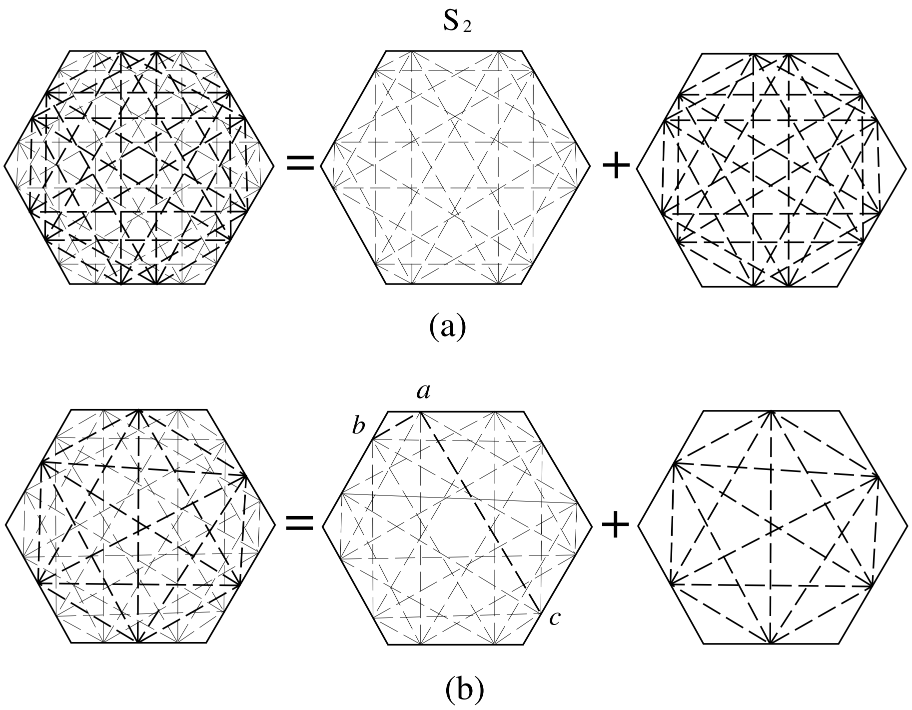

Figure 8: Two symmetric HSBs and their sub-blocks. (a) Decomposition of the symmetric HSB of $V = 4$. (b) Decomposition of the symmetric HSB of $V = 3$.

3.2 Proof of Universality

In this subsection, we prove that the symmetric switch blocks constructed by Algorithm Symmetric_Switch_Block are universal. To show that the symmetric switch blocks are universal, we first prove that the symmetric HSBs of size two are universal.

Lemma 2 *The HSB M_h of size two constructed by Algorithm Symmetric_Switch_Block is universal.*

Proof: By Definition 2, we must prove that $\vec{n}$ is routable on M_h if and only if the following inequalities are simultaneously satisfied:

$$n_{1,2} + n_{1,3} + n_{1,4} + n_{1,5} + n_{1,6} \leq 2 \quad (7)$$
$$n_{1,2} + n_{2,3} + n_{2,4} + n_{2,5} + n_{2,6} \leq 2 \quad (8)$$
$$n_{1,3} + n_{2,3} + n_{3,4} + n_{3,5} + n_{3,6} \leq 2 \quad (9)$$
$$n_{1,4} + n_{2,4} + n_{3,4} + n_{4,5} + n_{4,6} \leq 2 \quad (10)$$
$$n_{1,5} + n_{2,5} + n_{3,5} + n_{4,5} + n_{5,6} \leq 2 \quad (11)$$
$$n_{1,6} + n_{2,6} + n_{3,6} + n_{4,6} + n_{5,6} \leq 2. \quad (12)$$

(If) It is not difficult to identify all of the RRVs satisfying Inequalities (7)–(12). (In fact, there are 2578 such RRVs.) We verify the RRVs and conclude that they can all successfully be routed on the HSB of size two constructed by Algorithm Symmetric_Switch_Block [1]. The reason is that the two terminals, say terminals b and c, that connect to a terminal, say a, do not share any switch (see Figure 8(b)); thus the connections associated with them are non-interacting, except those associated with a.

[1] In fact, based on the work in [10], we need to check only the RRVs in the corresponding *dominating set*. (See [10] for the definition of dominating sets.)

(Only If) For an HSB M_h of size two, the total number of connections routed through each side of M_h cannot exceed two. Hence, if $\vec{n}$ is routable on M_h, the six inequalities must be satisfied. ∎

Let U_V denote the set of RRVs which satisfy the dimension constraint for an HSB of size V. For three RRVs $\vec{u}$, $\vec{v}$, and $\vec{x}$, we say $\vec{u}$ to be a *sub-RRV* of $\vec{v}$ if there exists a $\vec{x}$ such that $\vec{v} = \vec{u} + \vec{x}$. Let $V_1, V_2 \in Z^+$, $\vec{n_i}$ be a sub-RRV of $\vec{n}$,

$$\begin{aligned} \Omega &= \{\vec{n} | \vec{n} \in U_{V_1+V_2}\}, \\ \Omega' &= \{\vec{n} | \vec{n} = \vec{n_1} + \vec{n_2}, \vec{n_1} \in U_{V_1} \text{ and } \vec{n_2} \in U_{V_2}\}. \end{aligned}$$

We have the following Lemma.

Lemma 3 *(RRV Decomposition Property) $\Omega = \Omega'$ if V_1 or V_2 is even.*

Two sub-blocks are said to be *independent* if they do not share any terminals. By Lemma 3, independent switch sub-blocks can be considered individually and merged to form a larger switch block, and the routable RRVs for the merged switch block are identical to those by applying vector addition operations on the routable RRVs for the independent switch sub-blocks. With the decomposition properties of symmetric switch blocks and RRVs, we can prove the following theorem.

Theorem 3 *The symmetric switch blocks are universal.*

Proof: By Definition 2, we shall show that, for an HSB M_h of size V constructed by Algorithm Symmetric_Switch_Block, $\vec{n}$ is routable on M_h if and only if the following inequalities are simultaneously satisfied:

$$\begin{aligned} n_{1,2} + n_{1,3} + n_{1,4} + n_{1,5} + n_{1,6} &\leq V \\ n_{1,2} + n_{2,3} + n_{2,4} + n_{2,5} + n_{2,6} &\leq V \\ n_{1,3} + n_{2,3} + n_{3,4} + n_{3,5} + n_{3,6} &\leq V \\ n_{1,4} + n_{2,4} + n_{3,4} + n_{4,5} + n_{4,6} &\leq V \\ n_{1,5} + n_{2,5} + n_{3,5} + n_{4,5} + n_{5,6} &\leq V \\ n_{1,6} + n_{2,6} + n_{3,6} + n_{4,6} + n_{5,6} &\leq V. \end{aligned}$$

For the HSBs constructed by the algorithm, we have the following key observations (see Figure 8). For an HSB of an even V, we can partition it into $V/2$ non-interacting sub-blocks (shown in Figure 8(a)); each sub-block has the same topology as that of S_2 shown in Figure 8(a). For an HSB of an odd V, we can partition it into $\lceil V/2 \rceil$ non-interacting sub-blocks, with each of the $\lfloor V/2 \rfloor$ sub-blocks identical to S_2 and one sub-block with a clique topology formed by the six terminals from the middle of each side (see Figure 8(b)). Because terminals in different sub-blocks are non-interacting, each sub-block can be considered independently (Lemma 3). Therefore, each symmetric HSB consists of $\lfloor V/2 \rfloor$ independent universal switch sub-blocks of size two, and additional one of size one if V is odd. Further, by Lemma 2, an HSB of size two constructed by Algorithm Symmetric_Switch_Block is universal.

(If) For an *even* V, by Lemma 3, we can decompose a vector $\vec{n} = (n_{1,2}, n_{1,3}, \ldots, n_{1,6}, n_{2,3}, \ldots, n_{2,6}, n_{3,4}, \ldots, n_{3,6}, n_{4,5}, n_{4,6}, n_{5,6})$ into $V/2$ sub-RRVs $\vec{n_i} = (n_{i,(1,2)}, n_{i,(1,3)}, \ldots, n_{i,(1,6)}, n_{i,(2,3)}, \ldots, n_{i,(2,6)}, n_{i,(3,4)}, \ldots, n_{i,(3,6)}, n_{i,(4,5)}, n_{i,(4,6)}, n_{i,(5,6)})$, where $i = 1, 2, \ldots, V/2$, such that each sub-RRV satisfies the following set of inequalities:

$$n_{i,(1,2)} + n_{i,(1,3)} + n_{i,(1,4)} + n_{i,(1,5)} + n_{i,(1,6)} \leq 2 \tag{13}$$
$$n_{i,(1,2)} + n_{i,(2,3)} + n_{i,(2,4)} + n_{i,(2,5)} + n_{i,(2,6)} \leq 2 \tag{14}$$
$$n_{i,(1,3)} + n_{i,(2,3)} + n_{i,(3,4)} + n_{i,(3,5)} + n_{i,(3,6)} \leq 2 \tag{15}$$
$$n_{i,(1,4)} + n_{i,(2,4)} + n_{i,(3,4)} + n_{i,(4,5)} + n_{i,(4,6)} \leq 2 \tag{16}$$
$$n_{i,(1,5)} + n_{i,(2,5)} + n_{i,(3,5)} + n_{i,(4,5)} + n_{i,(5,6)} \leq 2 \tag{17}$$
$$n_{i,(1,6)} + n_{i,(2,6)} + n_{i,(3,6)} + n_{i,(4,6)} + n_{i,(5,6)} \leq 2, \tag{18}$$

where $\vec{n} = \sum_{i=1}^{V/2} \vec{n_i}$. By Lemma 2, each RRV $\vec{n_i}$ satisfying Inequalities (13)–(18) must be routable on the HSB of size two, and by Lemma 3, $\vec{n}$ is also routable on the symmetric HSB of size V.

For an *odd* V, by Lemma 3, we can decompose a vector $\vec{n}$ into $\lceil V/2 \rceil$ sub-RRVs $\vec{n_i}$'s, where $i = 1, 2, \ldots, \lceil V/2 \rceil$, such that each of the sub-RRVs $\vec{n_i}, i = 1, 2, \ldots, \lfloor V/2 \rfloor$ satisfies the set of Inequalities (13)–(18), and the remaining one $\vec{n}_{\lceil V/2 \rceil}$ satisfies the following set of inequalities:

$$n_{\lceil V/2\rceil,(1,2)} + n_{\lceil V/2\rceil,(1,3)} + n_{\lceil V/2\rceil,(1,4)} + n_{\lceil V/2\rceil,(1,5)} + n_{\lceil V/2\rceil,(1,6)} \leq 1 \tag{19}$$
$$n_{\lceil V/2\rceil,(1,2)} + n_{\lceil V/2\rceil,(2,3)} + n_{\lceil V/2\rceil,(2,4)} + n_{\lceil V/2\rceil,(2,5)} + n_{\lceil V/2\rceil,(2,6)} \leq 1 \tag{20}$$
$$n_{\lceil V/2\rceil,(1,3)} + n_{\lceil V/2\rceil,(2,3)} + n_{\lceil V/2\rceil,(3,4)} + n_{\lceil V/2\rceil,(3,5)} + n_{\lceil V/2\rceil,(3,6)} \leq 1 \tag{21}$$
$$n_{\lceil V/2\rceil,(1,4)} + n_{\lceil V/2\rceil,(2,4)} + n_{\lceil V/2\rceil,(3,4)} + n_{\lceil V/2\rceil,(4,5)} + n_{\lceil V/2\rceil,(4,6)} \leq 1 \tag{22}$$
$$n_{\lceil V/2\rceil,(1,5)} + n_{\lceil V/2\rceil,(2,5)} + n_{\lceil V/2\rceil,(3,5)} + n_{\lceil V/2\rceil,(4,5)} + n_{\lceil V/2\rceil,(5,6)} \leq 1 \tag{23}$$
$$n_{\lceil V/2\rceil,(1,6)} + n_{\lceil V/2\rceil,(2,6)} + n_{\lceil V/2\rceil,(3,6)} + n_{\lceil V/2\rceil,(4,6)} + n_{\lceil V/2\rceil,(5,6)} \leq 1. \tag{24}$$

We have $\vec{n} = \sum_{i=1}^{\lceil V/2 \rceil} \vec{n_i}$. By Lemma 2, each RRV $\vec{n_i}$ satisfying the set of Inequalities (13)–(18) must be routable on the symmetric HSB of size two. Further, the last RRV is also routable on an HSB of size one (a clique of six terminals). Hence, by Lemma 3, $\vec{n}$ is also routable on the symmetric HSB of size V.

(Only If) For an HSB M_h of size V, the total number of connections routed through each side of M_h cannot exceed V. Hence, if $\vec{n}$ is routable on M_h, Inequalities (1)–(6) must be satisfied. ∎

Theorem 4 *No HSBs with less than* $15V$ *switches can be universal.*

Proof: By Definition 2, an RRV with only one non-zero component V such as $(V, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0)$, $(0, V, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0)$, …, $(0, V, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, V)$ is routable on a universal HSB. Hence it needs at least V non-interacting switches for each type of connections to construct a universal HSB. Since there are 15 types of connections in an HSB, the smallest number of switches needed to construct a universal HSB is $15V$. ∎

As mentioned in Subsection 3.1, the total number of switches used in a 6-sided symmetric switch block is $15V$. Thus, the symmetric HSBs are the "cheapest" universal ones, i.e., it uses the minimum number of switches to construct a universal switch block. Note that the $15V$ switches requirement is quite small, compared to a fully connected HSB which has $15V^2$ switches.

By Theorem 1, any two isomorphic switch blocks have the same routing capacity. Hence, we have following lemma.

Lemma 4 *For any two isomorphic switch blocks* $M_h(T, S)$ *and* $M'_h(T', S')$*,* $M_h(T, S)$ *is universal if and only if* $M'_h(T', S')$ *is universal.*

By Lemma 4, we can obtain a whole class of universal switch blocks by performing isomorphism operations on a symmetric switch block.

4 Clique-Based Switch Blocks

In this section, we consider the clique-based HSBs associated with those used in the Xilinx XC4000-series FPGAs (see Figure 9(a)) and show that the clique-based HSBs are not universal.

Figures 9(a) and (b) show two clique-based switch blocks of four and six sides, respectively (Note that the switch block shown in Figure 9(a) is used in Xilinx XC4000-series FPGAs.). Nevertheless, as shown in Figure 5(c), the clique-based HSB is not universal since the RRV $(0, 0, 0, 0, 0, 1, 1, 0, 0, 1, 0, 0, 0, 0, 0)$ which satisfies the dimension constraint is not routable on the 6-sided clique-based switch block of size two. For the feasibility condition of the 6-sided clique-based switch blocks, we have the following lemma.

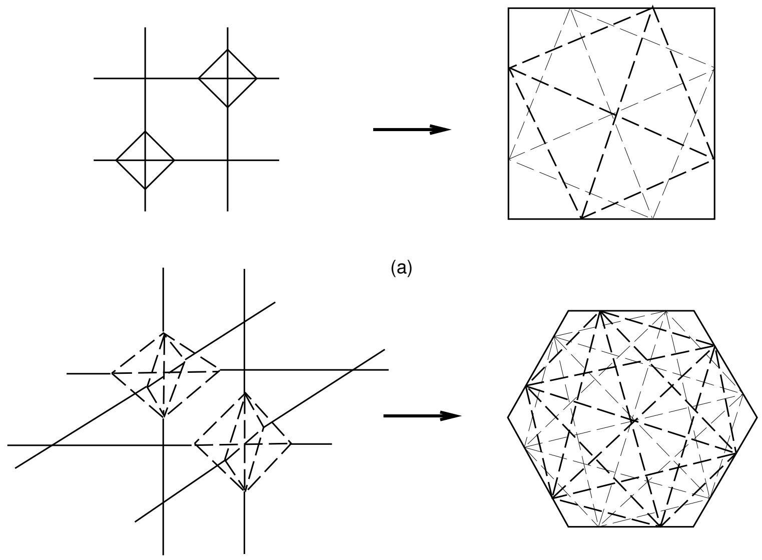

Figure 9: Clique-based switch blocks. (a) A 4-sided one. (b) A 6-sided one.

Lemma 5 *For a clique-based HSB $M_h(S_h, T_h)$ of size V, $\vec{n}$ is routable on M_h only if the following set of inequalities are simultaneously satisfied:*

$$n_{1,2} + n_{1,3} + n_{1,4} + n_{1,5} + n_{1,6} \leq V \tag{25}$$

$$n_{1,2} + n_{2,3} + n_{2,4} + n_{2,5} + n_{2,6} \leq V \tag{26}$$

$$n_{1,3} + n_{2,3} + n_{3,4} + n_{3,5} + n_{3,6} \leq V \tag{27}$$

$$n_{1,4} + n_{2,4} + n_{3,4} + n_{4,5} + n_{4,6} \leq V \tag{28}$$

$$n_{1,5} + n_{2,5} + n_{3,5} + n_{4,5} + n_{5,6} \leq V \tag{29}$$

$$n_{1,6} + n_{2,6} + n_{3,6} + n_{4,6} + n_{5,6} \leq V \tag{30}$$

$$n_{p,q} + n_{q,r} + n_{r,p} \leq V, \; p, q, r = 1, 2, \ldots 6, p \neq q, q \neq r, \; and \; p \neq r. \tag{31}$$

Proof: It is obvious that if an RRV is routable (on the clique-based HSB M_h), it must satisfy the dimension constraint Inequalities (25)–(30). For a clique-based HSB M_h of size V, we have the following key observation. Consider three arbitrary sides p, q, and r of M_h. The switches incident on p, q, r form V triangles, and these triangles are non-interacting and thus can be considered independently. (See Figure 9(b).) Since a triangle can be routed by at most one connection, the total number of connections that can route on p, q, r cannot exceed V. Thus the set of Inequalities (31) is also a necessary condition. ∎

Theorem 5 *The clique-based HSBs are not universal.*

Let $U_h(V)$ ($C_h(V)$) be the set of RRVs which satisfy the dimension constraint for the universal (clique-based) HSBs of size V. Let $|U_h(V)|$ ($|C_h(V)|$) be the cardinality of $U_h(V)$ ($C_h(V)$). We have the following theorem.

Theorem 6 $|C_h(V)| \subset |U_h(V)|$.

5 Experimental Results

To explore the effects of switch-block architectures on routing on a 3D FPGA, we implemented a maze router in the C language and ran on a SUN Ultra workstation. We tested the area performance of the router based

Circuit	#Logic blocks	#Con.	Number of tracks needed for detailed-routing completion					
			Original Order		Shortest net first		Longest net first	
			Symmetric	Clique	Sym.	Cliq.	Sym.	Cliq.
BUSC	$13 \times 12 \times 2$	392	7	9	7	7	8	8
DMA	$18 \times 16 \times 2$	771	9	9	8	8	10	10
BNRE	$22 \times 21 \times 2$	1257	9	9	8	9	10	10
DFSM	$23 \times 22 \times 2$	1422	9	9	8	8	9	9
Z03	$27 \times 26 \times 2$	2135	9	10	8	9	10	10
9symml	$11 \times 10 \times 2$	259	6	6	6	7	7	8
alu2	$15 \times 13 \times 2$	511	7	7	7	8	8	9
alu4	$19 \times 17 \times 2$	851	8	9	9	9	10	11
apex7	$12 \times 10 \times 2$	300	6	7	6	7	8	8
example2	$14 \times 12 \times 2$	444	8	8	8	8	9	10
k2	$22 \times 20 \times 2$	1256	11	11	10	11	12	12
term1	$10 \times 9 \times 2$	202	7	8	6	6	7	8
too_large	$15 \times 14 \times 2$	519	7	9	8	8	9	9
vda	$17 \times 16 \times 2$	722	7	9	8	9	9	10
Total	-	-	109	118	106	112	125	131
Comparison	-	-	1.00	1.08	1.00	1.06	1.00	1.05

Table 1: Minimum numbers of tracks needed for detailed-routing completion.

on the CGE [8] and the SEGA [7] benchmark circuits. A logic-block pin was connected to any of the W tracks in the adjacent routing channel. We routed these circuits on a two-layer 3D FPGA and randomly assigned the layer for each terminal of a net. The switch-block architectures used were the symmetric switch blocks and clique-based (Xilinx XC4000-like) switch blocks.

The quality of a switch block was evaluated by the area performance of the detailed router. Table 1 shows the results. For the results listed in this table, we determined the minimum number of tracks W required for 100% routing completion for each circuit, using the two kinds of switch blocks. Because net ordering often affects the performance of a maze router, we routed the benchmark circuits by using the following three net-ordering schemes to avoid possible biases: (1) net order as given in the original benchmark circuits, (2) shortest net first (non-decreasing order of net lengths), and (3) longest net first (non-increasing order of net lengths). Our results show that, between the two kinds of switch blocks, the symmetric switch blocks usually needed the minimum W's for 100% routing completion, no matter what net order was used. The results show that our symmetric switch blocks improve the routability at the chip level. (An average of 6% improvement in the area performance was achieved.)

We also performed experiments to explore the effects of net density on the area performance of switch blocks. We randomly generated connections on a $15 \times 15 \times 3$ (number of logic blocks in the three layers) 3D FPGA. For this purpose, we assume that the number of pins on each logic blocks is unlimited (so that we could test denser circuits). As shown in Figure 10, no matter how dense the circuit is (numbers of connections ranging from 400 to 1600), the symmetric switch blocks consistently outperform the clique-based switch blocks. (An average of 10% improvement in the area performance was achieved.)

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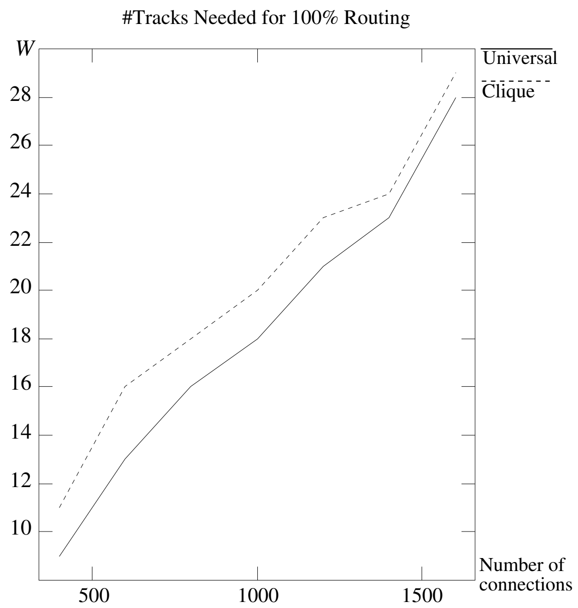

Figure 10: Comparison of the area performance by using the symmetric switch blocks and clique-based switch blocks for different numbers of connections on a $15 \times 15 \times 3$ 3D-FPGA.

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