Chap. 4 Basic MOS Device Physics

Textbook Chapter 2

2.1 General Considerations
2.2 MOS I/V Characteristics
2.3 Second-Order Effects
2.4 MOS Device Models
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I/V Characteristics: Saturation/Triode

\[ V_{DS} \geq V_{GS} - V_{TH} \]

\[ I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \]

\[ V_{DS} < V_{GS} - V_{TH} \]

\[ I_D = \mu_n C_{ox} \frac{W}{L} [(V_{GS} - V_{TH}) \cdot V_{DS} - \frac{V_{DS}^2}{2}] \]
Small-Signal Model

\[
g_m = \frac{\partial I_D}{\partial V_{GS}} \bigg|_{V_{DS}=\text{constant}} = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})
\]

\[
= \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = \frac{2I_D}{V_{GS} - V_{TH}}
\]
Body effect

\[ V_{TH} = V_{TH0} + \gamma \left( \sqrt{-2\phi_F + V_{SB}} - \sqrt{-2\phi_F} \right) \]

where \( \gamma = \sqrt{2q\varepsilon_{Si}N_{sub}} / C_{ox} \)

denotes the body effect coefficient. (0.3 ~ 0.4V^{1/2} )

\( \phi_F = -(kT / q)\ln(N_{sub} / n_i) \) surface potential, \( q \) is electron charge, \( N_{sub} \) is the doping concentration of the substrate, \( n_i = 1.45 \times 10^{10} cm^{-3} \)
Second-Order Effects (cont’d)

Channel-length modulation

\[ I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L'} (V_{GS} - V_{TH})^2 \]

where

- \( L' \) is a function of \( V_{DS} \).
- Writing \( L' = L - \Delta L \),
- i.e., \( 1/L' \approx (1 + \Delta L / L) / L \),
- and assuming \( \Delta L / L = \lambda V_{DS} \).

\[ I_D \approx \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS}) \]

\( \lambda \) : the channel-length modulation coefficient
MOS Device Capacitances

(1) Oxide capacitance between the gate and the channel, \( C_1 = WLC_{ox} \).

(2) Depletion capacitance between the channel and the substrate, \( C_2 = WL\sqrt{\frac{q\varepsilon_{Si}N_{sub}}{4\phi_F}}} \).

(3) Capacitance due to the overlap of the gate poly with the source and drain areas, \( C_3 \) and \( C_4 \).

(4) The overlap capacitance per unit width is denoted by \( C_{ov} \).

(5) Junction capacitance between the source/drain areas and the substrate.
   a. bottom-plate capacitance associated with the bottom of the junction, \( C_j = C_{jo} / [1+V_R/\phi_B]^m \).
   b. sidewall capacitance due to the perimeter of the junction, \( C_{jSW} \). (note \( C_j : \text{F/m}^2, C_{jSW} : \text{F/m} \))
MOS Device Capacitances (cont’d)

(a)

\[ C_{DB} = C_{SB} \equiv AX \cdot C_j + PX \cdot C_{jsw}, \quad X=S \text{ or } D \]

\[ C_{DB} = C_{SB} = WE \cdot C_j + 2(W + E) \cdot C_{jsw} \]

(b)

\[ C_{DB} = \frac{W}{2} E \cdot C_j + 2\left(\frac{W}{2} + E\right) \cdot C_{jsw} \]

\[ C_{SB} = 2C_{DB} = WE \cdot C_j + 2(W + 2E) \cdot C_{jsw} \]

➢ In fact, the capacitance of the sidewall facing the channel may be less than that of the other three sidewalls because of the channel-stop implant.
MOS Device Capacitances (cont’d)

- Variation of $C_{GS}$ and $C_{GD}$ versus $V_{GS}$
MOS small-signal model

- Basic MOS small-signal model
  \[ g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) \]

- Channel-length modulation represented by a dependent current source

- Channel-length modulation represented by an output resistor
  \[ r_o = \frac{\partial V_{DS}}{\partial I_D} \approx \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \cdot \lambda \approx \frac{1}{I_D} \]
  where
  \[ I_D \approx \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS}) \]
Body effect represented by a dependent current source

In the saturation region, $g_{mb}$ can be expressed as

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = \frac{\partial I_D}{\partial V_{TH}} \frac{\partial V_{TH}}{\partial V_{BS}} = \mu_n C_{ox} \frac{W}{L} \left( V_{GS} - V_{TH} \right) \left( -\frac{\partial V_{TH}}{\partial V_{BS}} \right)$$

$$\therefore V_{TH} = V_{TH0} + \gamma \left( \sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|} \right)$$

$$\frac{\partial V_{TH}}{\partial V_{BS}} = \frac{\partial V_{TH}}{\partial V_{SB}} = -\frac{\gamma}{2} \left( | -2\phi_F + V_{SB} | \right)^{-1/2}$$

$$\Rightarrow$$

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = g_m \cdot \frac{\gamma}{2\sqrt{|-2\phi_F + V_{SB}|}} = \eta g_m$$
MOS small-signal model (cont’d)
FinFETs

- FinFETs have three-dimensional geometry and exhibit superior performance as channel lengths fall below ~20 nm.
- Here, $W = W_F + 2H_F$, but since $H_F$ is not under the circuit designer’s control and $W_F$ impacts device imperfections, there are only discrete values for transistor width.
• Spacing between fins, $S_F$, also plays a significant role in performance and is typically fixed.
• Due to small dimensions of the intrinsic FinFET, the gate and S/D contacts must be placed away from the core of the device.