Chapter 10: Bandgap References

Textbook Chapter 12

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Supply-Independent Biasing

\[ V_{GS1} = V_{GS2} + I_{D2}R_S \]

\[ \Rightarrow \left( \sqrt{\frac{2I_{REF}}{\mu_n C_{ox}(W/L)_N}} + V_{TH1} \right) I_{REF} = I_{out} \]

\[ = \sqrt{\frac{2I_{out}}{\mu_n C_{ox}K(W/L)_N}} + V_{TH2} + I_{out}R_S \]

\[ \Rightarrow \sqrt{\frac{2I_{out}}{\mu_n C_{ox}(W/L)_N}} \left( 1 - \frac{1}{\sqrt{K}} \right) = I_{out}R_S \]

\[ \Rightarrow I_{out} = \frac{2}{\mu_n C_{ox}(W/L)_N} \cdot \frac{1}{R_S^2} \left( 1 - \frac{1}{\sqrt{K}} \right)^2 \]

The current is independent of the supply voltage, but still a function of process and temperature. M2 has the body effect.

\[ g_m \propto \sqrt{I_{out}} \propto \frac{1}{R_S} \]
Supply-Independent Biasing

• The “start-up” problem

- In Fig. (a), diode-connected device $M_5$ provides a current path from $V_{DD}$ through $M_3$ and $M_1$ to ground upon start-up
- $M_3$ and $M_1$, and hence $M_2$ and $M_4$, cannot remain off
- This technique is practical only if $V_{TH1} + V_{TH5} + |V_{TH3}| < V_{DD}$ and $V_{GS1} + V_{TH5} + |V_{GS3}| > V_{DD}$ to ensure $M_5$ remains off after start-up
The base-emitter voltage of bipolar transistors, or the forward voltage of a \textit{pn}-junction diode exhibits a negative temperature coefficient (TC)

For a bipolar device,

\[ I_C = I_S \exp \left( \frac{V_{BE}}{V_T} \right) \Rightarrow V_{BE} = V_T \ln \left( \frac{I_C}{I_S} \right) \]

\[ V_T = kT / q \]

Saturation current \( I_S \)

\[ I_S \propto \mu kT \left[ n_i^2 \right] \propto \mu_0 T^m \cdot kT \left[ T^3 \exp \left( -\frac{E_g}{kT} \right) \right] \]

\[ \Rightarrow I_S = b T^{4+m} \exp \left( -\frac{E_g}{kT} \right) \]

where \( \mu \) denotes the mobility of minority carriers and \( n_i \) is the intrinsic carrier concentration of silicon

The temperature dependence of these quantities is expressed as \( \mu \propto \mu_0 T^m \), where \( m \approx -3/2 \), and \( n_i^2 \propto T^3 \exp[-E_g/(kT)] \), where \( E_g \approx 1.12 \text{ eV} \) is the bandgap energy of silicon and \( b \) is proportionality factor
Negative-TC Voltage

\[ \frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T} \ln \frac{I_C}{I_S} + V_T \cdot \frac{\partial}{\partial T} \left( \ln \frac{I_C}{I_S} \right) = \frac{V_{BE} - (4 + m)V_T - E_g/q}{T} \]

\[ = \frac{0.75 - (4 - 3/2) \times 26mV - 1.12V}{300^\circ K} = -1.5mV /^\circ K \]

- The base-emitter voltage exhibits a negative TC.

- The base-emitter voltage difference exhibits a positive TC.

\[ \Delta V_{BE} = V_{BE1} - V_{BE2} = V_T \ln \frac{I_{C1}}{I_{S1}} - V_T \ln \frac{I_{C2}}{I_{S2}} \]

\[ = V_T \ln(n) = \frac{kT}{q} \ln(n) \Rightarrow \frac{\partial \Delta V_{BE}}{\partial T} = \frac{k}{q} \ln(n) \]
\[ V_{\text{REF}} = \alpha_1 V_{BE} + \alpha_2 V_T \ln(n) \]

\[ \frac{\partial V_{BE}}{\partial T} = -1.5 \text{mV} / K \quad \text{and} \quad \frac{\partial V_T}{\partial T} \approx +0.087 \text{mV} / K \]

- At room temperature, we set \( \alpha_1 = 1 \) and

\[ V_{\text{REF}} = \alpha_1 V_{BE} + \alpha_2 V_T \ln(n) \]

\[ 1.5 \text{mV} / K = \alpha_2 \ln(n) \cdot 0.087 \text{mV} / K \Rightarrow \alpha_2 \ln(n) \approx 17.2 \]

- A reference voltage with zero TC is achieved.
- Need to devise a circuit that adds \( V_{BE} \) to \( 17.2V_T \)
\[ V_{BE1} - V_{BE2} = V_T \ln n, \] arriving at a current of \( V_T \ln n/R_3 \) through the right branch and an output voltage of

\[
V_{out} = V_{REF} = V_{BE2} + V_T \ln(n) \times \left(1 + \frac{R_2}{R_3}\right)
\]

\[
= 800mV + (26mV \times \ln(31))(1 + 4) \approx 1.25V
\]

- For a zero TC, we must have \((1 + R_2/R_3)\ln n \approx 17.2\), for example \( n = 31 \) and \( R_2/R_3 = 4 \)
(1) **Collector Current Variation:**

- $I_{C1}$ and $I_{C2}$ are not constant
- Assume $I_{C1} = I_{C2} \approx (V_T \ln n)/R_3$

\[
\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T} \ln \frac{I_C}{I_S} + V_T \cdot \left( \frac{1}{I_C} \frac{\partial I_C}{\partial T} - \frac{1}{I_C} \frac{\partial I_S}{\partial T} \right)
\]

\[
\therefore \frac{\partial I_C}{\partial T} \approx V_T \ln(n) / (R_3T) = \frac{I_C}{T}
\]

\[
\Rightarrow \frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (3+m)V_T - E_g/q}{T} > -1.5mV/°K
\]

(2) **Compatibility with CMOS Technology:**

- In n-well processes, a pnp transistor can be formed.
Bandgap Reference: Issues

(3) Op-Amp Offset and Output Impedance:

- Op amps suffer from input “offset”
- This effect is quantified as

\[
V_{BE1} - V_{OS} = V_{BE2} + R_3 I_{C2}
\]

\[
V_{out} = V_{BE2} + (R_2 + R_3) \cdot \frac{V_{BE1} - V_{BE2} - V_{OS}}{R_3}
= V_{BE2} + \left(V_T \ln(n) - V_{OS}\right) \cdot \left(1 + \frac{R_2}{R_3}\right)
\]

- \(V_{OS}\) is amplified by \(1+R_2/R_3\), introducing error in \(V_{out}\)
(3) **Op-Amp Offset and Output Impedance:**

- Several methods employed to lower the effect of $V_{OS}$
- First, op amp with large devices to lower the offset
- Second, the collector currents of $Q_1$ and $Q_2$ can be ratioed by a factor of $m$ such that $\Delta V_{BE} = V_T \ln(mn)$
- Third, each branch may use two $pn$ junctions in series to double $\Delta V_{BE}$

$$V_{out} = V_{EB3} + V_{EB4} + I_2 \cdot (R_2 + R_3) = 2V_{EB} + \left(1 + \frac{R_2}{R_3}\right)\left[2V_T \ln(mn) - V_{OS}\right]$$
(3) **Op-Amp Offset and Output Impedance:**

- To avoid the op amp to drive the resistive loads, we modify the circuit as

![Circuit Diagram]

- Why called “Bandgap Reference”

\[
\frac{\partial V_{REF}}{\partial T} = \frac{\partial V_{BE}}{\partial T} + \frac{\partial V_T}{\partial T} \ln(n) = \frac{\partial V_{BE}}{\partial T} + \frac{k}{q} \ln(n) = 0
\]

\[
\Rightarrow \frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (4 + m)V_T - E_g/q}{T} = -\frac{V_T}{T} \ln(n)
\]

\[
\Rightarrow V_{REF} = V_{BE} + V_T \ln n = V_{BE} + \left\{-\left[V_{BE} - (4 + m)V_T - E_g/q\right]\right\}
\]

\[
= \frac{E_g}{q} + (4 + m)V_T
\]

- The term “bandgap” is used because as \( T \to 0 \), \( V_{REF} \to E_g/q \)
(4) **Feedback Polarity:**

- Negative feedback factor is
  \[ \beta_N = \frac{1/g_{m2} + R_3}{1/g_{m2} + R_2 + R_3} \]

- Positive feedback factor is
  \[ \beta_P = \frac{1/g_{m1}}{1/g_{m1} + R_1} \]

- To ensure an overall negative feedback, \( \beta_P \) must be less than \( \beta_N \), roughly by a factor of two
(5) **Supply Dependence and Start-Up:**

- Circuit may require a start-up mechanism because if $V_X$ and $V_Y$ are equal to zero, the input differential pair of the op amp may turn off.
- Supply rejection of the circuit typically degrades at high frequencies, mandating “supply regulation.”
(6) **Curvature Correction:**

- Bandgap voltages exhibit a finite “curvature”, i.e., their TC is zero at one temperature and positive or negative at others.
- Curvature arises from temperature variation of base-emitter voltages, collector currents, offset voltages.
- Many curvature-correction techniques introduced in bipolar bandgap circuits, but rarely used in CMOS counterparts.
- Samples of CMOS bandgap reference display substantially different zero-TC temperatures due to large offsets and process variations.
PTAT Current Generation

• PTAT currents can be generated as follows
• Assume that $M_1$-$M_2$ and $M_3$-$M_4$ are identical pairs
• For $I_{D1} = I_{D2}$, the circuit must ensure that $V_X = V_Y$
• Thus, $I_{D1} = I_{D2} = (V_T \ln n)/R_1$, yielding the same behavior for $I_{D5}$
PTAT Current Generation

- A modified circuit to provide a bandgap reference voltage is shown below
- Idea is to add a PTAT voltage $I_{D5}R_2$ to a base-emitter voltage; the output therefore equals

$$V_{out} = V_{BE3} + I_{D5} \cdot R_2 = V_{BE3} + \frac{R_2}{R_1} V_T \ln(n)$$

- All PMOS transistors are assumed identical
- The value of $V_{BE3}$ and size of $Q_3$ are somewhat arbitrary so long as their sum gives a zero TC
Speed and Noise Issues

- Reference generators are low-frequency circuits, but can impact speed of circuits they feed.
- Various building blocks experience “crosstalk” through reference lines.
- Caused by finite output impedance of reference generators.
- In the configuration below, voltage at node $N$ is heavily disturbed by circuit fed by $M_5$. 

![Diagram of circuit](image)
Speed and Noise Issues

• For fast changes in $V_N$ the op amp cannot maintain $V_P$ constant and bias currents of $M_5$ and $M_6$ experience large transient changes
• Duration of the transient at node $P$ may be quite long if op amp has a slow response
• Reference generator may require a high-speed op amp
Speed and Noise Issues

• For low-power applications, high-speed op amp may not be feasible

• Alternatively, node $P$ in circuit below can be bypassed to ground by a large capacitor $C_B$ to suppress external disturbances

• For stability of op amp to not degrade with addition of $C_B$, op amp must be of one-stage nature
Speed and Noise Issues

- Output noise of reference generators may impact the performance of low-noise circuits.
- As shown below, the load current source of a CS stage is driven by a bandgap circuit with a current multiplication factor of $N$.
- Thus, noise current of $M_1$ (or $M_2$) is multiplied by the same factor as it appears in $M_3$.
- $M_1$-$M_3$ carry noise due to the op amp $A_1$ as well.
Speed and Noise Issues

• As another example, if a high-precision A/D converter employs a bandgap reference voltage with which the analog input signal is compared, then the noise in the reference is directly added to the input
Speed and Noise Issues

\[ \frac{V_{n,\text{out}}}{R_1 + g_{mN}^{-1}} = -g_{mP} \cdot V_P \implies V_P = \frac{-V_{n,\text{out}}}{g_{mP} (R_1 + g_{mN}^{-1})} \]

\[ V_A = \frac{V_{n,\text{out}}}{g_{mN} (R_1 + g_{mN}^{-1})} \]

\[ V_{n,\text{out}} + V_{n,\text{OP}} - V_A = \frac{V_P}{A_0} \]

\[ \frac{V_{n,\text{out}}}{R_1 + g_{mN}^{-1}} \cdot \frac{1}{g_{mN}} - \frac{V_{n,\text{out}}}{g_{mP} A_0 (R_1 + g_{mN}^{-1})} = V_{n,\text{op}} + V_{n,\text{out}} \]

\[ V_{n,\text{out}} \left[ \frac{1}{R_1 + g_{mN}^{-1}} \left( \frac{1}{g_{mN}} - \frac{1}{g_{mP} A_0} \right) - 1 \right] = V_{n,\text{op}} \]

If \( g_{mP} A_0 \gg g_{mN} \gg R_1^{-1} \) \( \implies \) \( |V_{n,\text{out}}| \approx V_{n,\text{OP}} \)
Low-Voltage Bandgap References

\[ |I_{D4}| = \frac{V_T \ln(n)}{R_1} \]

- Add \( R_2 \) to have a negative TC current to compensate \( I_{D4} \)? Did not work!

- Add \( R_2 \) and \( R_3 \)

\[ I_{C1} + \frac{|V_{BE1}|}{R_3} = I_{C2} + \frac{|V_{BE1}|}{R_2} \]

If \( R_3 = R_2 \) \( \Rightarrow I_{C1} = I_{C2} \)
Low-Voltage Bandgap References

\[ I_{C2} = \frac{|V_{BE1}| - |V_{BE2}|}{R_1} = \frac{V_T \ln(n)}{R_1} \]

\[ |I_{D4}| = I_{C2} + \frac{|V_{BE1}|}{R_2} = \frac{V_T \ln(n)}{R_1} + \frac{|V_{BE1}|}{R_2} \]

\[ \Rightarrow V_{BG} = \frac{R_4}{R_2} [\frac{V_{BE1}}{R_2} + \frac{R_2}{R_1} V_T \ln(n)] \]

- Requiring a minimum \( V_{DD} \) of \( V_{BE1} + |V_{DS3}| \)
- Minimum \( V_{DD} \) of 0.75 V is achievable
Low-Voltage Bandgap References

• The op amp can be realized as a five-transistor OTA
• OTA design guidelines:
  (1) Large transistor dimensions to minimize flicker noise and offset
  (2) $V_{GS}$ of $M_a$ and $M_b$ plus headroom requires by $I_{SS}$ must not exceed $|V_{BE1}|$
  (3) Transistors are chosen long enough to yield reasonable loop gain, e.g., 5 to 10.

• $M_e$ serves as a start-up circuit
Low-Voltage Bandgap References

- Another low-voltage bandgap circuit

\[ |I_{D5}| = \frac{V_{ou}}{R_3} + \frac{V_{out} - |V_{BE3}|}{R_2} \]

\[ |I_{D4}| = |I_{D5}| = \frac{V_T \ln(n)}{R_1} \]

\[ \Rightarrow V_{out} = \frac{R_3}{R_2 + R_3} [|V_{BE3}| + \frac{R_2}{R_1} V_T \ln(n)] \]