Chapter 12. Operational Amplifier Circuits

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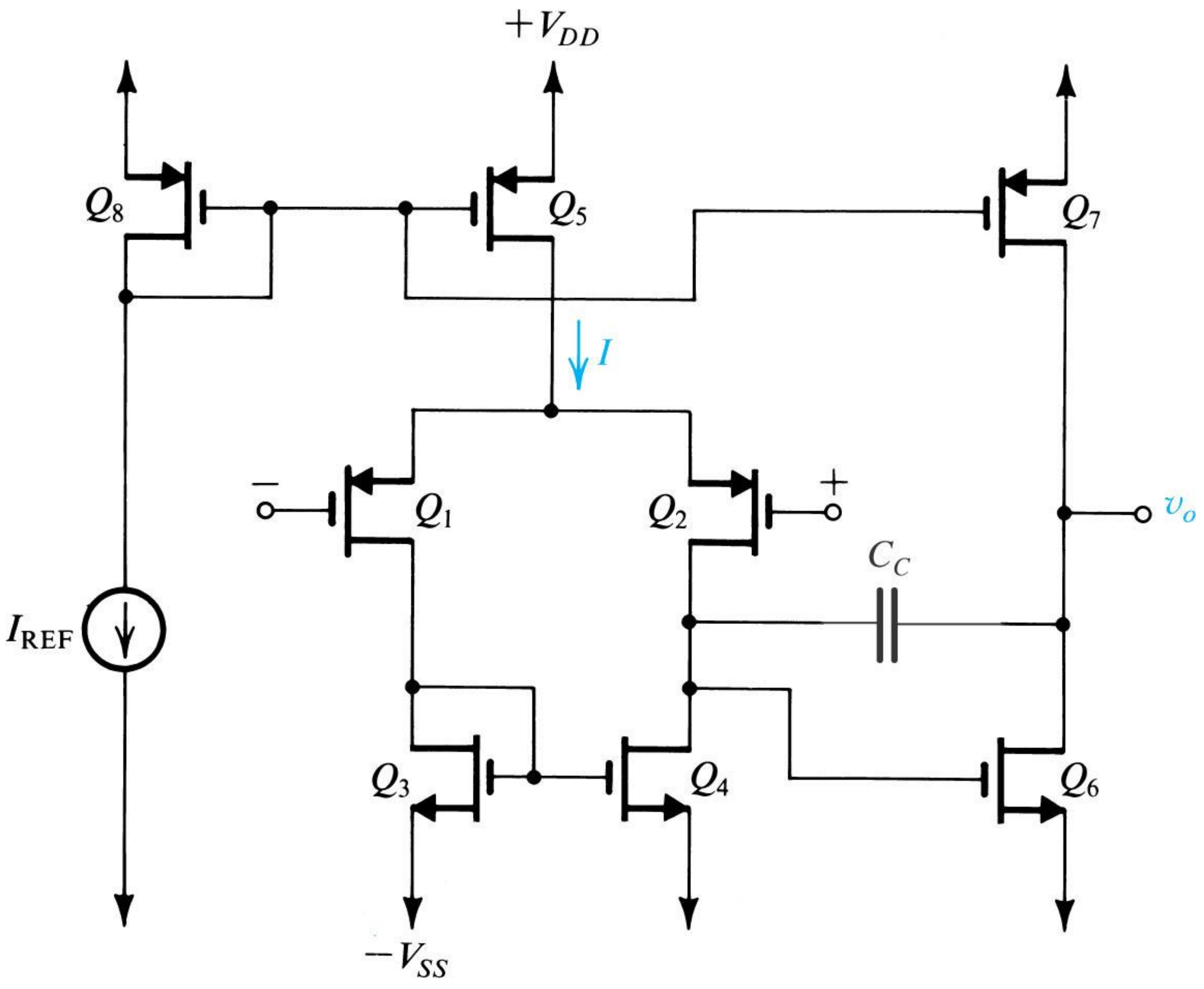
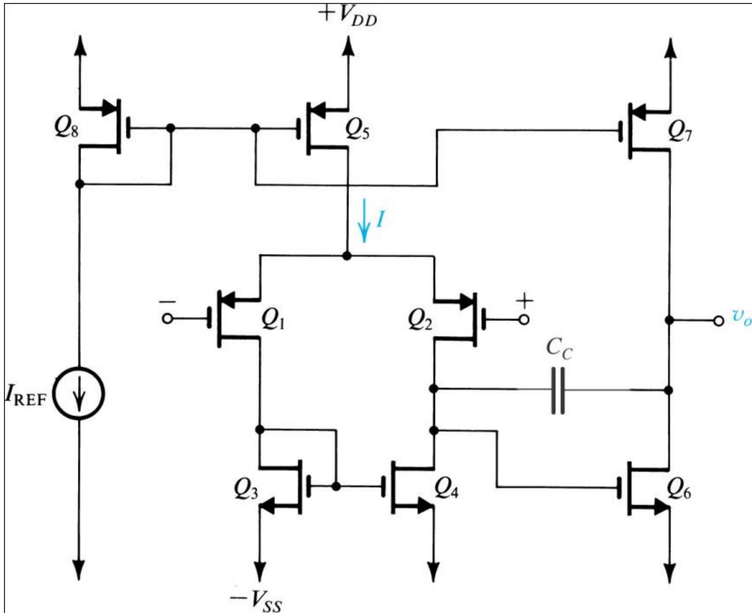
12.1 The Two Stage CMOS Op Amp



12.1.1 The Circuit

Bias generation



1st stage

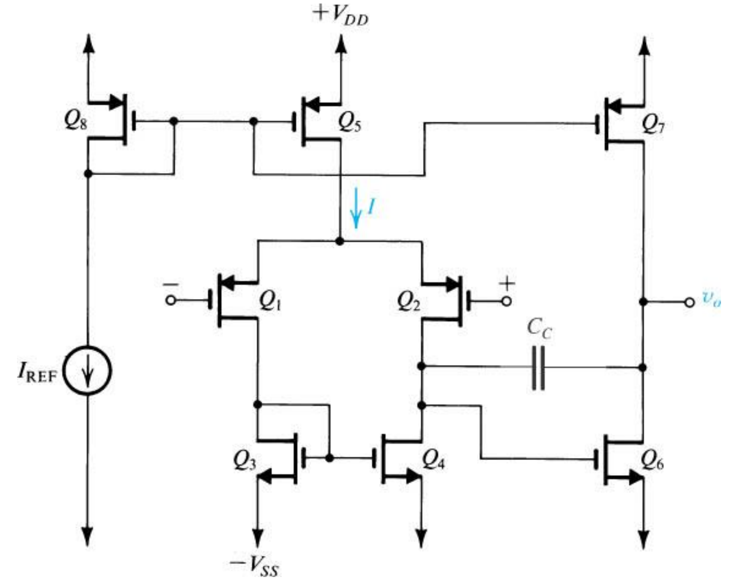
2nd stage

- Voltage gain
  - Voltage gain of 1st stage: $A_1 = -g_{m1}(r_{o2} \parallel r_{o4})$
  - Voltage gain of 2nd stage: $A_2 = -g_{m6}(r_{o6} \parallel r_{o7})$
  - DC open-loop gain: $A_v = A_1 \times A_2$
- Input offset voltage
  - *Random offset*: device mismatches as random in nature
  - Systematic offset: due to design technique ⇨ predictable

⇨ $$\frac{(W/L)_6}{(W/L)_4} = 2\frac{(W/L)_7}{(W/L)_5}$$ If this condition is not met, a systematic offset will result.

- C_C is Miller-multiplied by the gain of the second stage to provide the required dominant pole.

12.1.2 Input Common-Mode Range



- To keep Q_1 and Q_2 in saturation.

$$V_{ICM} \geq -V_{SS} + V_{tn} + V_{OV3} - |V_{tp}|$$

- The highest value of V_{ICM} ensures Q_5 in saturation.

$$V_{ICM} \leq V_{DD} - |V_{OV5}| - V_{SG1}$$

$$\Rightarrow V_{ICM} \leq V_{DD} - |V_{OV5}| - |V_{tp}| - |V_{OV1}|$$

$$\Rightarrow -V_{SS} + V_{OV3} + V_{tn} - |V_{tp}| \leq V_{ICM} \leq V_{DD} - |V_{tp}| - |V_{OV1}| - |V_{OV5}|$$

From the point view of V_{ICM}, select the values of V_{OV} as low as possible!!

Output swing

to keep Q_6 and Q_7 saturated

$$\Rightarrow -V_{SS} + V_{OV6} \leq v_O \leq V_{DD} - |V_{OV7}|$$

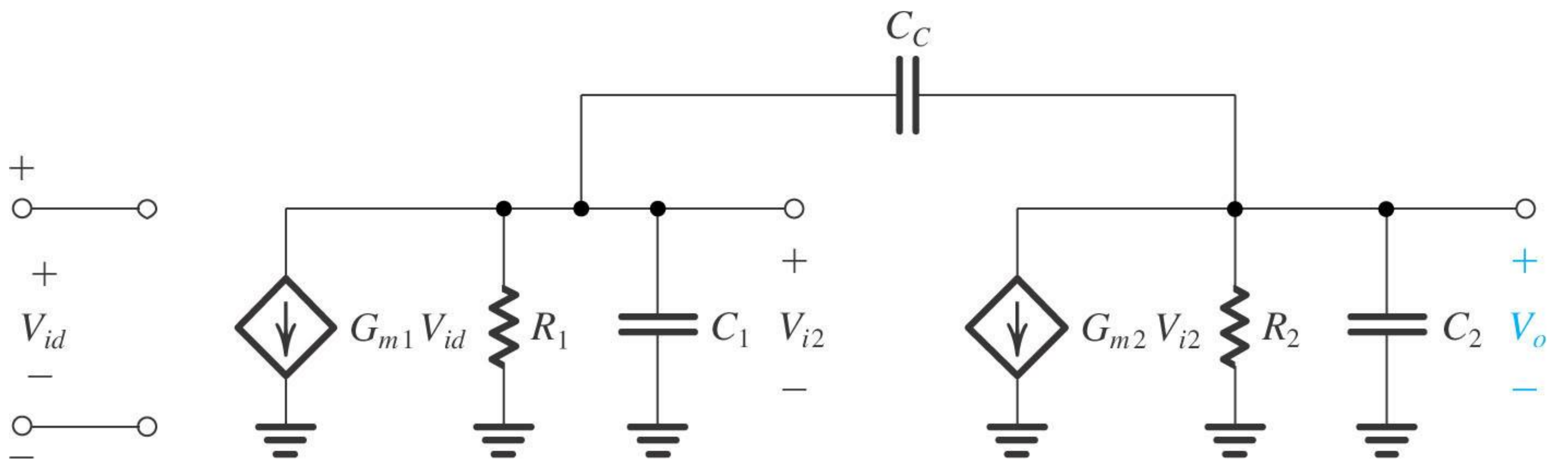
Select the values of V_{OV} (of Q_6 and Q_7) as low as possible!!

But $f_T \propto V_{OV}$; the high-frequency performance improved with the higher overdrive voltage.

- A substantial allowable range of V_{ICM} and v_O needed for an unity-gain application.

12.1.3 Voltage Gain

Simplified small-signal equivalent circuit



- $R_{in} = \infty$
- $G_{m1} = g_{m1} = g_{m2}$ ⇨ $G_{m1} = \dfrac{2(I/2)}{V_{OV1}} = \dfrac{I}{V_{OV1}}$
- $R_1 = r_{o2} \,\|\, r_{o4}$ $\quad r_{o2} = \dfrac{|V_{A2}|}{I/2} \quad r_{o4} = \dfrac{V_{A4}}{I/2}$
- Dc gain of 1st stage

$$A_1 = -G_{m1}R_1 = -g_{m1}\left(r_{o2} \| r_{o4}\right) = -\frac{2}{V_{OV1}\left(\dfrac{1}{|V_{A2}|} + \dfrac{1}{V_{A4}}\right)}$$

A_1 is increased by

❶ Q_1 and Q_2 with a low overdrive

❷ Choosing a longer channel length to obtain larger Early voltage, $|V_A|$.

Both, however, degrade the frequency response of the amplifier.

- $G_{m2} = g_{m6} = \dfrac{2I_{D6}}{V_{OV6}}$
- $R_2 = r_{o6} \parallel r_{o7}$ $\quad r_{o6} = \dfrac{V_{A6}}{I_{D6}} \quad r_{o7} = \dfrac{|V_{A7}|}{I_{D7}} = \dfrac{|V_{A7}|}{I_{D6}}$
- Dc gain of 2nd stage

$$A_2 = -G_{m2}R_2 = -g_{m6}\left(r_{o6} \| r_{o7}\right) = -\frac{2}{V_{OV6}\left(\dfrac{1}{V_{A6}} + \dfrac{1}{|V_{A7}|}\right)}$$

- Overall dc gain

$$A_v = A_1 A_2 = G_{m1}R_1 G_{m2}R_2 = g_{m1}\left(r_{02} \| r_{o4}\right) g_{m6}\left(r_{06} \| r_{o7}\right)$$

Generally, 500 ~5000 V/V of $A_{v,\max}$.

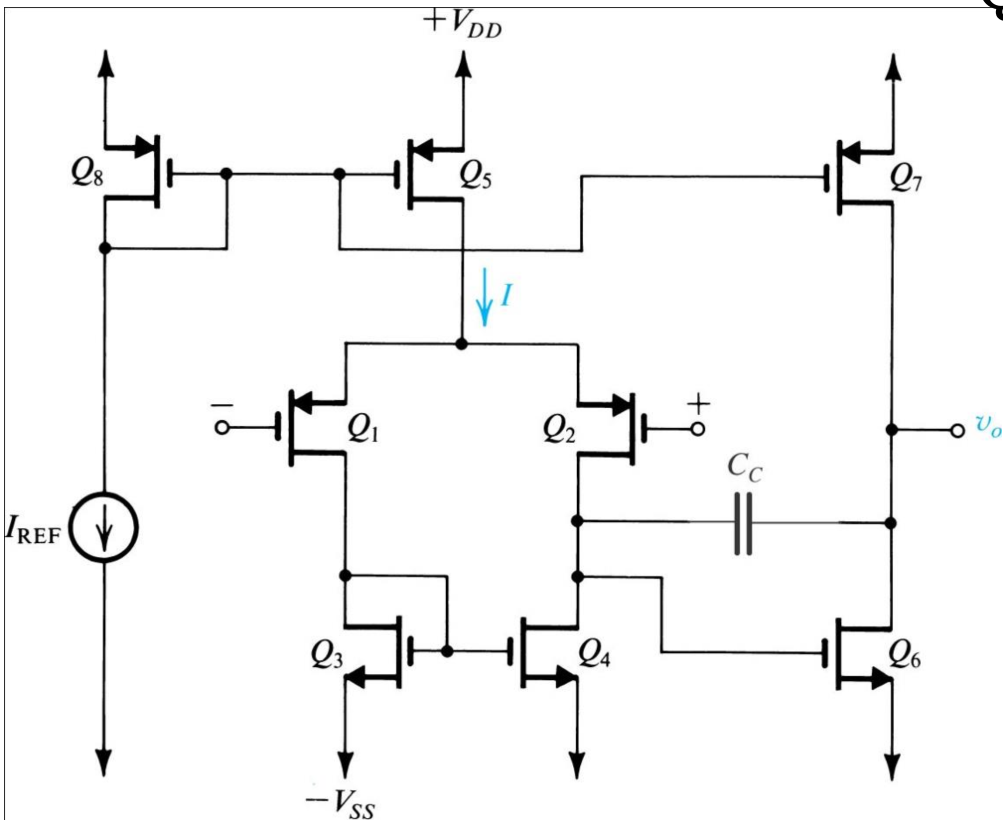
- Output resistance $R_o = r_{o6} \parallel r_{o7}$

12.1.4 Common-Mode Rejection Ratio (CMRR)

Section 8.5.5; eq. (8.158)

$$\mathrm{CMRR} = \frac{|A_d|}{|A_{cm}|} = [\,g_m(r_{o2} // r_{o4})][\,2g_{m3}R_{SS}\,]$$

Q_5's output resistance R_{SS}

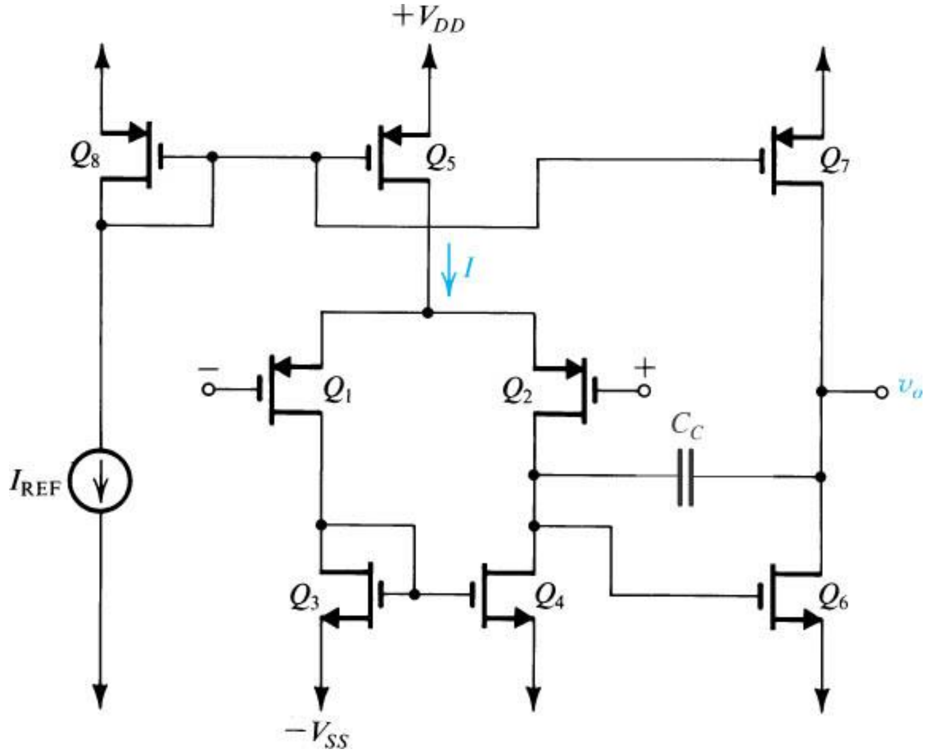


$$CMRR \propto (g_m r_o)^2$$

$$g_m r_o \propto \frac{V_A}{V_{OV}} = \frac{V_A' \cdot L}{V_{OV}}$$

$$\therefore L \Uparrow \Rightarrow CMRR \Uparrow$$

12.1.5 Frequency Response



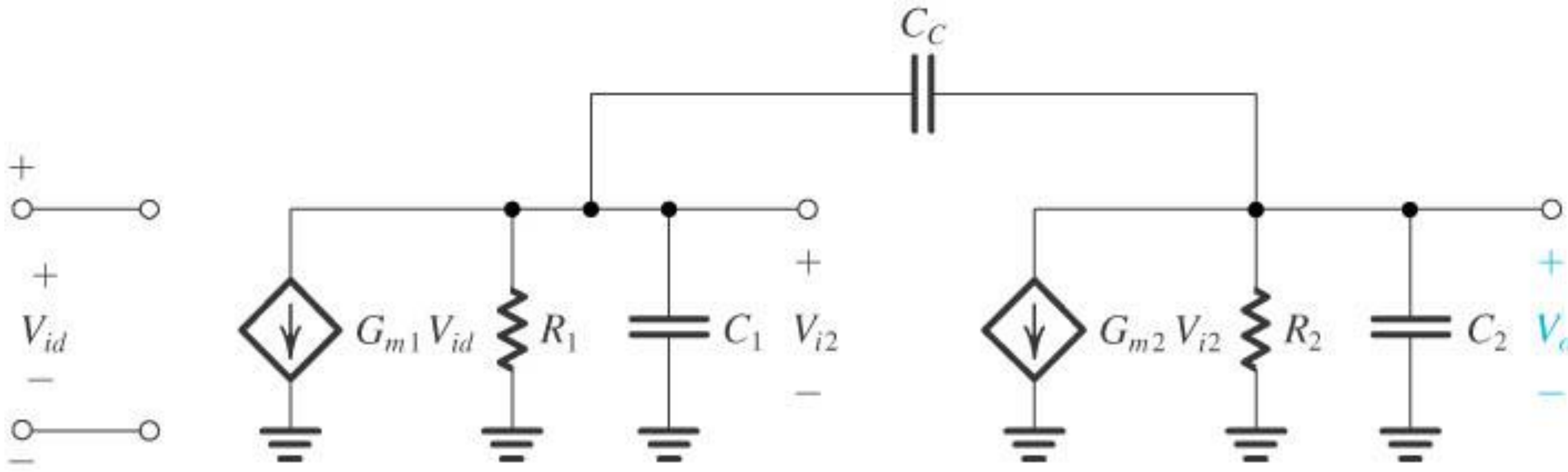
$$C_1 = C_{gd2} + C_{db2} + C_{gd4} + C_{db4} + C_{gs6}$$

$$C_2 = C_{db6} + C_{db7} + C_{gd7} + C_L$$

$C_C >> C_{gd6} \rightarrow C_{gd6}$ is neglected

$$R_1 = r_{o2} \parallel r_{o4}$$

$$R_2 = r_{o6} \parallel r_{o7}$$



$$G_{m1}V_{id}+\frac{V_{i2}}{R_1}+sC_1V_{i2}+sC_C(V_{i2}-V_o)=0$$

$$G_{m2}V_{i2}+\frac{V_o}{R_2}+sC_2V_o+sC_C(V_o-V_{i2})=0$$

$$\frac{V_0}{V_{id}}=\frac{G_{m1}(G_{m2}-sC_C)R_1R_2}{1+s[C_1R_1+C_2R_2+C_C(G_{m2}R_1R_2+R_1+R_2)]+s^2[C_1C_2+C_C(C_1+C_2)]R_1R_2}$$

$$S_Z=\frac{G_{m2}}{C_C}\Rightarrow\omega_Z=\frac{G_{m2}}{C_C}$$

$$D(s) = (1+\frac{s}{\omega_{P1}})(1+\frac{s}{\omega_{P2}}) = 1 + s(\frac{1}{\omega_{P1}} + \frac{1}{\omega_{P2}}) + \frac{s^2}{\omega_{P1}\omega_{P2}}$$

$$\omega_{P1} << \omega_{P2} \;\Rightarrow D(s) \approx 1 + \frac{s}{\omega_{P1}} + \frac{s^2}{\omega_{P1}\omega_{P2}}$$

$$\omega_{P1} = \frac{1}{C_1R_1 + C_2R_2 + C_C(G_{m2}R_1R_2 + R_1 + R_2)} \qquad \omega_{P2} = \frac{C_C G_{m2}}{C_1C_2 + C_C(C_1 + C_2)}$$

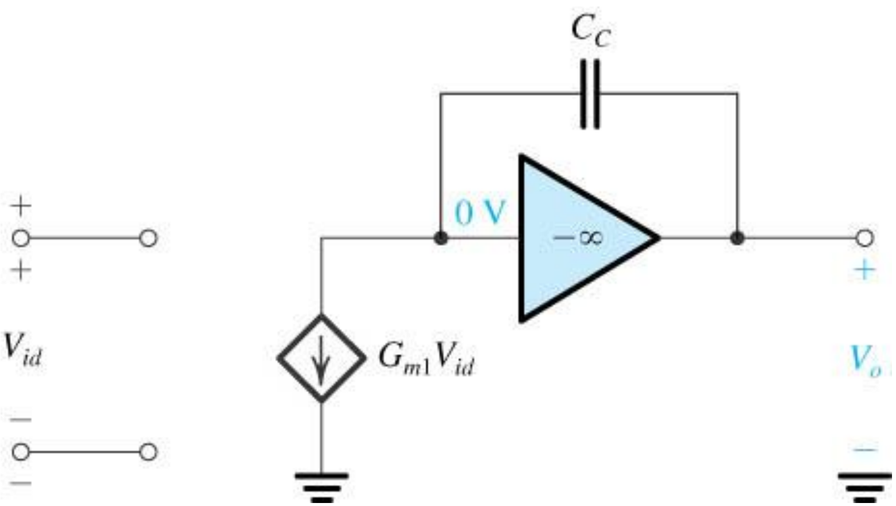
$$\because C_C >> C_1, C_2 >> C_1, G_{m2}R_2 >> 1 \Rightarrow \omega_{P1} \approx \frac{1}{C_C G_{m2} R_1 R_2},\; \omega_{P2} \approx \frac{G_{m2}}{C_2}$$

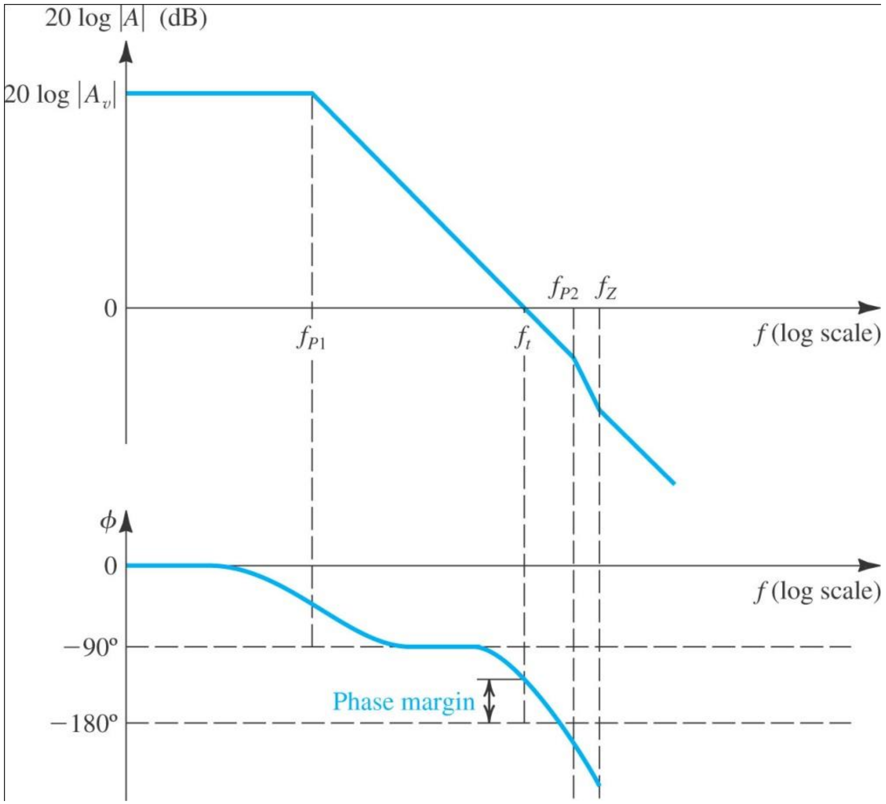
$$\omega_t = A_M \omega_{P1} = G_{m1}G_{m2}R_1R_2 \frac{1}{C_C G_{m2} R_1 R_2} = \frac{G_{m1}}{C_C}$$

$$\omega_t << \omega_{P2}, \omega_Z \Rightarrow \frac{G_{m1}}{C_C} < \frac{G_{m2}}{C_2} \text{ and } G_{m1} < G_{m2}$$

When $f >> f_{P1}$, a uniform -20dB/decade gain rolloff down to 0dB

→Simplified Equivalent Circuit





Phase margin

$$A(s) = \frac{A_o(1 - s/\omega_Z)}{(1 + s/\omega_{P1})(1 + s/\omega_{P2})}$$

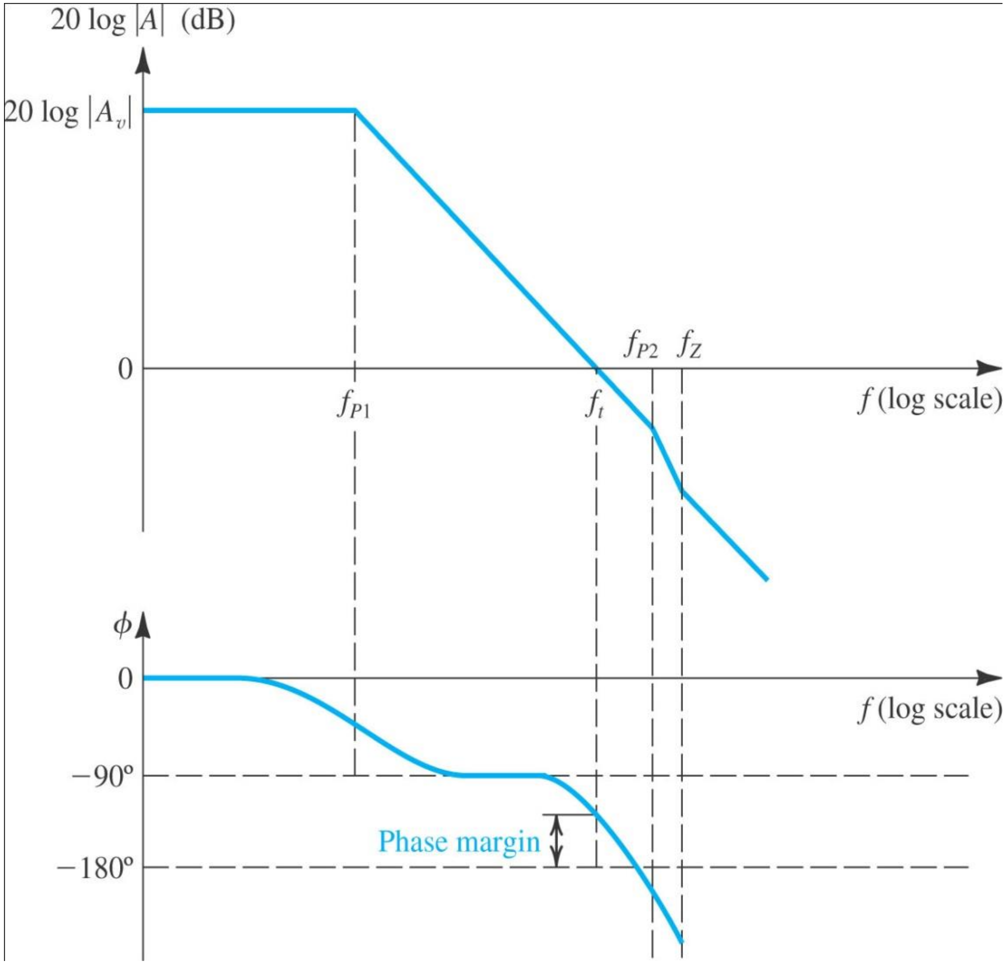
$$\omega = \omega_t$$

$$\phi_{P1} = -\tan^{-1}\left(\frac{f_t}{f_{P1}}\right) \approx -90^o$$

$$\phi_{P2} = -\tan^{-1}\left(\frac{f_t}{f_{P2}}\right)$$

$$\phi_Z = -\tan^{-1}\left(\frac{f_t}{f_Z}\right)$$

$$\phi_{\text{total}} = 90^\circ + \tan^{-1}(f_t / f_{P2}) + \tan^{-1}(f_t / f_Z)$$



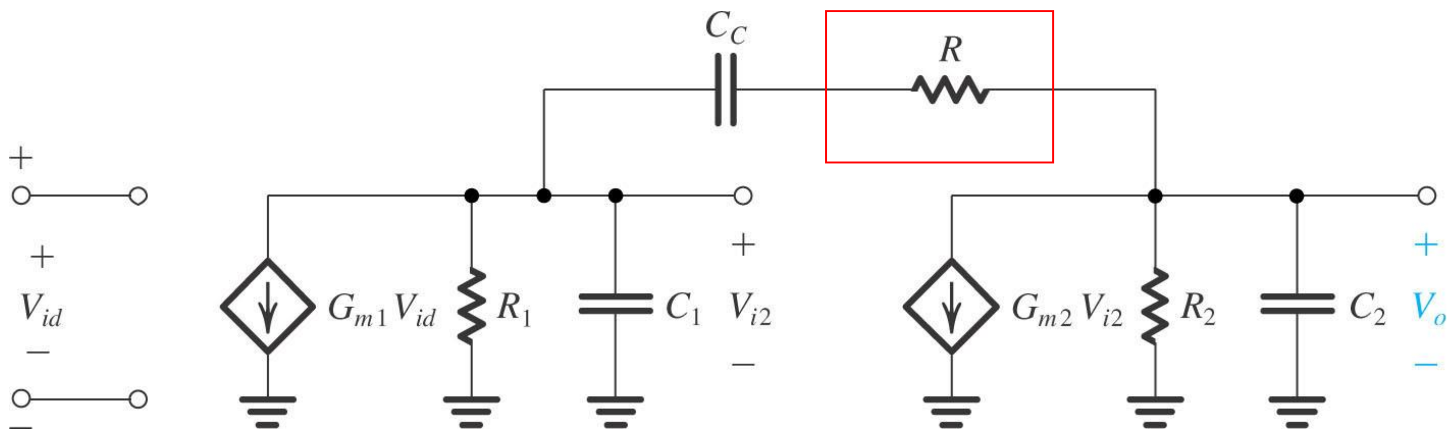
$$\text{Phase Margin(PM)} = 180^\circ - \phi_{\text{total}}$$

$$= 90^\circ - \tan^{-1}(f_t / f_{p2}) - \tan^{-1}(f_t / f_z)$$

$$\textit{If } f_Z \geq 10 f_t, \text{PM} = 60^o \Rightarrow 60^o = 90^o - \tan^{-1}(f_t / f_{P2}) - 5.71^o$$

$$\Rightarrow f_{P2} / f_t \approx 2.2$$

The right-half-plane zero reduces the phase margin.
How to improve it?



- Find zero: Vo=0

$$\frac{V_{i2}}{R+1/sC_C} = G_{m2}V_{i2} \Rightarrow s_z = \frac{1}{C_C(1/G_{m2} - R)}$$

  - $R = 1/G_{m2}$, the zero can be placed at infinite frequency.
  - $R > 1/G_{m2}$, a left-half plane zero improves the phase margin.

- Discussion: The second pole is not very far from ω_t. Thus the second pole introduces appreciable phase shift at ω_t, which reduces the phase margin.

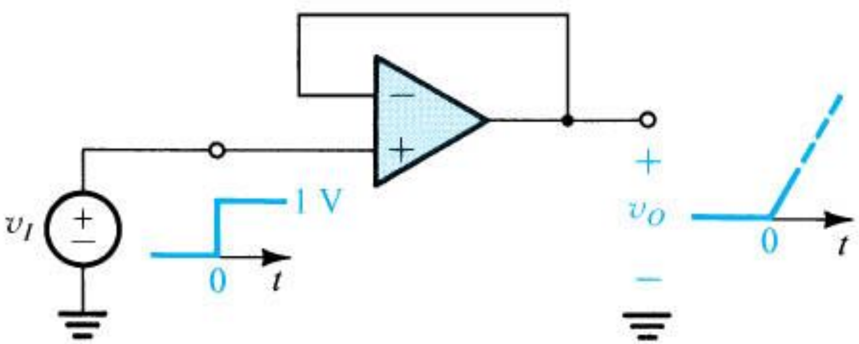
12.1.6 Slew Rate

- When a large output signal is present, slew-rate limiting can cause nonlinear distortion.
- Slew rate: the maximum rate of change possible at the output of a real op amp.

$$SR = \left.\frac{dv_o}{dt}\right|_{\max}$$

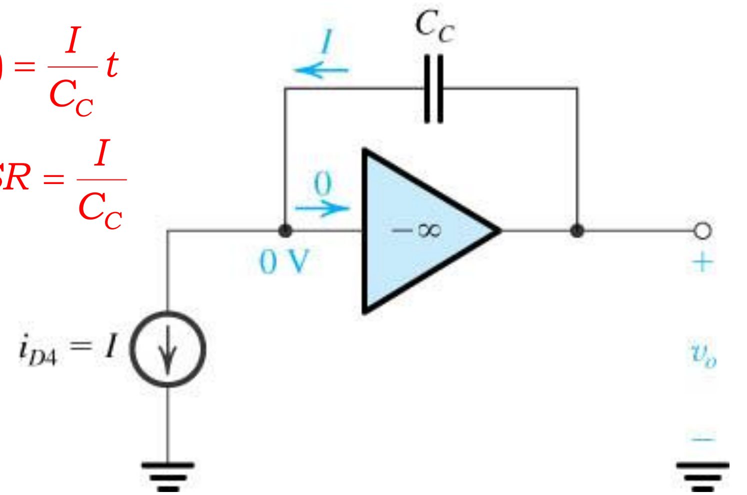
- A unity-gain follower with a large step input.

  (the output voltage cannot change immediately.)



$$v_o(t) = \frac{I}{C_C} t$$

$$\Rightarrow SR = \frac{I}{C_C}$$



Relationship Between SR and f_t

Slew rate

$$SR = \frac{I}{C_C}$$

$$G_{m1} = g_{m1} = \frac{I}{V_{OV1}}$$

$$\omega_t = \frac{G_{m1}}{C_C}$$

$$\Rightarrow SR = V_{OV1}\omega_t$$

- For a given ω_t, the slew rate is determined by the overdrive voltage at which the input transistor are operated.
- $V_{OV} \uparrow \Rightarrow SR \uparrow$.

❶ For a given bias current *I*, a large V_{OV} is obtained if Q_1 and Q_2 are *p*-channel devices. (1st stage)

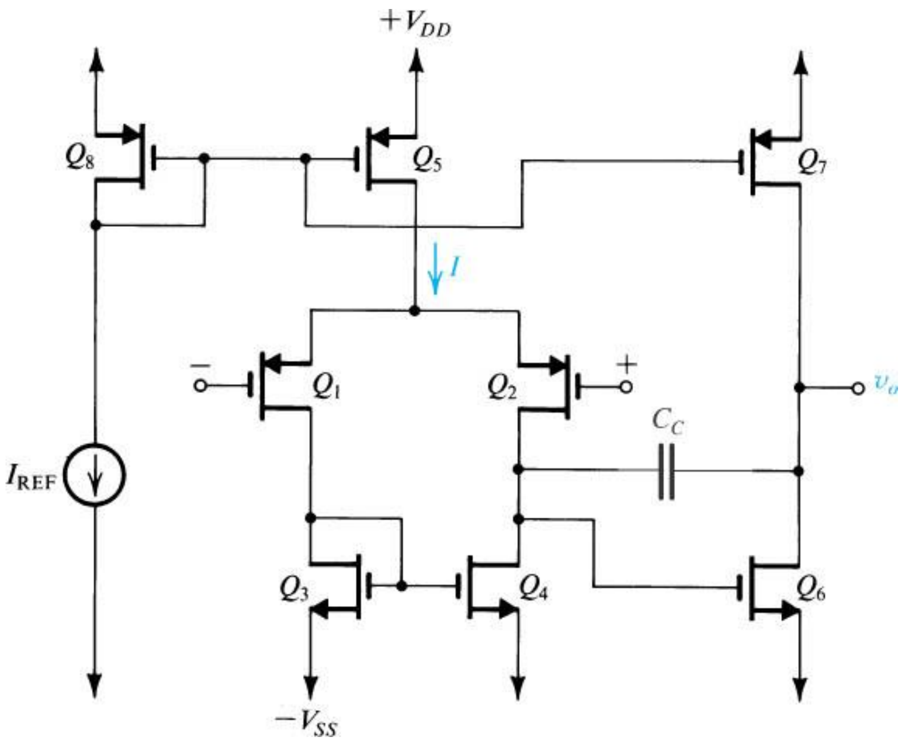
❷ It allows the 2nd stage to employ an *n*-channel device that has a greater transconductance, G_{m2}, resulting in a higher second-pole frequency and a corresponding higher ω_t.

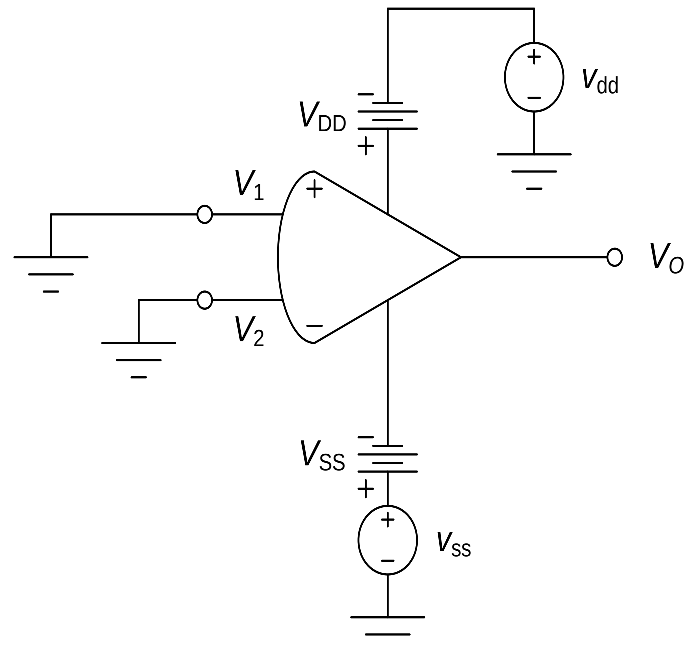
12.1.7 Power-Supply Rejection Ratio (PSRR)

PSRR is defined as the ratio of the amplifier differential gain to the gain experienced by a change in the power-supply voltage (v_{dd} and v_{ss})

$$PSRR^+ = \frac{A_d}{A^+} \text{ and } PSRR^- = \frac{A_d}{A^-}$$

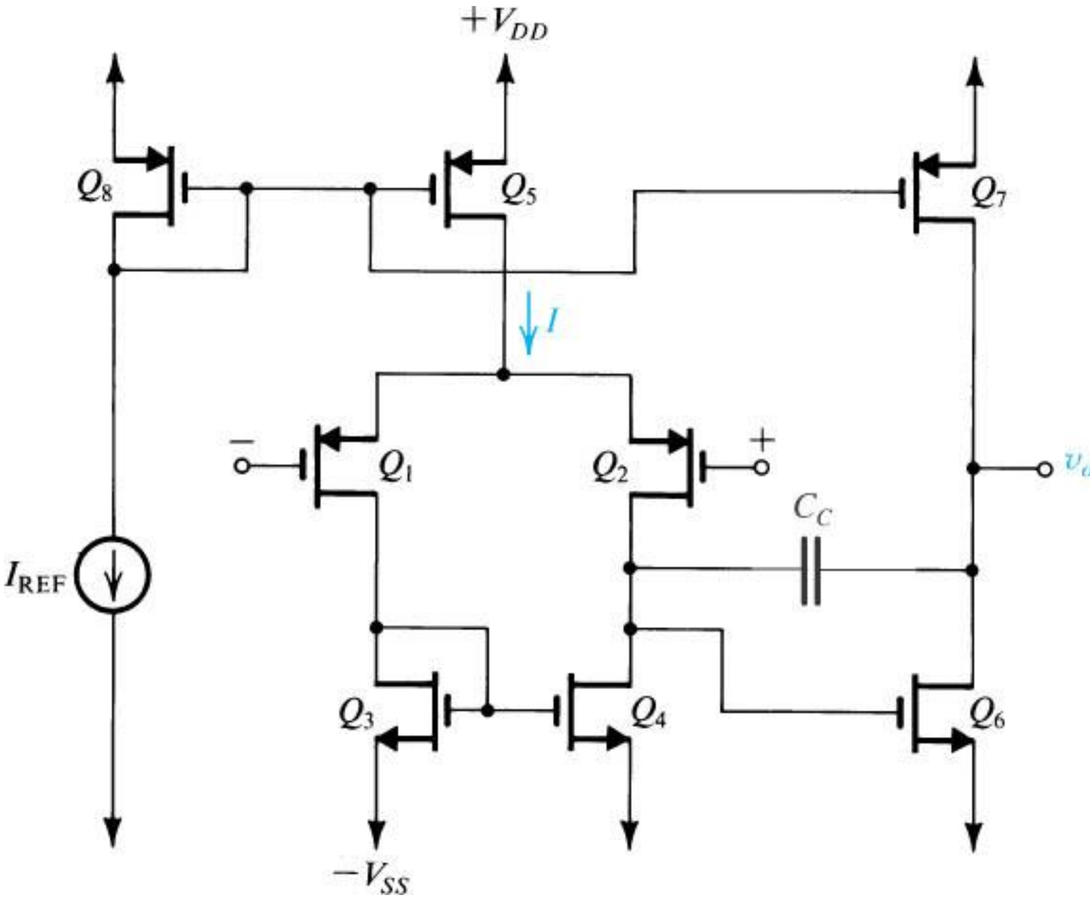
$$A^+ = \frac{v_o}{v_{dd}} \text{ and } A^- = \frac{v_o}{v_{ss}}$$





$PSRR^+$ is high

since Q_5 and Q_7 are current sources



$PSRR^-$

$$v_o = v_{ss}\frac{r_{o7}}{r_{o6}+r_{o7}}$$

$$A^- = \frac{v_o}{v_{ss}} = \frac{r_{o7}}{r_{o6}+r_{o7}}$$

$$PSRR^- = \frac{A_d}{A^-} = g_{m1}(r_{o2}//r_{o4})g_{m6}r_{o6}$$

$$PSRR^- \propto (g_m r_o)^2$$

$$g_m r_o \propto \frac{V_A}{V_{OV}} = \frac{V_A^{'} \cdot L}{V_{OV}}$$

$$\therefore L \Uparrow \Rightarrow PSRR^- \Uparrow$$

12.1.8 Design Tradeoffs

1. The length L used for each MOSFET
2. Overdrive voltage $|V_{OV}|$ for each MOSFET

$$CMRR \propto (g_m r_o)^2$$

$$g_m r_o \propto \frac{V_A}{V_{OV}} = \frac{V_A^{'} \cdot L}{V_{OV}}$$

$$\therefore L \Uparrow \Rightarrow CMRR \Uparrow$$

$$PSRR^- \propto (g_m r_o)^2$$

$$g_m r_o \propto \frac{V_A}{V_{OV}} = \frac{V_A^{'} \cdot L}{V_{OV}}$$

$$\therefore L \Uparrow \Rightarrow PSRR^- \Uparrow$$

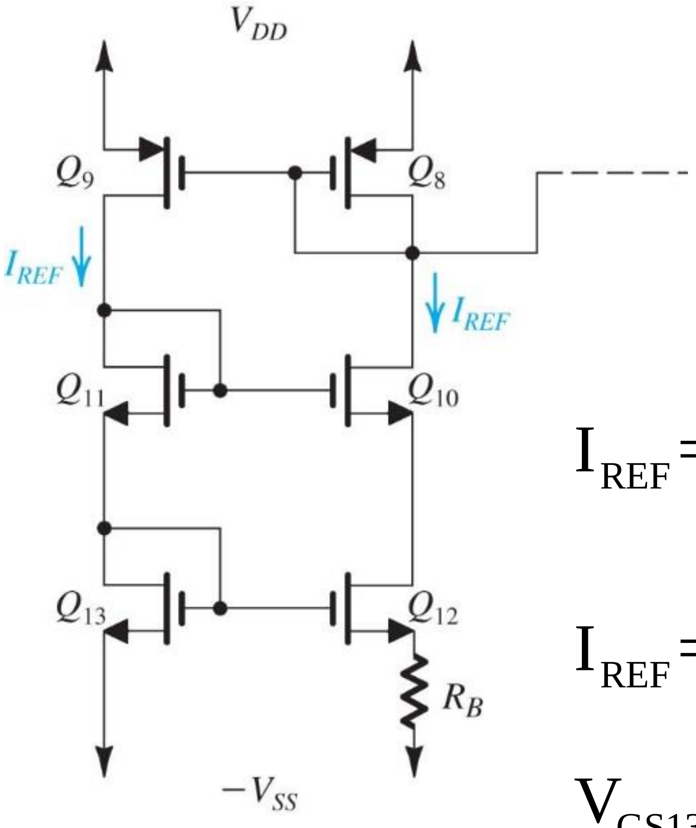
$$g_m = \mu_n C_{OX} \frac{W}{L} V_{OV}$$

$$C_{gs} \approx \frac{2}{3} W L C_{ox}$$

transition frequency

$$f_T = \frac{\omega_T}{2\pi} = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \approx \frac{1.5\mu_n V_{OV}}{2\pi L^2}$$

12.1.9 A Bias Circuit for the Two-Stage CMOS Op Amp



1. All devices are in the saturation region
2. Q8 and Q9, Q10 and Q11 matched
3. Q12 and Q13 not matched
4. Positive feedback; $R_B \downarrow I_{D13} \uparrow V_{G13} \uparrow$
5. Need a kick-off circuit

$$I_{REF} = \frac{\mu_n C_{OX}}{2}\left(\frac{W}{L}\right)_{12}\left(V_{GS12} - V_t\right)^2$$

$$I_{REF} = \frac{\mu_n C_{OX}}{2}\left(\frac{W}{L}\right)_{13}\left(V_{GS13} - V_t\right)^2$$

$$V_{GS13} = V_{GS12} + I_{REF} R_B \Rightarrow$$

$$\sqrt{\frac{2I_{REF}}{\mu_n C_{OX}(W/L)_{13}}} = \sqrt{\frac{2I_{REF}}{\mu_n C_{OX}(W/L)_{12}}} + I_{REF} R_B$$

$$I_{REF} = \frac{2}{\mu_n C_{OX} (W/L)_{12} R_B^2} \left(\sqrt{\frac{(W/L)_{12}}{(W/L)_{13}}} - 1 \right)^2$$

$$R_B = \frac{2}{\sqrt{2\mu_n C_{OX} (W/L)_{12} I_{REF}}} \left(\sqrt{\frac{(W/L)_{12}}{(W/L)_{13}}} - 1 \right)$$

$$= \frac{2}{g_{m12}} \left(\sqrt{\frac{(W/L)_{12}}{(W/L)_{13}}} - 1 \right)$$

$$\Rightarrow g_{m12} = \frac{2}{R_B} \left(\sqrt{\frac{(W/L)_{12}}{(W/L)_{13}}} - 1 \right)$$

$$\because g_{m12} = \sqrt{2\mu_n C_{OX} (W/L)_{12} I_{REF}}$$

for each n-channel transistor in this bias circuit

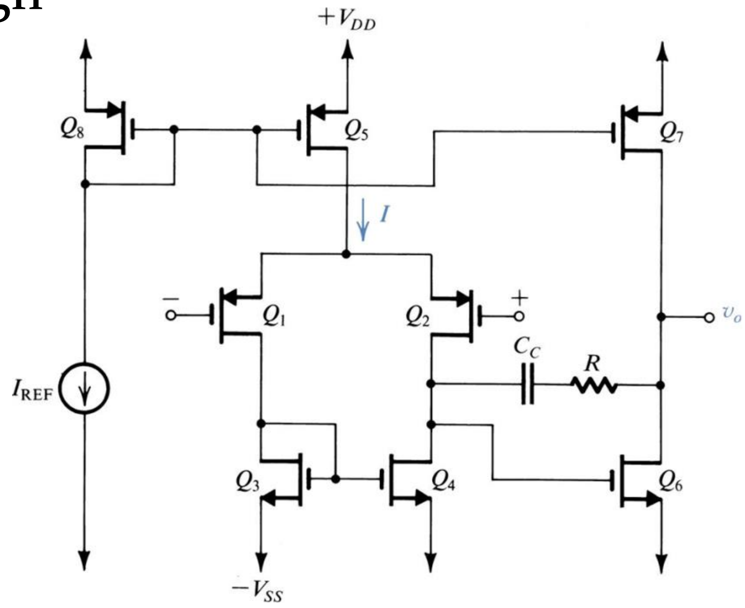
$$\frac{g_{mi}}{g_{m12}} = \sqrt{\frac{(W/L)_i I_{Di}}{(W/L)_{12} I_{REF}}}$$

for each p-channel transistor in this bias circuit

$$\frac{g_{mi}}{g_{m12}} = \sqrt{\frac{\mu_p (W/L)_i I_{Di}}{\mu_n (W/L)_{12} I_{REF}}}$$

Ex.12.1 Two-Stage CMOS Op Amp Design

Design a dc gain of 4000 V/V in a 0.5-μm CMOS technology. $V_{tn} = |V_{tp}| = 0.5$V, $k'_n = 200\ \mu A/V^2$, $k'_p = 80\ \mu A/V^2$, $V'_{An} = |V'_{Ap}| = 20V/\mu m$, $V_{DD} = V_{SS} = 1.65$V, $L = 1\mu m$ for all devices. Let $I = 200\mu A$, $I_{D6} = 0.5mA$. If $C_1 = 0.2$pF and $C_2 = 0.8$pF, find the required C_C and R to place the transmission zero at $s = \infty$ for phase margin of 85°.



Solution

- Voltage gain $A_v = g_{m1}(r_{o2} \| r_{o4}) g_{m6}(r_{o6} \| r_{o7}) = \frac{2(I/2)}{V_{OV}} \cdot \frac{1}{2} \cdot \frac{V_A}{(I/2)} \cdot \frac{2I_{D6}}{V_{OV}} \cdot \frac{1}{2} \cdot \frac{V_A}{I_{D6}} = \left(\frac{V_A}{V_{OV}}\right)^2$

$A_v = 4000$ and $V_A = 20$V ⇨ $4000 = \frac{400}{V_{OV}^2} \quad \Rightarrow \quad V_{OV} = 0.316$V

- $(W/L)_1$ and $(W/L)_2$:

$$I_{D1} = \frac{1}{2} k'_p \left(\frac{W}{L}\right)_1 v_{OV}^2 \quad \Rightarrow \quad 100 = \frac{1}{2} \cdot 80 \left(\frac{W}{L}\right)_1 \cdot 0.316^2 \quad \Rightarrow \quad \left(\frac{W}{L}\right)_1 = \frac{25\mu m}{1\mu m} = \left(\frac{W}{L}\right)_2$$

- $(W/L)_3$ and $(W/L)_4$:

$$I_{D1} = \frac{1}{2} k_n' \left(\frac{W}{L}\right)_3 v_{OV}^2 \quad \Rightarrow \quad 100 = \frac{1}{2} \cdot 200 \left(\frac{W}{L}\right)_3 \cdot 0.316^2 \quad \Rightarrow \quad \left(\frac{W}{L}\right)_3 = \frac{10\mu m}{1\mu m} = \left(\frac{W}{L}\right)_4$$

- $(W/L)_5$:

$$I_{D5} = \frac{1}{2} k_p' \left(\frac{W}{L}\right)_5 v_{OV}^2 \quad \Rightarrow \quad 200 = \frac{1}{2} \cdot 80 \left(\frac{W}{L}\right)_5 \cdot 0.316^2 \quad \Rightarrow \quad \left(\frac{W}{L}\right)_5 = \frac{50\mu m}{1\mu m}$$

- $(W/L)_6$ and $(W/L)_7$:

$$\left(\frac{W}{L}\right)_7 = 2.5 \left(\frac{W}{L}\right)_5 = \frac{125\mu m}{1\mu m} \qquad 500 = \frac{1}{2} \cdot 200 \left(\frac{W}{L}\right)_6 \cdot 0.316^2 \quad \Rightarrow \quad \left(\frac{W}{L}\right)_6 = \frac{50\mu m}{1\mu m}$$

- Select $I_{REF} = 20\mu$A, thus $\left(\frac{W}{L}\right)_8 = 0.1 \left(\frac{W}{L}\right)_5 = \frac{5\mu m}{1\mu m}$

- Input CM range: $-1.33 \text{ V} \le V_{ICM} \le 0.52 \text{ V}$

  $(-V_{SS} + V_{OV3} + V_{tn} - |V_{tp}| \le V_{ICM} \le V_{DD} - |V_{tp}| - |V_{OV1}| - |V_{OV5}|)$

- Max. signal swing: $-1.33 \text{ V} \le v_o \le 1.33 \text{ V}$
- Input resistance: $R_i = \infty$
- Output resistance: $R_o = r_{o6} \parallel r_{o7} = 20 \text{ k}\Omega$

$$\mathrm{CMRR} = [g_m(r_{o2} // r_{o4})][2g_{m3}R_{SS}]$$

- $R_{SS} = r_{o5} = V_A / I$

$$\mathrm{CMRR} = \frac{2(I/2)}{V_{OV}} \cdot \frac{1}{2} \cdot \frac{V_A}{(I/2)} \cdot 2 \cdot \frac{2(I/2)}{V_{OV}} \cdot \frac{V_A}{I}$$

$$= 2\left(\frac{V_A}{V_{OV}}\right)^2 = 2\left(\frac{20}{0.316}\right)^2 = 8000$$

$$\mathrm{CMRR} = 20\,log(8000) = 78\mathrm{dB}$$

- $PSRR^- = g_{m1}(r_{o2} // r_{o4}) g_{m6} r_{o6}$

$$= \frac{2(I/2)}{V_{OV}} \cdot \left(\frac{1}{2} \cdot \frac{V_A}{(I/2)}\right) \cdot \frac{2I_{D6}}{V_{OV}} \cdot \frac{V_A}{I_{D6}}$$

$$= 2\left(\frac{V_A}{V_{OV}}\right)^2 = 2\left(\frac{20}{0.316}\right)^2 = 8000$$

$$PSRR^- = 20\log(8000) = 78dB$$

- Determine $fp2$:

$$G_{m2} = g_{m6} = \frac{2I_{D6}}{V_{OV}} = \frac{2 \times 0.5}{0.316} = 3.2mA/V \qquad f_{p2} \approx \frac{G_{m2}}{2\pi C_2} = \frac{3.2 \times 10^{-3}}{2\pi \cdot 0.8 \times 10^{-12}} = 637MHz$$

- To move the transmission zero to $s = \infty$, we select the value of R as

$$R = \frac{1}{G_{m2}} = \frac{1}{3.2\times 10^{-3}} = 316\Omega$$

- For a phase margin of 85°, the phase shift due to f_{p2} at $f = f_t$ must be 5°, that is

$$\tan^{-1}\frac{f_t}{f_{p2}} = 5^\circ$$

$$\Rightarrow \quad f_t = 637\times \tan 5^\circ = 55.7MHz$$

- Determine C_C:

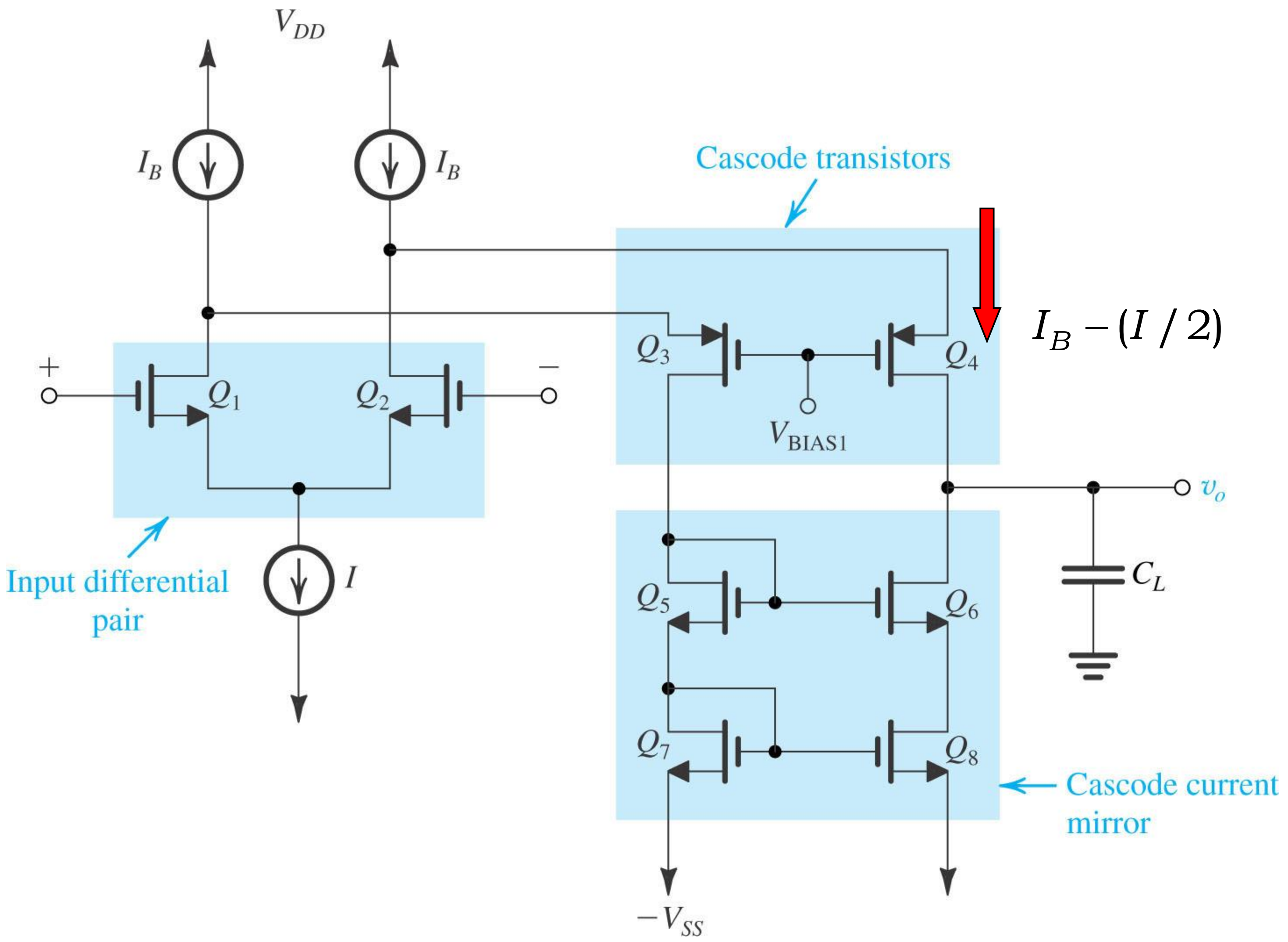
$$C_C = \frac{G_{m1}}{2\pi f_t} \qquad \text{where} \quad G_{m1} = g_{m1} = \frac{2\cdot 100\mu A}{0.316V} = 0.63mA/V$$

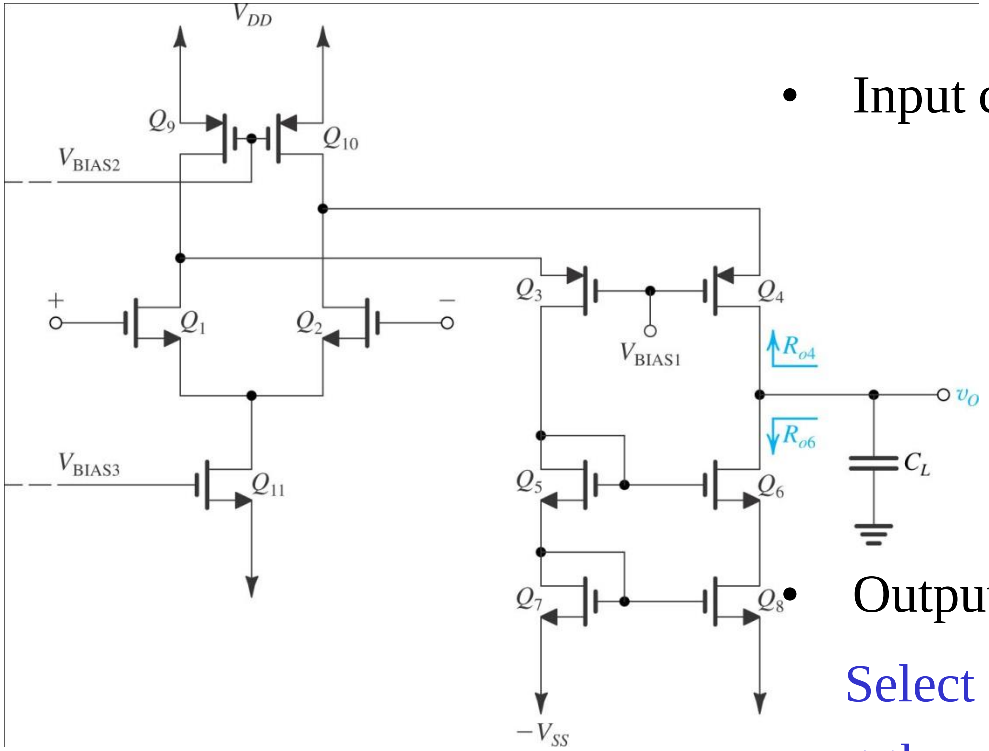
$$\therefore \quad C_C = \frac{0.6\times 10^{-3}}{2\pi\cdot 55.7\times 10^{6}} = 1.8pF$$

- Slew rate: [Eq. (12.46)]

$$SR = 2\pi f_t V_{OV} = 2\pi\cdot 55.7\times 10^{6}\times 0.316 = 111V/\mu s$$

12.2 The Folded Cascode CMOS Op Amp





- Input common-mode range:

$$V_{ICM\,\max} = V_{DD} - |V_{OV9}| + V_{tn}$$

$$V_{ICM\,\min} = -V_{SS} + V_{OV11} + V_{OV1} + V_{tn}$$

$$-V_{SS} + V_{OV11} + V_{OV1} + V_{tn} \le V_{ICM} \le V_{DD} - |V_{OV9}| + V_{tn}$$

- Output voltage swing:

Select V_{BIAS1} so that Q_{10} operates at the edge of saturation:

$$V_{BIAS1} = V_{DD} - |V_{OV10}| - V_{SG4}$$

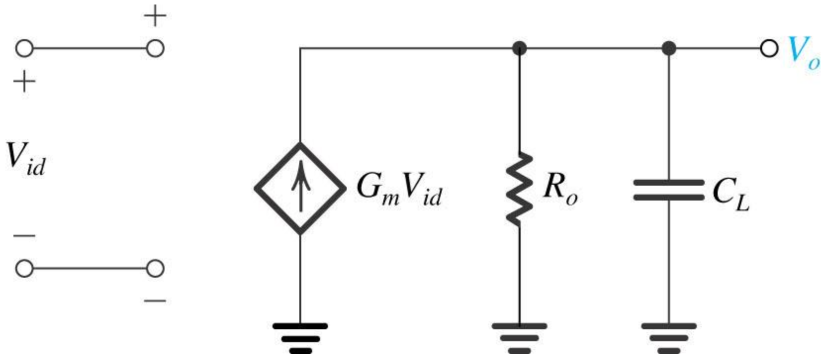
$$\Rightarrow v_{o\,\max} = V_{DD} - |V_{OV10}| - |V_{OV4}|$$

$v_{o,min}$ is obtained when Q_6 reaches the edge of saturation.

$$v_{o\,\min} = -V_{SS} + V_{OV7} + V_{OV5} + V_{tn}$$

- Voltage gain

  Small-signal equivalent circuit:



  – Transconductance

$$G_m = g_{m1} = g_{m2} \qquad G_m = \frac{2(I/2)}{V_{OV1}} = \frac{I}{V_{OV1}}$$

  – Output resistance

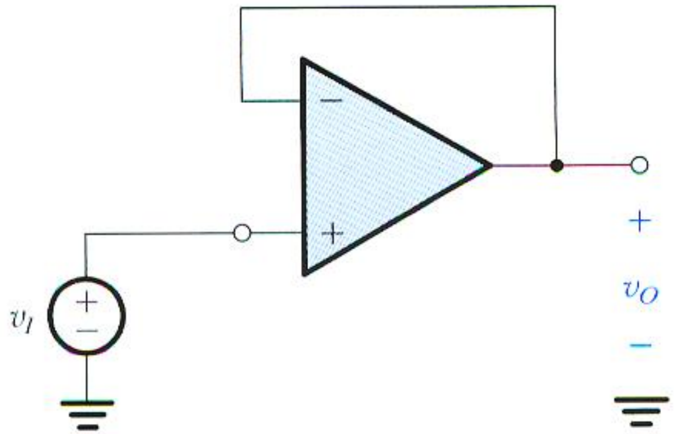
$$R_o = R_{o4} \| R_{o6} \qquad R_{o4} \approx (g_{m4}r_{o4})(r_{o2} \| r_{o10}) \qquad R_{o6} \approx g_{m6}r_{o6}r_{o8}$$

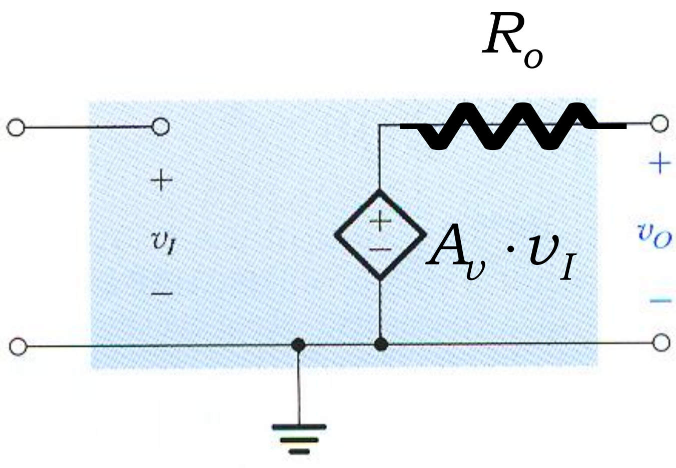
$$\Rightarrow \quad R_o = \left[g_{m4}r_{o4}(r_{o2} \| r_{o10})\right] \| (g_{m6}r_{o6}r_{o8})$$

  – Open-loop gain

$$A_v = G_mR_o = g_{m1}\left\{\left[g_{m4}r_{o4}(r_{o2} \| r_{o10})\right] \| (g_{m6}r_{o6}r_{o8})\right\}$$

- Unity-gain buffer (voltage follower):





- Output resistance

$$R_{of} = \frac{R_o}{1 + A_v} \approx \frac{R_o}{A_v} = \frac{R_o}{G_m R_o} = \frac{1}{G_m} = \frac{1}{g_{m1}}$$

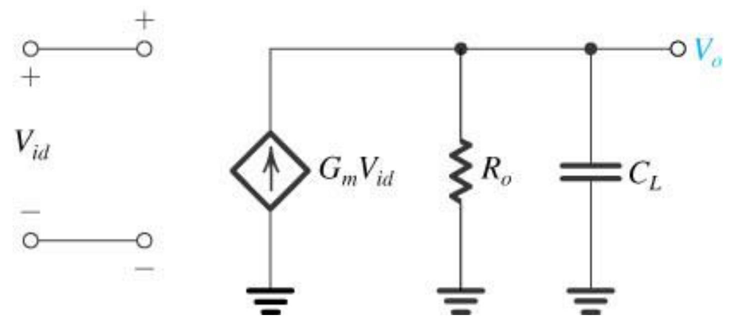
  - It is not very small for a single-stage op amp (OTA, operational transconductance amplifier).
  - An ideal op amp has an zero output resistance!

- Frequency response:

  Since the primary purpose of CMOS op amps is to feed capacitive loads, C_L is usually large, and the pole at the output becomes dominant.

  – Transfer function $\frac{V_o}{V_{id}} = \frac{G_m R_o}{1 + sC_L R_o}$

  – Dominant pole $f_p = \frac{1}{2\pi C_L R_o}$



  – Unity-gain frequency

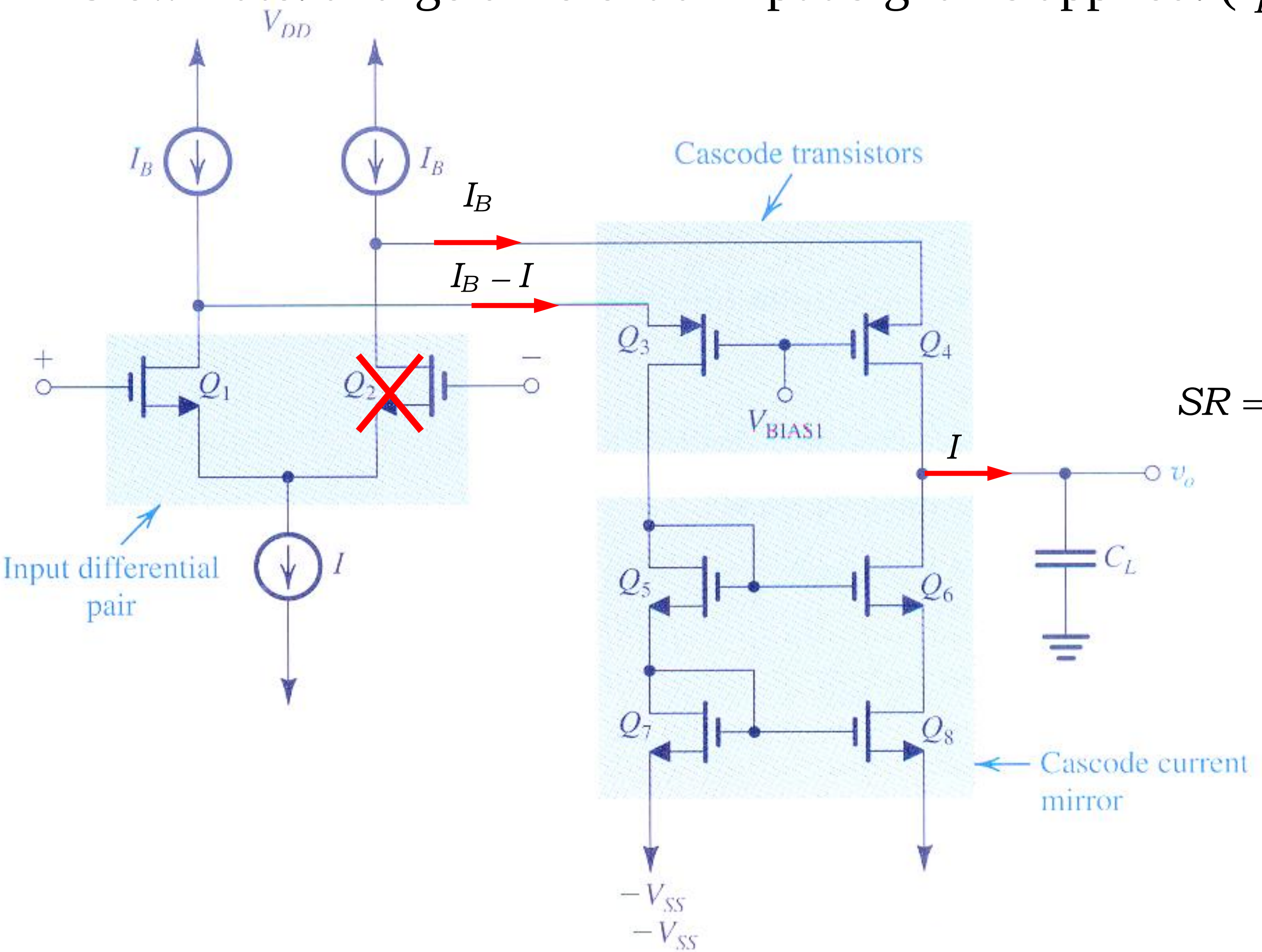
$$f_t = A_v f_p = G_m R_o f_p = \frac{G_m}{2\pi C_L}$$

  – Discussion

  Folded-cascode op amp: $C_L \uparrow \Rightarrow f_{p1},\ f_t \downarrow \Rightarrow$ phase margin $\uparrow$

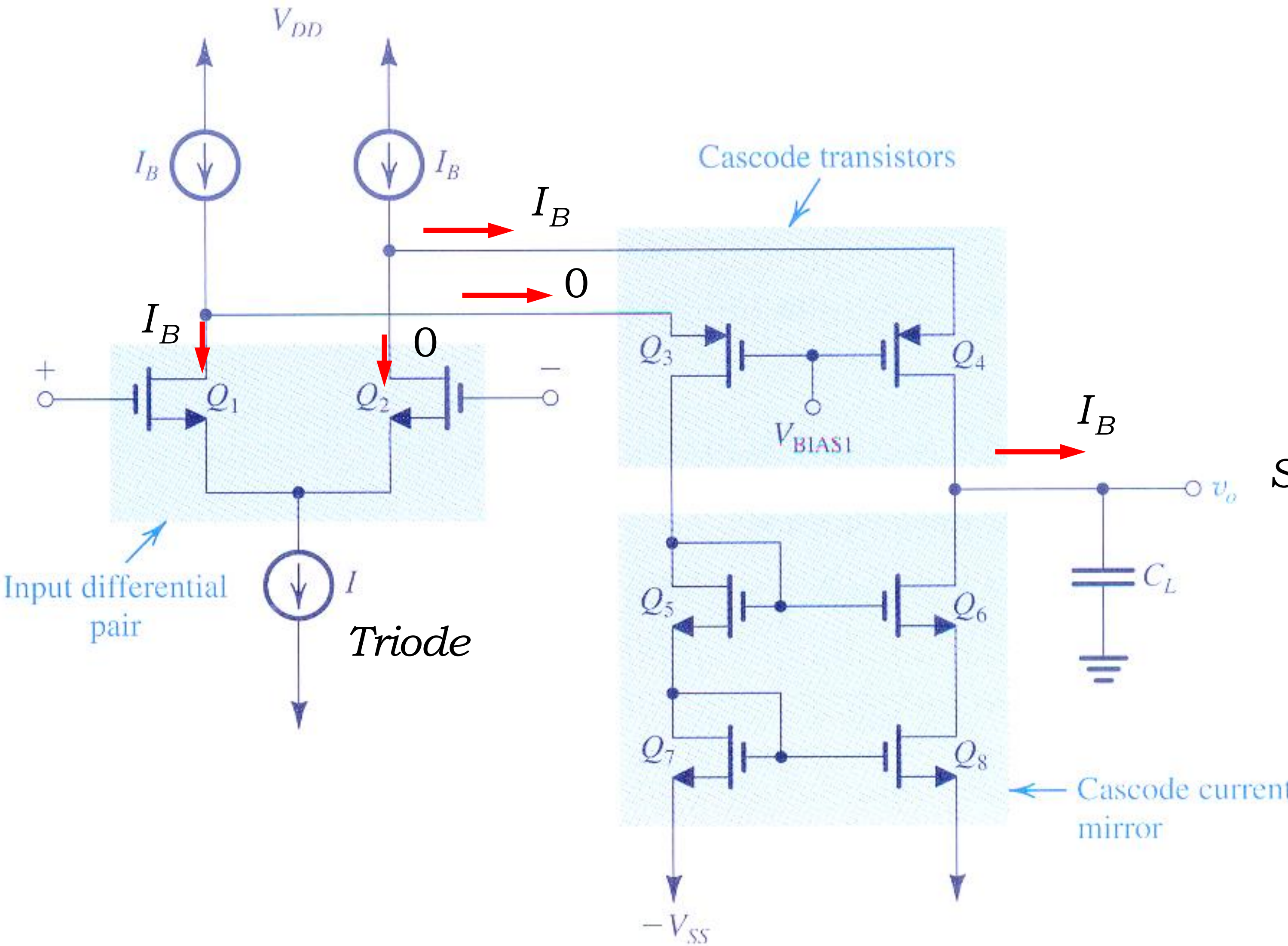
  Two-stage op amp: $C_L \uparrow \Rightarrow f_{p2} \downarrow \Rightarrow$ phase margin $\downarrow$

- Slew Rate: a large differential input signal is applied. ($I_B > I$)



$$SR = \frac{I}{C_L}$$

- Slew Rate: a large differential input signal is applied. ($0.5I < I_B < I$)

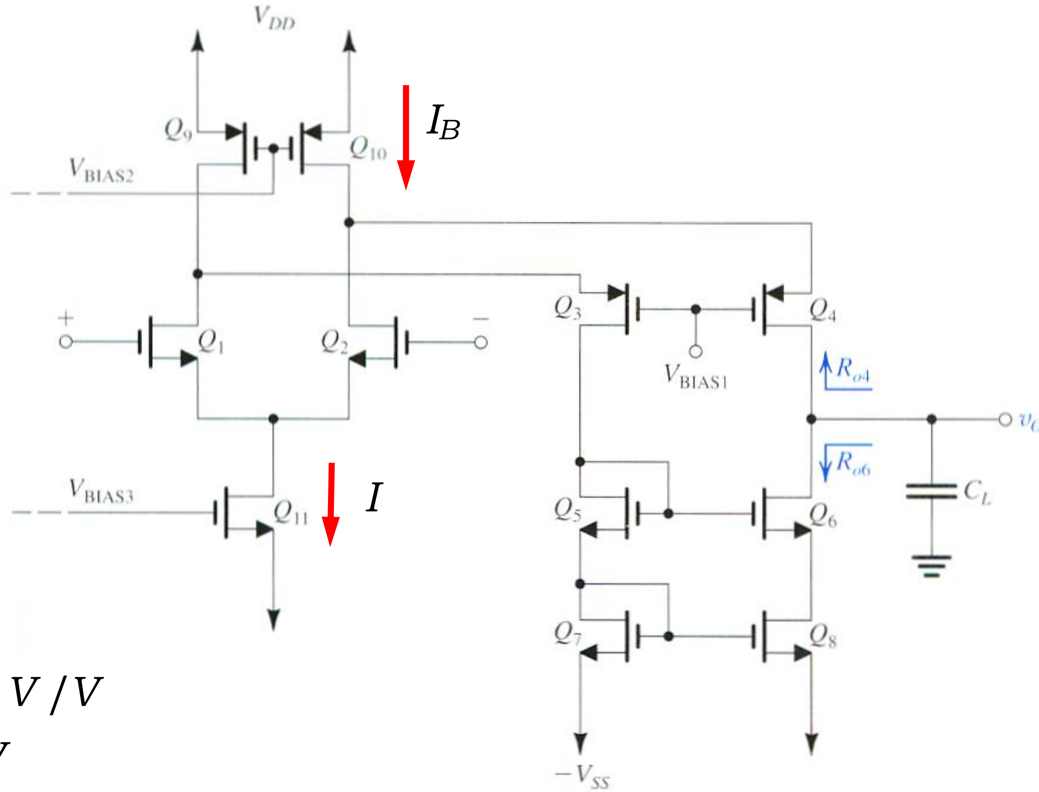


$$SR = \frac{I_B}{C_L}$$

Ex 12.2: Design of a folded-cascode op amp.

$I = 240\mu A$, $I_B = 150\mu A$, and $|V_{OV}| = 0.25V$ for all transistors. $V_{DD} = V_{SS} = 2.5V$
$K_n' = 100\mu A/V^2$, $K_p' = 40\mu A/V^2$, $|V_A'| = 20V/\mu m$ and $|V_t| = 0.75V$. $L = 1\mu m$,
$C_L = 5pF$.

- Find I_D, g_m, r_o and W/L for all transistors.



$$g_m = \frac{2I_D}{V_{OV}} = \frac{2I_D}{0.25}$$

$$r_o = \frac{|V_A|}{I_D} = \frac{20}{I_D}$$

$$\left(\frac{W}{L}\right)_i = \frac{2I_{Di}}{k' V_{OV}^2}$$

Note: for all transistors

$$g_m r_o = 160 \ V/V$$

$$V_{GS} = 1.0 \ V$$

	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9	Q_{10}	Q_{11}
I_D (μA)	120	120	30	30	30	30	30	30	150	150	240
g_m (mA/V)	0.96	0.96	0.24	0.24	0.24	0.24	0.24	0.24	1.2	1.2	1.92
r_o (kΩ)	167	167	667	667	667	667	667	667	133	133	83
W/L	38.4	38.4	24	24	9.6	9.6	9.6	9.6	120	120	76.8

- Find the allowable range of V_{ICM} and of the output voltage swing.

$$-1.25V \le \upsilon_o \le 2V$$

$$-1.25V \le V_{ICM} \le 3V$$

$$-V_{SS} + V_{OV11} + V_{OV1} + V_{tn} \le V_{ICM} \le V_{DD} - |V_{OV9}| + V_{tn}$$

$$\upsilon_{o\,\max} = V_{DD} - |V_{OV10}| - |V_{OV4}|$$
$$\upsilon_{o\,\min} = -V_{SS} + V_{OV7} + V_{OV5} + V_{tn}$$

- Determine the values of A_υ, f_t, f_p, and SR.

$$R_{o4} = (g_{m4} r_{o4})(r_{o2} \| r_{o10}) = 160(167 \| 133) = 11.85M\Omega \quad R_{o6} = g_{m6} r_{o6} r_{o8} = 106.7M\Omega$$

$$R_o = R_{o4} \| R_{o6} = 10.7M\Omega$$

$$A_\upsilon = G_m R_o = 0.96 \times 10^{-3} \cdot 10.7 \times 10^{6} = 10240V/V$$

$$f_t = \frac{G_m}{2\pi C_L} = \frac{0.96 \times 10^{-3}}{2\pi \cdot 5 \times 10^{-12}} = 30.6MHz$$

$$f_p = \frac{f_t}{A_\upsilon} \left(\text{or } = \frac{1}{2\pi C_L R_o} \right) = \frac{30.6MHz}{10240} = 3kHz$$

$$SR = \frac{I_B}{C_L} = \frac{150 \times 10^{-6}}{5 \times 10^{-12}} = 30V/\mu s$$

- What is the power dissipation of the op amp?

$$P_D = 5V \times 0.3mA = 1.5mW$$

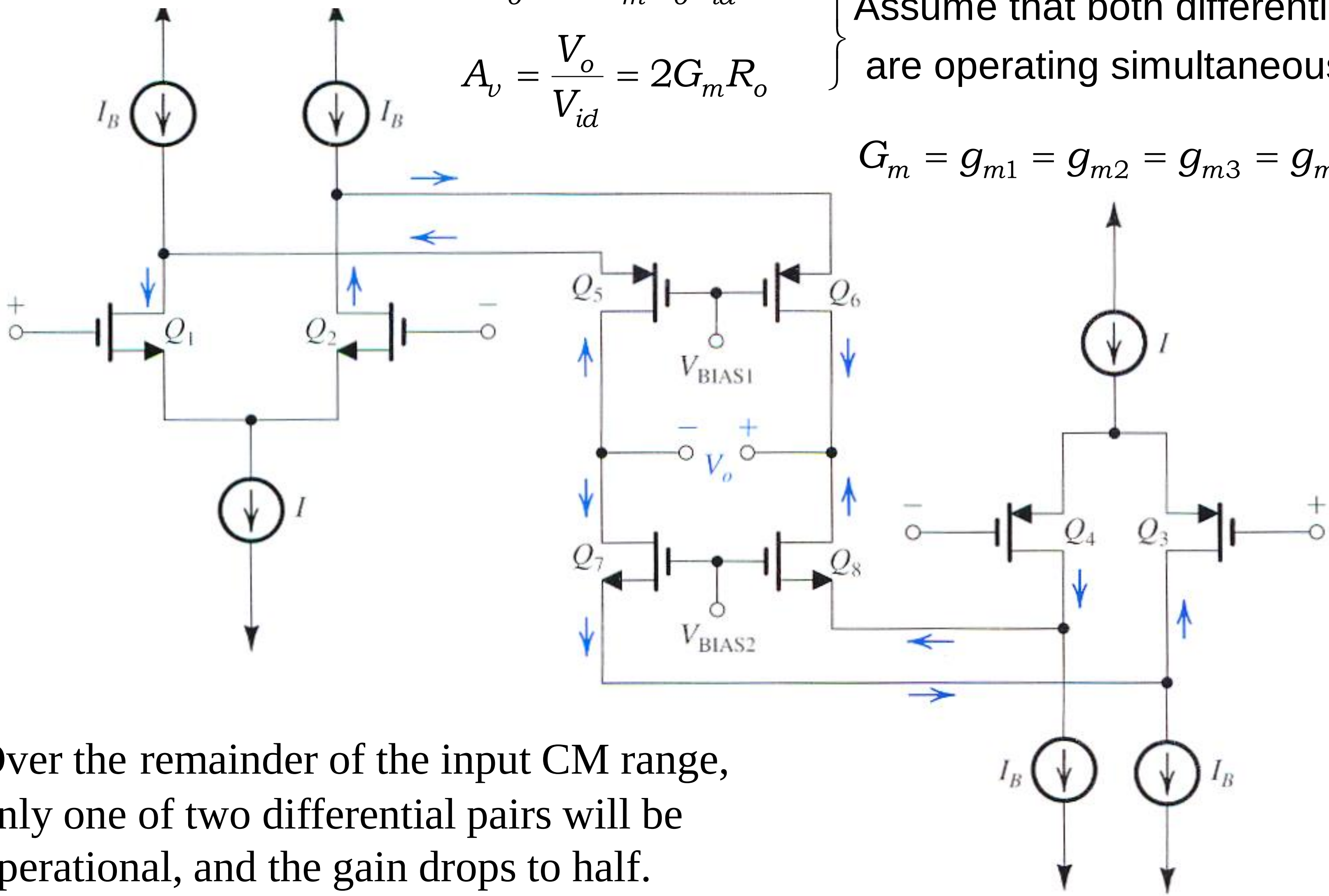
12.2.6 Increasing the Input Common-Mode Range: Rail-to-Rail Input Operation

$$V_o = 2G_m R_o V_{id}$$

$$A_v = \frac{V_o}{V_{id}} = 2G_m R_o$$

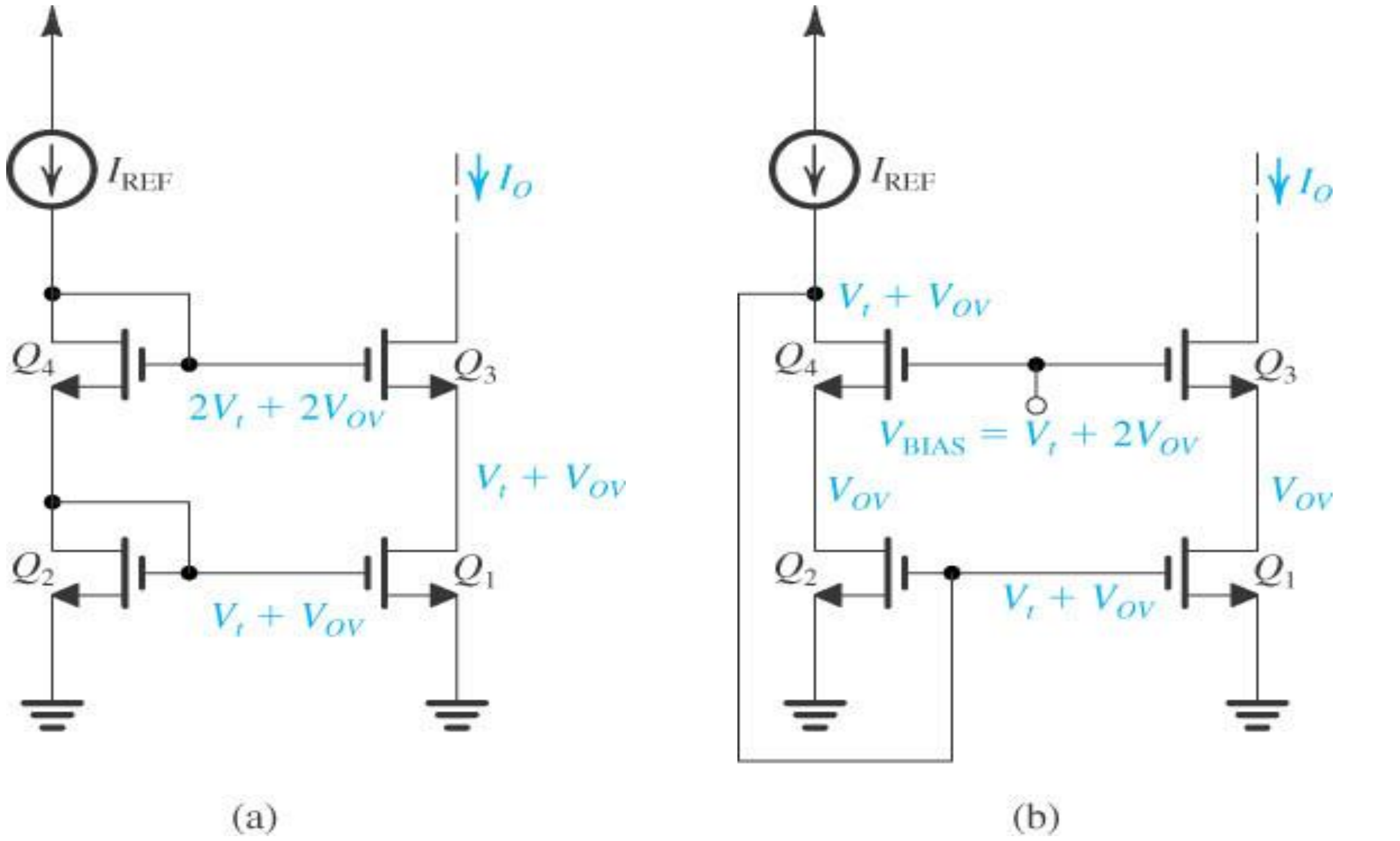
Assume that both differential pairs are operating simultaneously.

$$G_m = g_{m1} = g_{m2} = g_{m3} = g_{m4}$$



Over the remainder of the input CM range, only one of two differential pairs will be operational, and the gain drops to half.

12.2.7 Wide-Swing Current Mirror (Increasing the Output Voltage Range)



For Q4 in saturation, Vds>Vgs-Vt

Vds=Vt, Vgs-Vt=Vov

→Vt>Vov