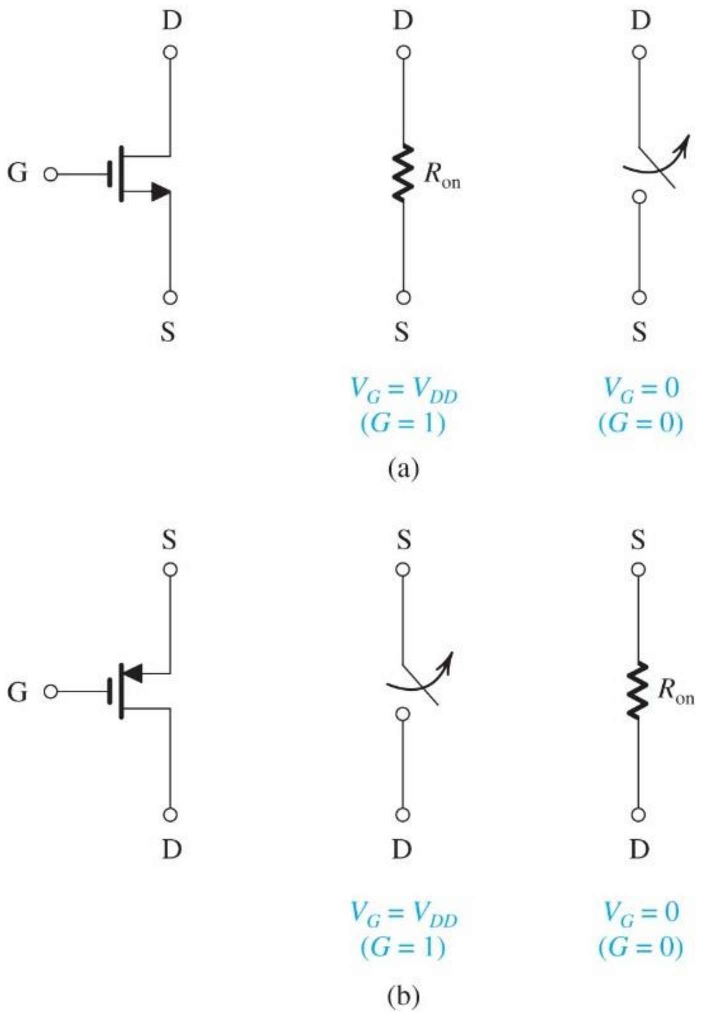
CHAPTER 15 CMOS Digital Logic Circuits

15.1 CMOS Logic-Gate Circuits

15.1.1 Switch-Level Transistor Model

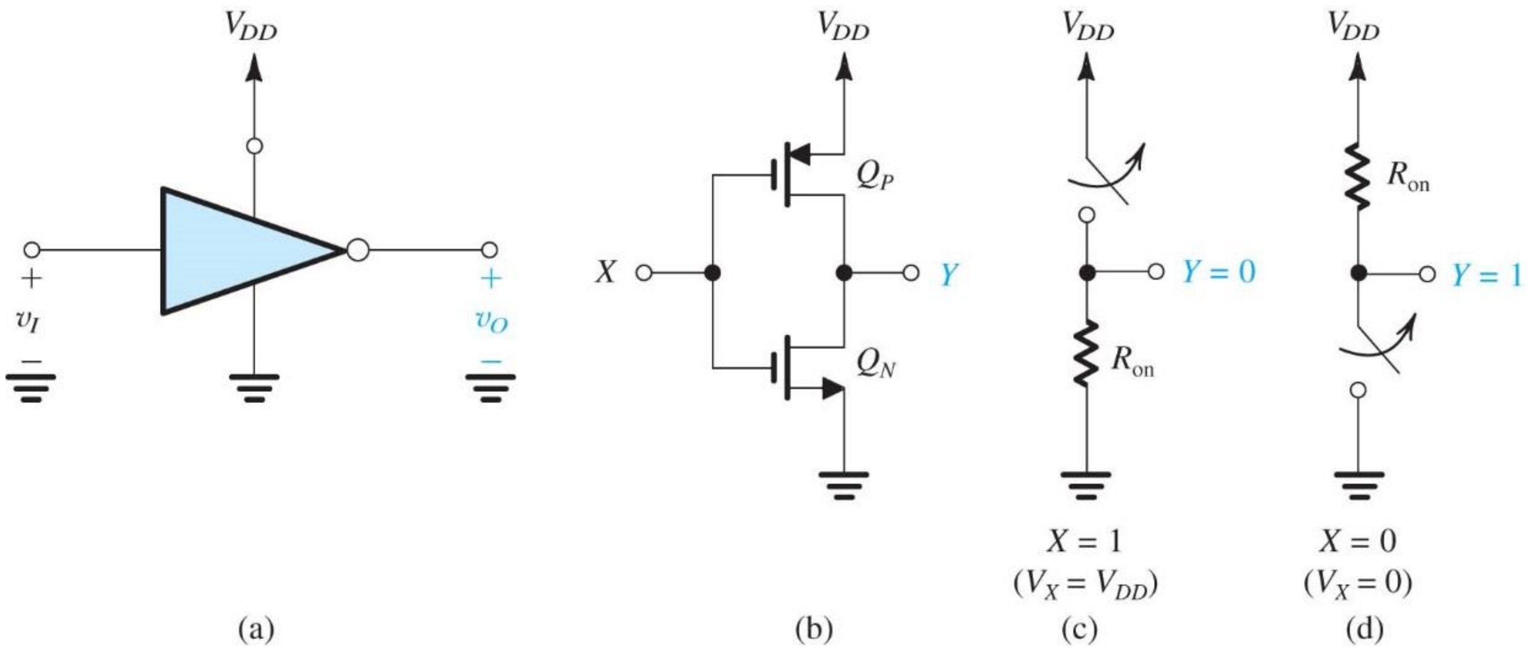


Gate voltage=V_{DD} → Logic "1"
Gate voltage=0 → Logic "0"

Logic "1" at G
→
NMOS on and PMOS off

Logic "0" at G
→
NMOS off and PMOS on

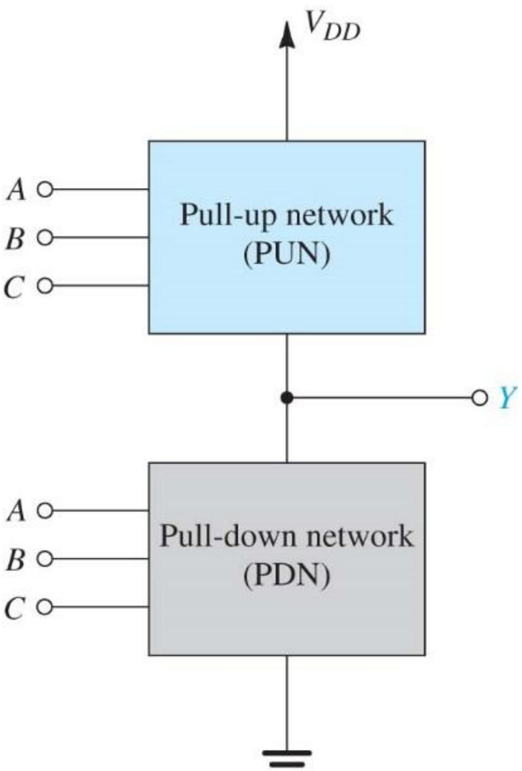
15.1.2 The CMOS Inverter



$$\text{Logic:} \quad Y = \overline{X}$$

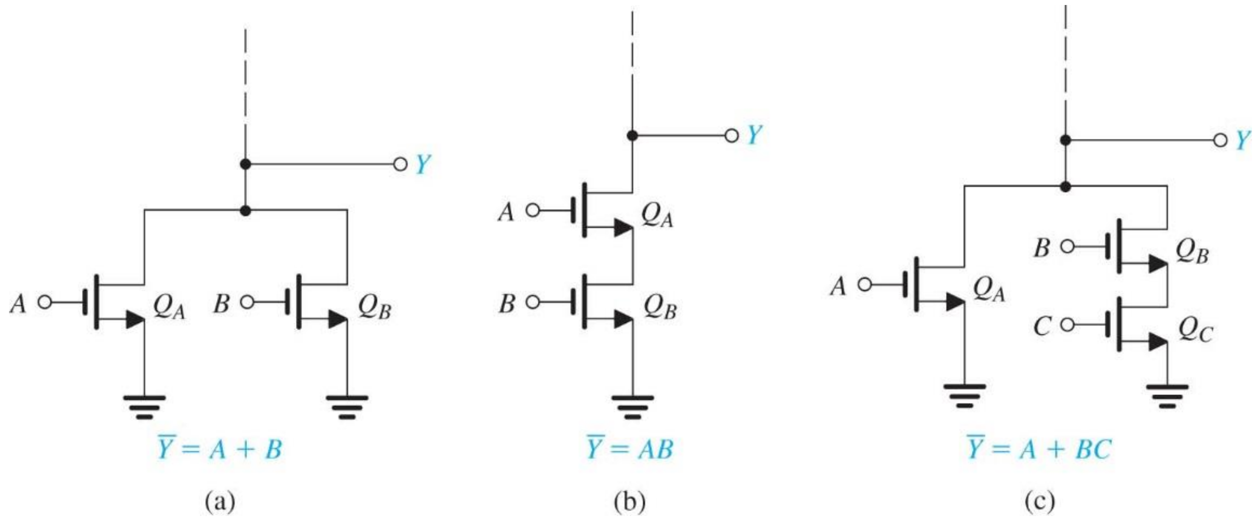
NMOS : Pull Down transistor
PMOS : Pull Up transistor

15.1.3 General Structure of CMOS Logic



CMOS Logic Gate:
Pull Down Network and Pull Up Network

Pull Down Network (PDN)

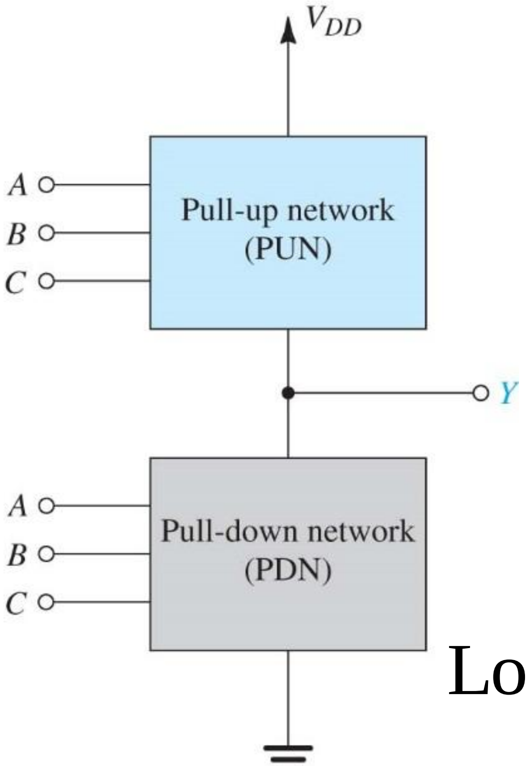


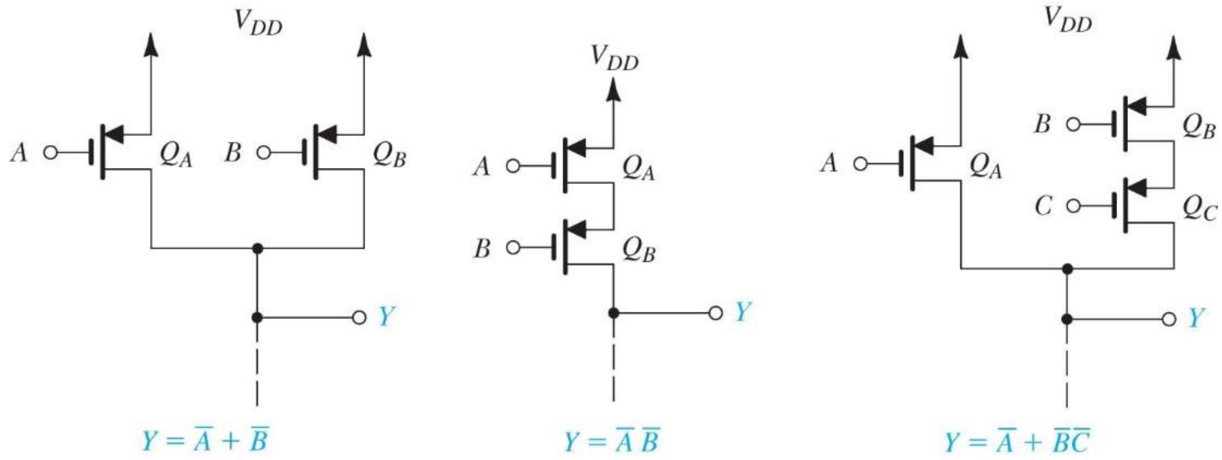
(a) (b) (c)

Logic: $\overline{Y} = A + B$ $\quad$ $\overline{Y} = AB$ $\quad$ $\overline{Y} = A + BC$

or $Y = \overline{A + B}$ $\quad$ or $Y = \overline{AB}$ $\quad$ or $Y = \overline{A + BC}$

Pull UP Network (PUN)

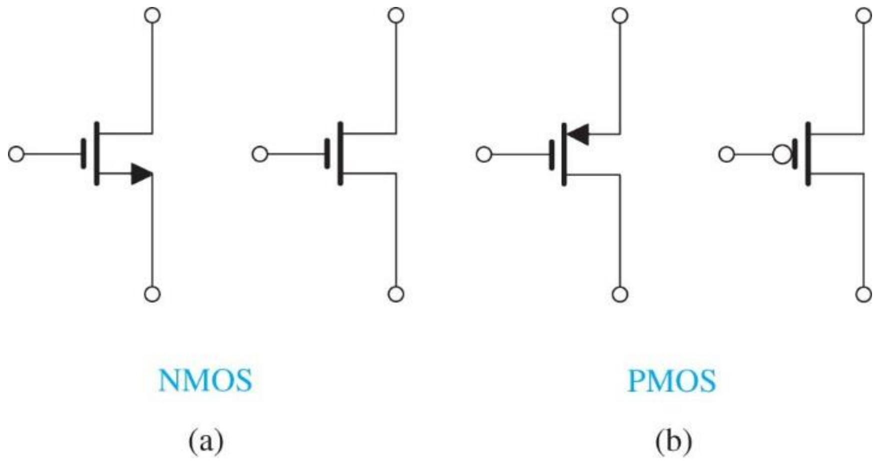


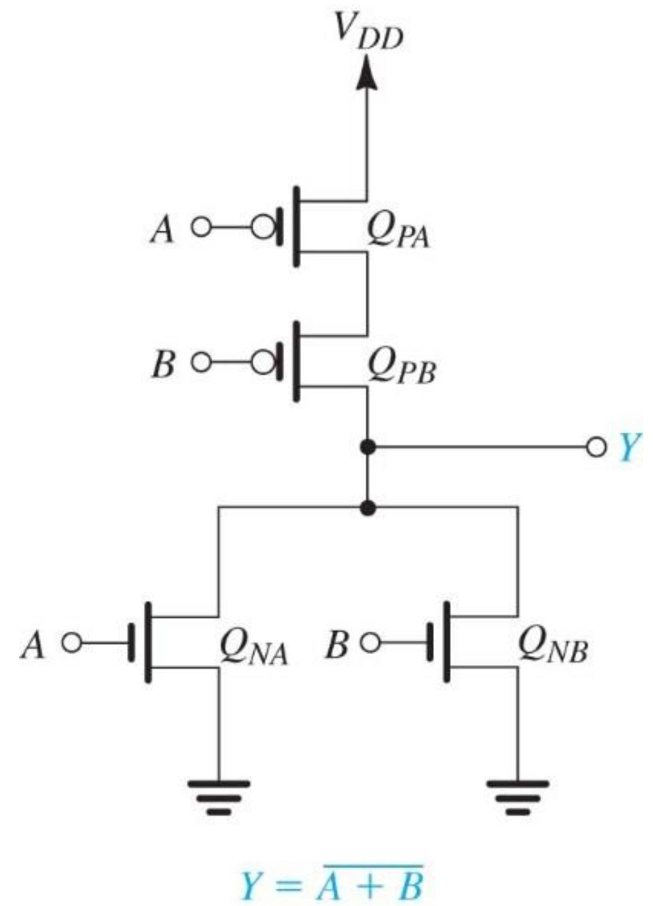


(a) (b) (c)

Logic: $Y = \overline{A} + \overline{B}$ $\quad Y = \overline{A} \cdot \overline{B}$ $\quad Y = \overline{A} + \overline{B} \cdot \overline{C}$

15.1.4 Two-Input NOR Gate





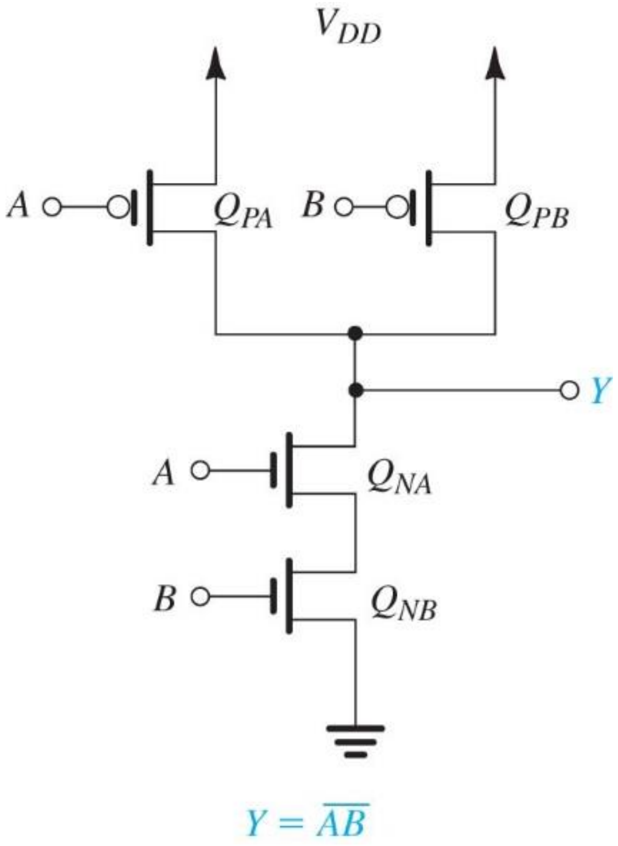
From PDN: $\overline{Y} = A + B$

or $Y = \overline{A + B}$

From PUN: $Y = \overline{A} \cdot \overline{B}$

Logic: $Y = \overline{A + B} = \overline{A} \cdot \overline{B}$

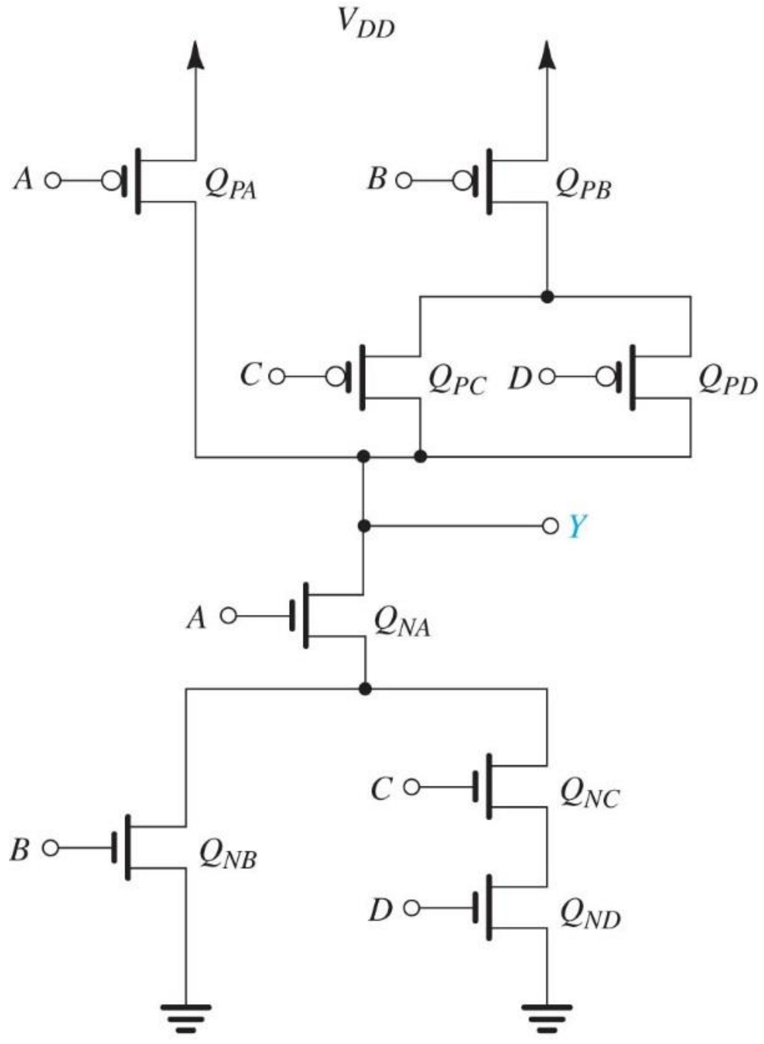
15.1.5 The Two-Input NAND Gate



Logic: $Y = \overline{AB} = \overline{A} + \overline{B}$

15.1.6 A Complex Gate

15.1.7 Obtaining the PUN from the PDN and Vice Versa



$Y = \overline{A(B + CD)}$

From PDN (relatively easy)

$$\text{Logic:} \quad \overline{Y} = A(B + CD)$$

We can use the duality property to obtain PUN from PDN

From PUN (De-Morgan's law)

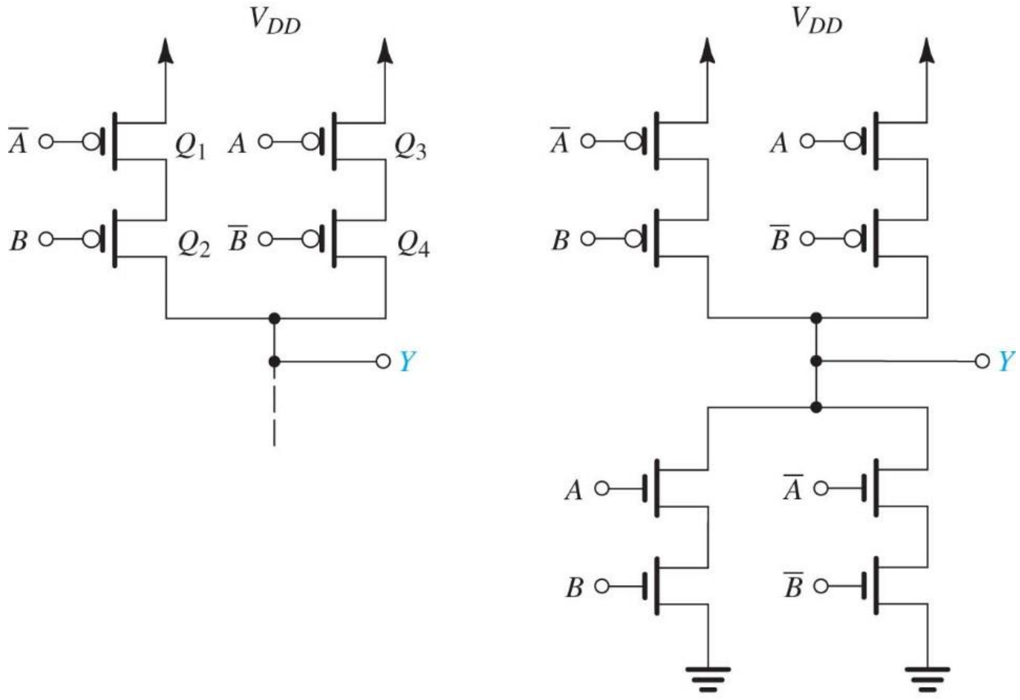
$$\overline{Y} = A(B + CD)$$

$$\Rightarrow$$

$$Y = \overline{A(B + CD)} = \overline{A} + \overline{B + CD}$$

$$= \overline{A} + \overline{B} \cdot \overline{CD} = \overline{A} + \overline{B}(\overline{C} + \overline{D})$$

15.1.8 The Exclusive-OR Function



(a) (b)

From PUN **(relatively easy)**

$$Y = A\cdot\bar{B} + \bar{A}\cdot B$$

From PDN

$$\bar{Y} = AB + \bar{A}\cdot\bar{B}$$

From PUN (De-Morgan's law)

$$Y = A\cdot\bar{B} + \bar{A}\cdot B$$

$$\Rightarrow \bar{Y} = \overline{A\cdot\bar{B} + \bar{A}\cdot B} = \overline{A\cdot\bar{B}}\cdot\overline{\bar{A}\cdot B}$$

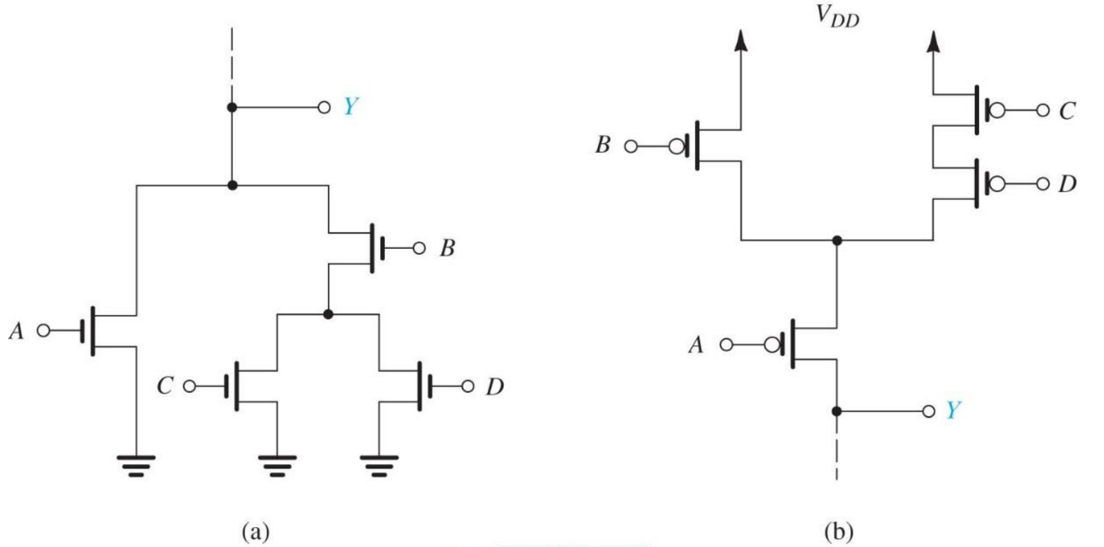
$$= (\bar{A} + B)\cdot(A + \bar{B}) = AB + \bar{A}\cdot\bar{B}$$

1. **Two inverters are required. So, totally 12 transistors are needed.**
2. **PUN and PDN are not dual networks.**
   Two networks are not necessarily duals.

15.1.9 Summary of the Synthesis Method

1. **The PDN can be synthesized by expressing /Y as a function of the un-complemented variables. If the complemented variables appear, additional inverters are needed.**
2. **The PUN can be synthesized by expressing Y as a function of the complemented variables. Then, applying the un-complemented variables to the gates of the PMOS transistors. If the un-complemented variables appear, additional inverters are needed.**
3. **The PDN can be obtained from the UN (vice versa) using the duality property.**

Example 15.1 Synthesize $Y = \overline{A + B(C + D)}$



$Y = \overline{A + B\,(C + D)}$

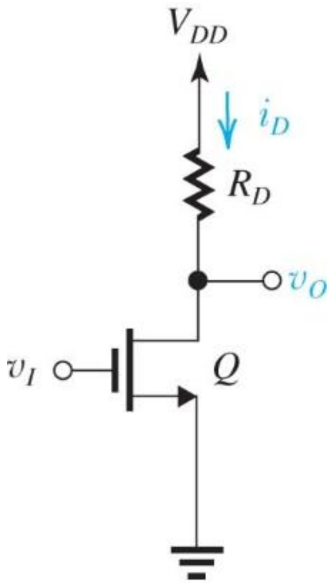
From PDN: $\overline{Y} = A + B(C + D)$

From PUN: $Y = \overline{A + B(C + D)} = \overline{A} \cdot \overline{B(C + D)}$

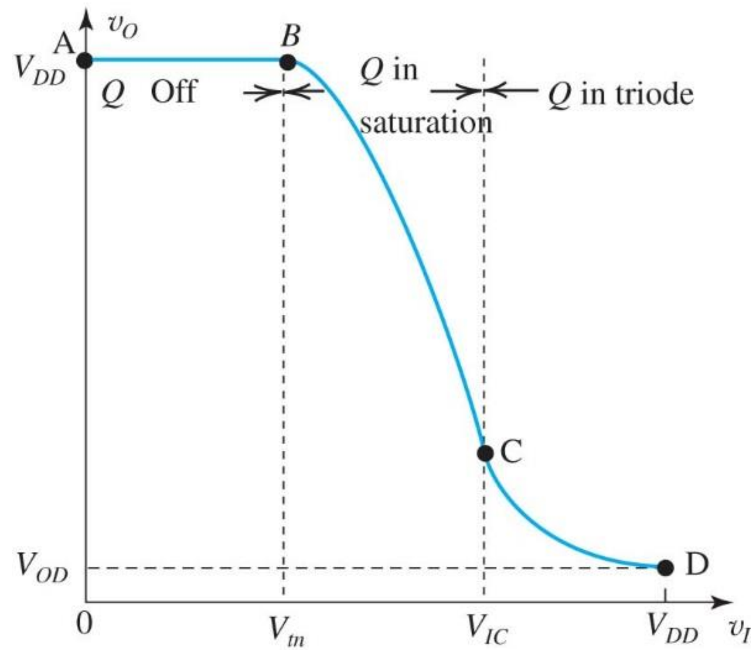
$= \overline{A} \cdot (\overline{B} + \overline{C + D}) = \overline{A} \cdot (\overline{B} + \overline{C} \cdot \overline{D})$

15.2 Digital Logic Inverters

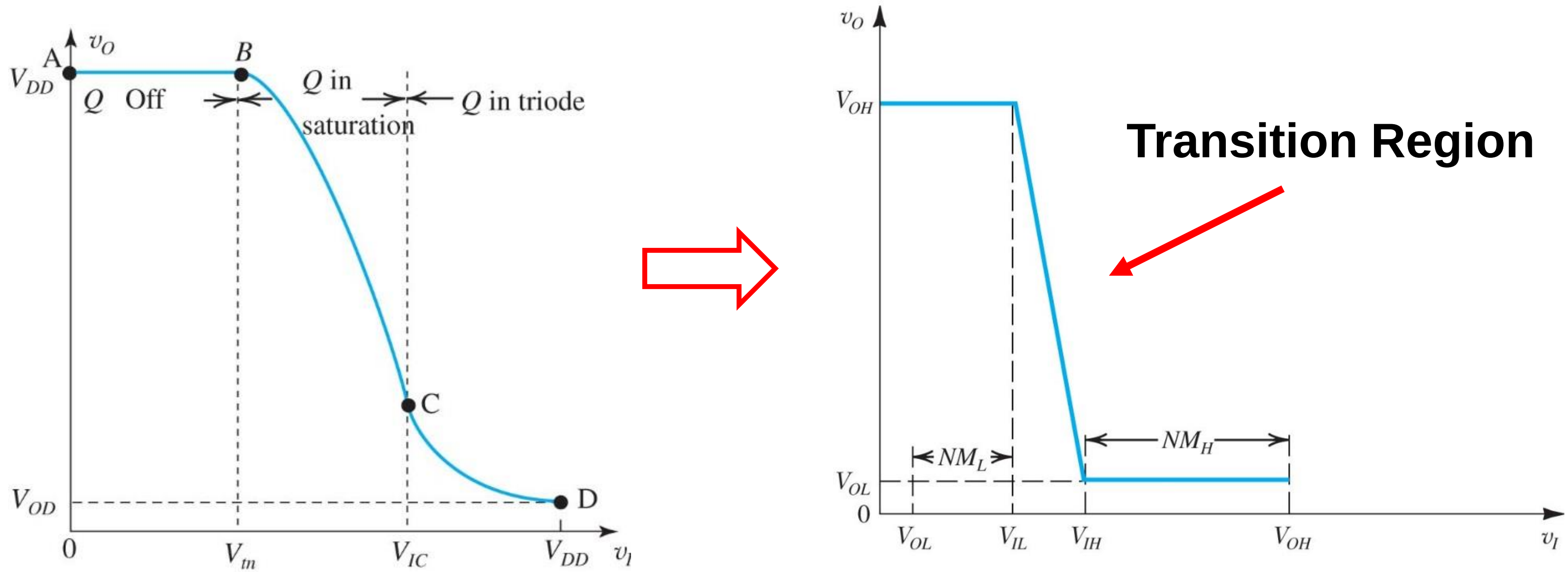
15.2.1 The Voltage Transfer Characteristic (VTC)



(a)



(b)

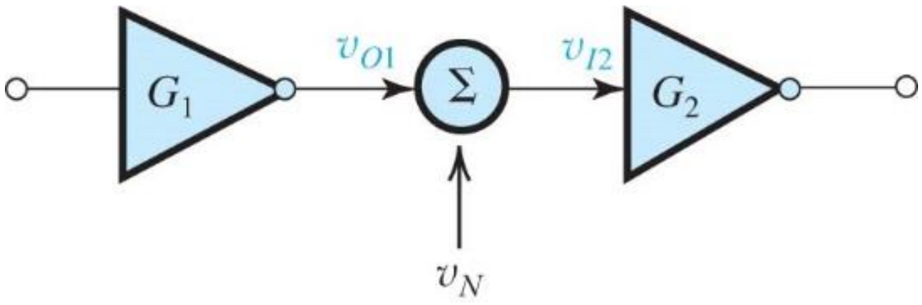


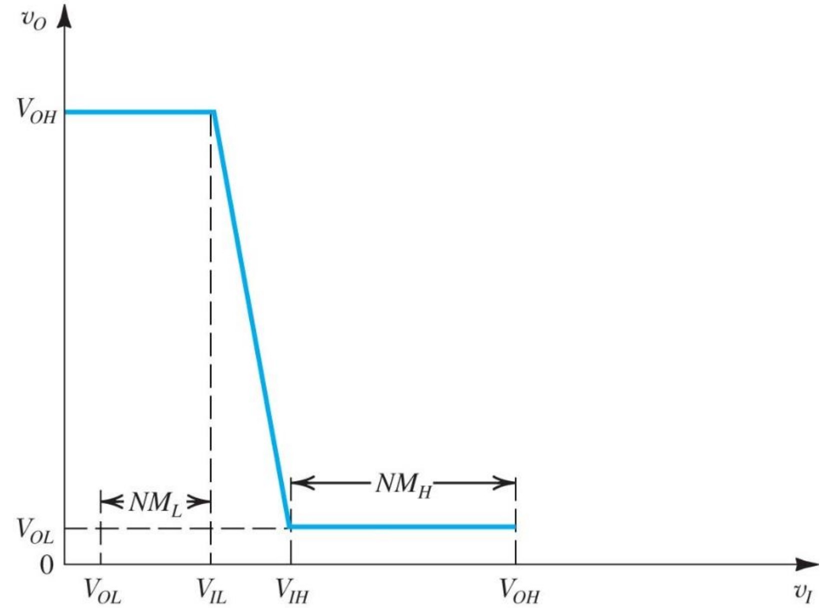
Four parameters (V_{OH}, V_{OL}, V_{IL} , and V_{IH}) to determine the noise margins (N_{MH} and N_{ML})

Table 15.1 Important Parameters of the VTC of the Logic Inverter (Refer to Fig. 15.13)

V_{OL}:	Output low level
V_{OH}:	Output high level
V_{IL}:	Maximum value of input interpreted by the inverter as a logic 0
V_{IH}:	Minimum value of input interpreted by the inverter as a logic 1
NM_L:	Noise margin for low input $= V_{IL} - V_{OL}$
NM_H:	Noise margin for high input $= V_{OH} - V_{IH}$

15.2.2 Noise Margin





Noise voltage v_N is coupled to the interconnection between G1 and G2. The input of G2 becomes

$$v_{I2} = v_{O1} + v_N$$

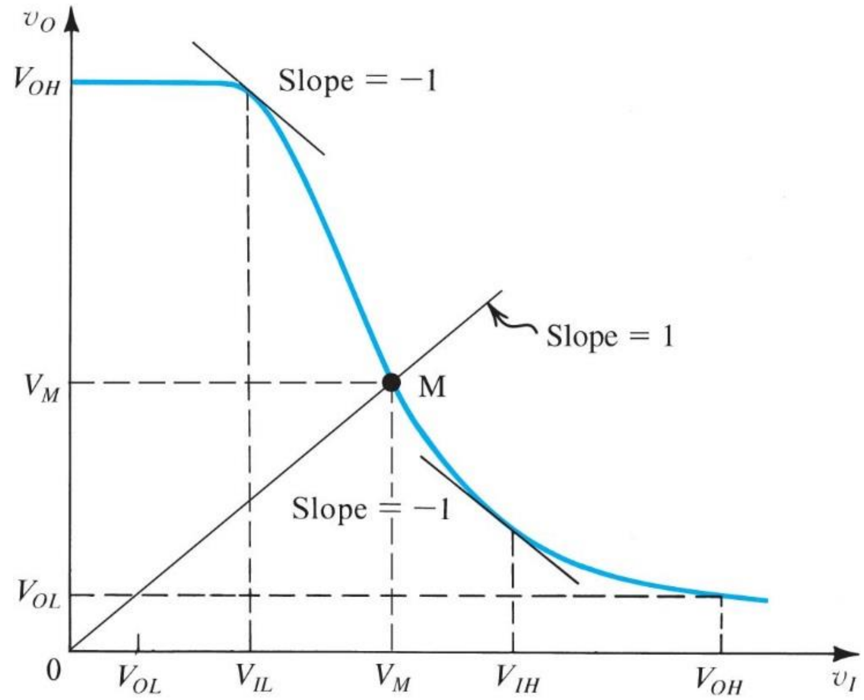
G2 has a noise margin for input low @ $v_{O1} = v_{OL} \,\&\, v_N > 0$

$$v_{I2} = v_{O1} + v_N < v_{IL} \Rightarrow v_N < (v_{IL} - v_{OL}) \equiv NM_L$$

G2 has a noise margin for input high @ $v_{O1} = v_{OH} \,\&\, v_N < 0$

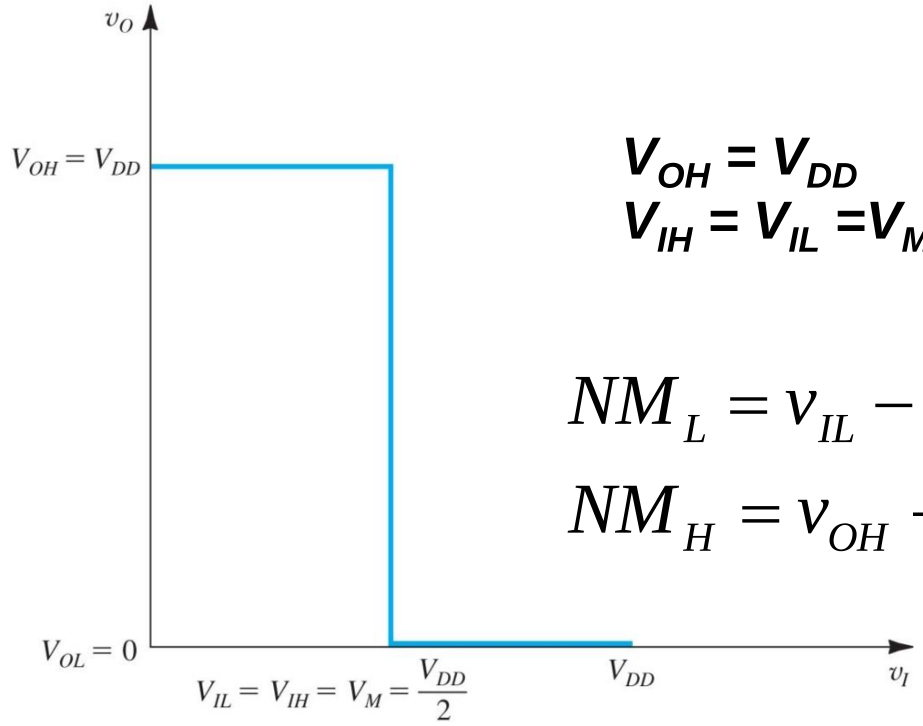
$$v_{I2} = v_{O1} + v_N > v_{IH} \Rightarrow |v_N| < (v_{OH} - v_{IH}) \equiv NM_H$$

V_{IL} and V_{IH} : The VTC points at which the slope is -1



V_M : The M point at which $V_O = V_I$

15.2.3 The Ideal VTC



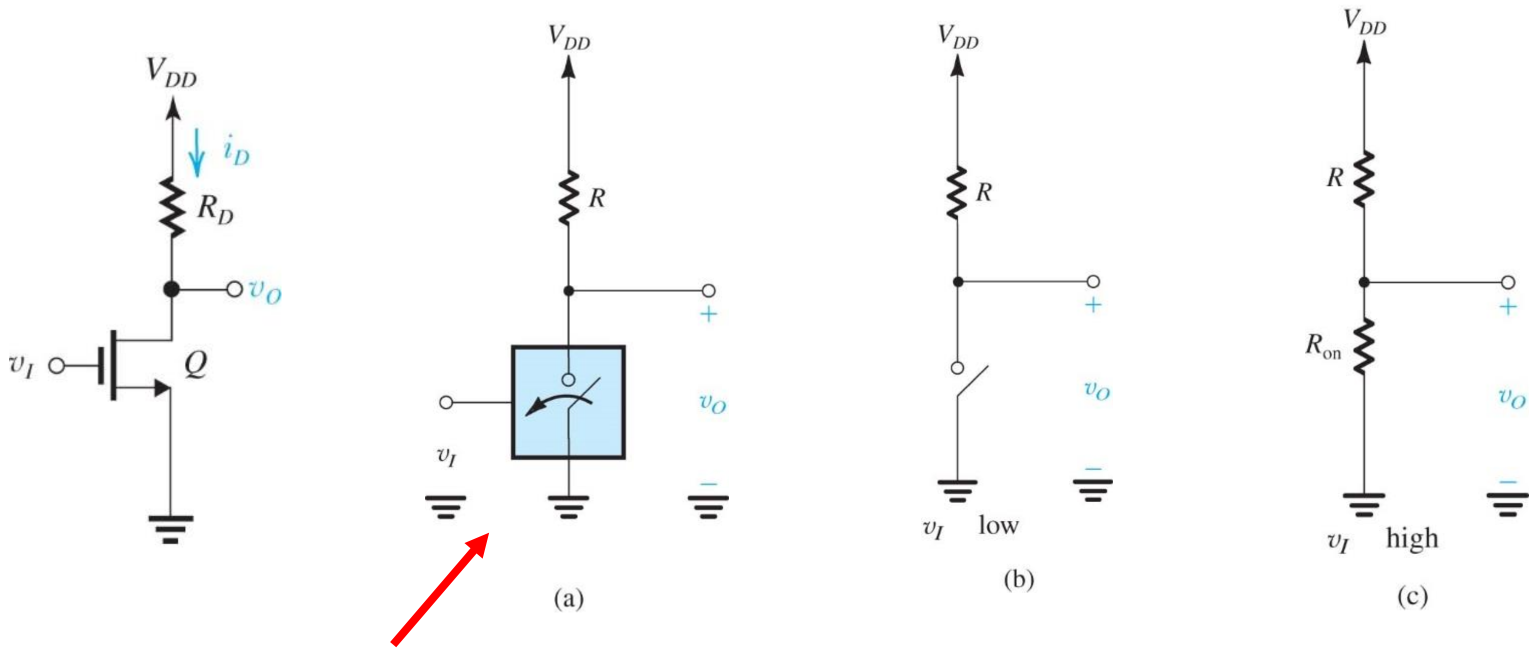
$V_{OH} = V_{DD}$

$V_{IH} = V_{IL} = V_M = V_{DD}/2$

$$NM_L = v_{IL} - v_{OL} = V_{DD} / 2$$

$$NM_H = v_{OH} - v_{IH} = V_{DD} / 2$$

15.2.4 Inverter Implementation



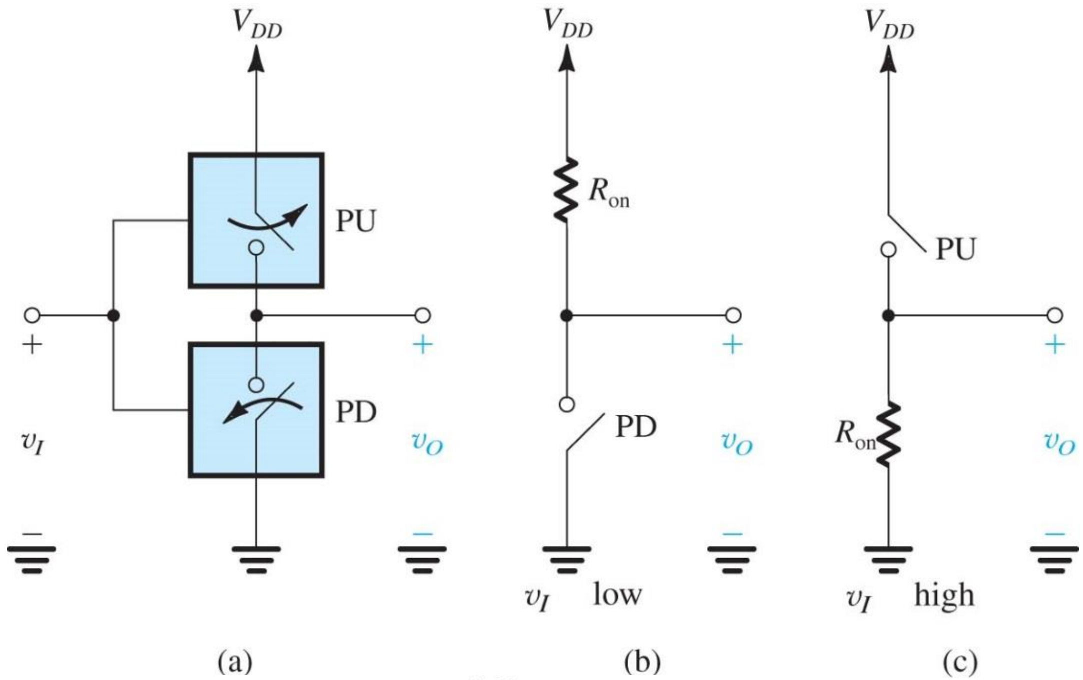
Voltage-controlled Switch:
on-resistance R_{on} is small and off-resistance R_{off} is large

$$\text{When } V_I \text{ is high, } V_{OL} = V_{DD}\frac{R_{on}}{R + R_{on}}$$

$$R_{on} \approx \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)}$$

The logic inverter utilizing two complementary switches.

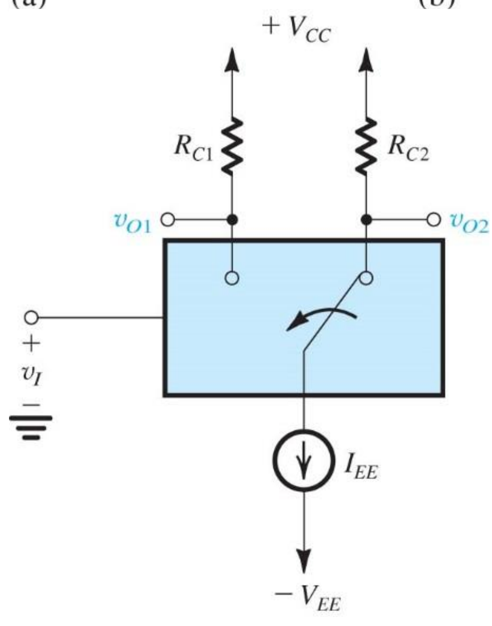
Pull UP (PU) Switch
Pull Down (PD) Switch



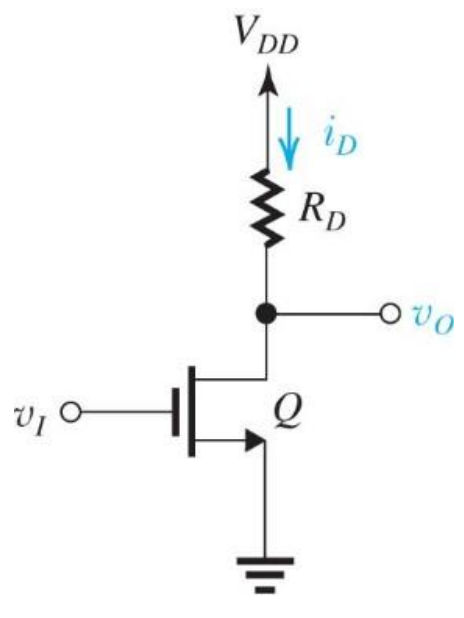
Double-Throw Switch

Current-Steering Logic or
Current-Mode Logic (CML)

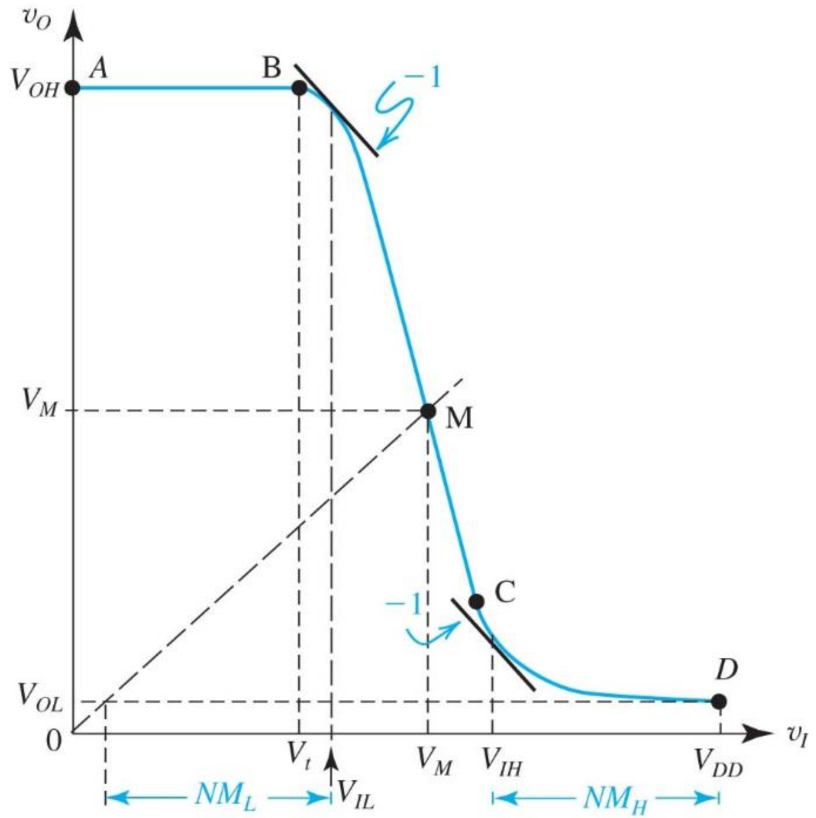
BJT version:
Emitter-Coupled Logic (ECL)



Example 15.2 Resistively Loaded MOS Inverter



(a)



(b)

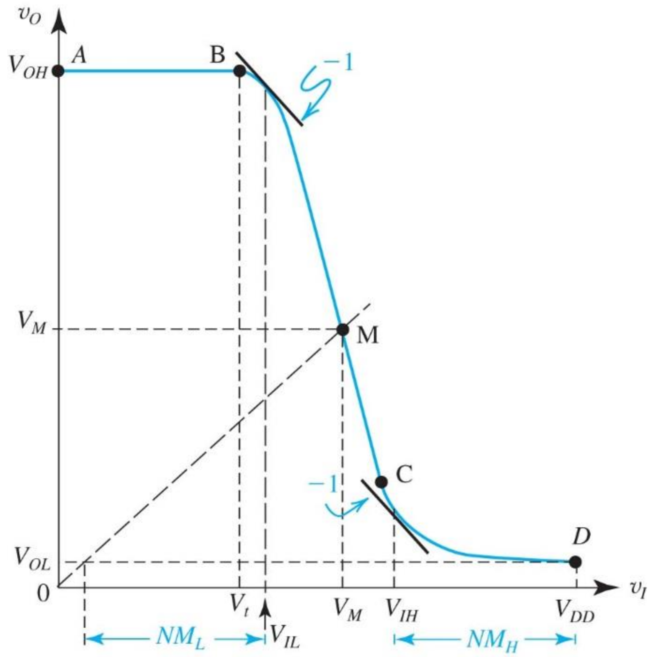
(a) When $V_I < V_t$

$i_D=0$ and $V_{OH}= V_{DD}$

(a) When $V_I > V_t$

Q in Saturation

$$i_D = \frac{\mu_n C_{OX} W}{2L}\left(V_{GS} - V_t\right)^2 \Rightarrow i_D = \frac{k_n}{2}\left(v_I - V_t\right)^2 \quad , \lambda = 0$$



(b)

$$i_D = \frac{k_n}{2}\left(v_I - V_t\right)^2 \quad , \lambda = 0$$

$$v_o = V_{DD} - i_D R = V_{DD} - \frac{k_n R_D}{2}\left(v_I - V_t\right)^2$$

$$k_n R_D = \frac{1}{V_x}$$

$$\Rightarrow v_O = V_{DD} - \frac{1}{2V_x}\left(v_I - V_t\right)^2$$

To determine V_{IL} @ $dv_O/dv_I = -1$

$$\Rightarrow -1 = -\frac{1}{V_x}\left(V_{IL} - V_t\right) \quad \Rightarrow V_{IL} = V_x + V_t$$

(15.12)

To determine V_M @ $v_O = v_I = V_M$

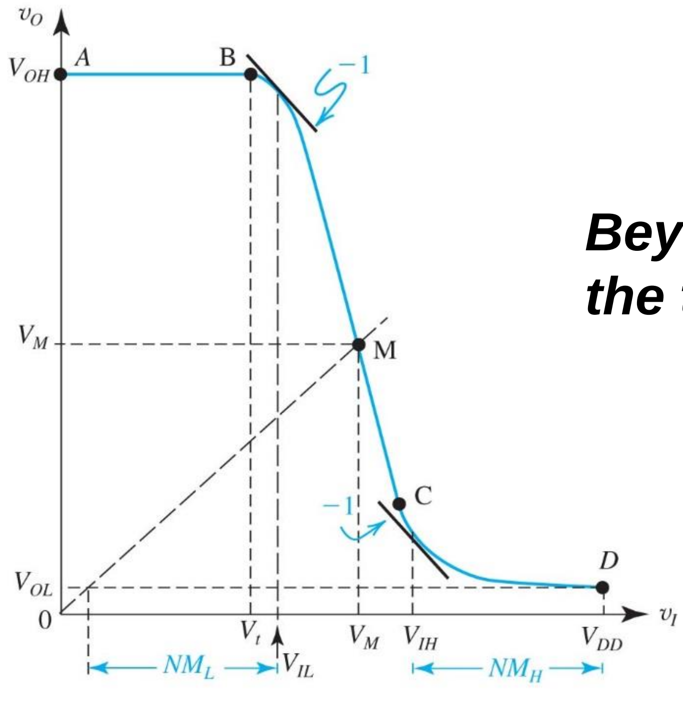
$$\Rightarrow V_M = V_{DD} - \frac{1}{2V_x}\left(V_M - V_t\right)^2 \quad \Rightarrow V_M = V_t + \sqrt{2(V_{DD} - V_t)V_x + V_x^{\ 2}} - V_x$$

(15.14)

The boundary of the saturation-segment BC : Point C

Substituting $v_O = V_{GS} - V_t = v_I - V_t$ ***into*** $v_O = V_{DD} - \frac{1}{2V_x}\left(v_I - V_t\right)^2$

The boundary of the saturation-segment BC : Point C



(b)

$$\Rightarrow V_{OC} = \sqrt{2V_{DD}V_x + V_x^{\ 2}} - V_x$$

$$V_{IC} = V_t + \sqrt{2V_{DD}V_x + V_x^{\ 2}} - V_x$$

Beyond Point C, i.e., segment CD, the transistor in the triode region

$$i_D = k_n\left[\left(V_{GS} - V_t\right)V_{DS} - \frac{1}{2}V_{DS}^{\ 2}\right]$$

$$\Rightarrow i_D = k_n\left[\left(v_I - V_t\right)v_O - \frac{1}{2}v_O^{\ 2}\right]$$

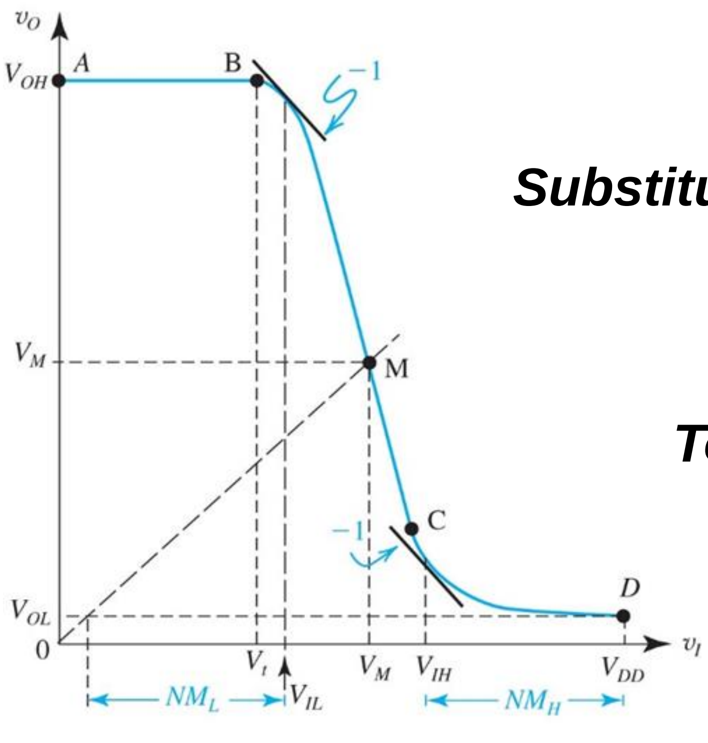
$$v_o = V_{DD} - i_D R \quad \Rightarrow v_O = V_{DD} - \frac{\left(v_I - V_t\right)v_O - \frac{1}{2}v_O^{\ 2}}{V_x} \qquad \textbf{(15.17)}$$

To determine V_{IH} @ $dv_O/dv_I = -1$

$$\Rightarrow V_{IH} = 2v_O - V_x + V_t \qquad \textbf{(15.18)}$$

Substituting (15.18) into (15.17) and $v_I = V_{IH}$

Substituting (15.18) into (15.17) and v_I=V_{IH}



(b)

$$\Rightarrow v_O\,|_{v_I=V_{IH}} = 0.816\sqrt{V_{DD}V_x}$$

Substituting into (15.18)

$$\Rightarrow V_{IH} = V_t + 1.63\sqrt{V_{DD}V_x} - V_x \qquad \textbf{(15.20)}$$

To determine V_{OL} @ v_I= V_{DD}

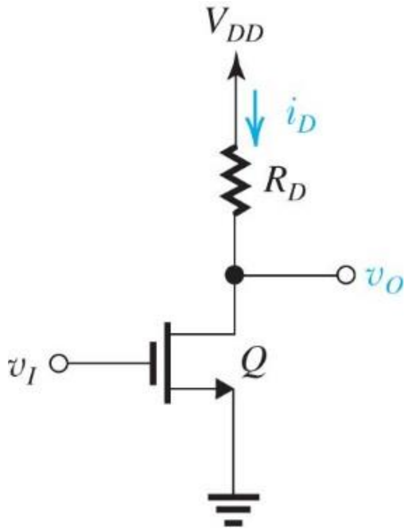
$$v_O = V_{DD} - \frac{1}{V_x}[(v_I - V_t)v_O - \frac{1}{2}v_O^{\,2}]$$

$$\Rightarrow V_{OL} = V_{DD} - \frac{1}{V_x}[(V_{DD} - V_t)V_{OL} - \frac{1}{2}V_{OL}^{\,2}]$$

To determine V_{OL} << V_{DD} -V_t

$$\Rightarrow V_{OL} \cong V_{DD} - \frac{1}{V_x}[(V_{DD} - V_t)V_{OL}]$$

$$\Rightarrow V_{OL} \cong \frac{V_{DD}}{1+(V_{DD} - V_t)/V_x} \qquad \textbf{(15.22)}$$



(a)

It is interesting that V_{OL} *can be found by*

$$V_{OL} \cong V_{DD} \frac{r_{DS}}{R_D + r_{DS}} \quad @\, r_{DS} = R_{on} \cong \frac{1}{k_n (V_{DD} - V_t)}$$

$$\Rightarrow V_{OL} = \frac{V_{DD}}{1 + (V_{DD} - V_t)/V_x}$$

Same as (15.22)

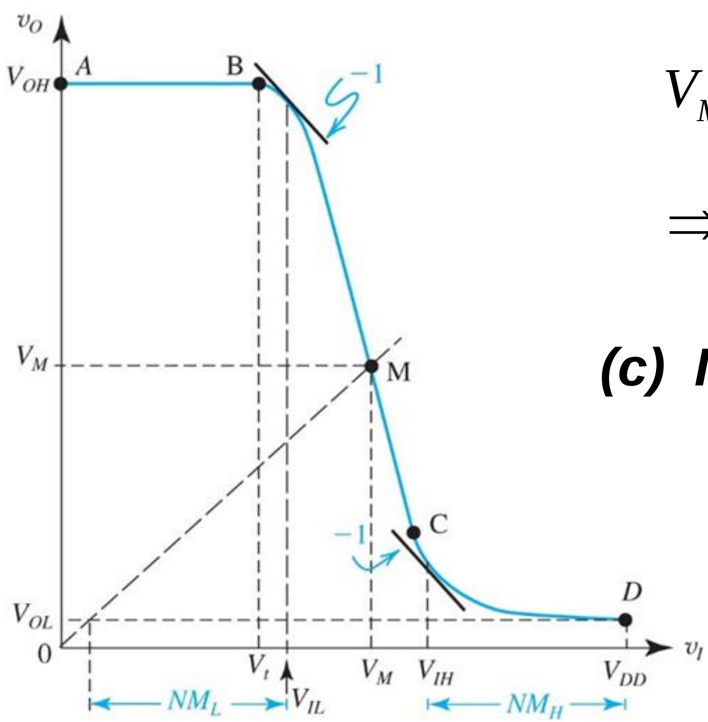
(b) If $V_M = V_{DD}/2$***, what is*** V_x

$$V_M = V_t + \sqrt{2(V_{DD} - V_t)V_x + V_x^{\,2}} - V_x \qquad \textbf{(15.14)}$$

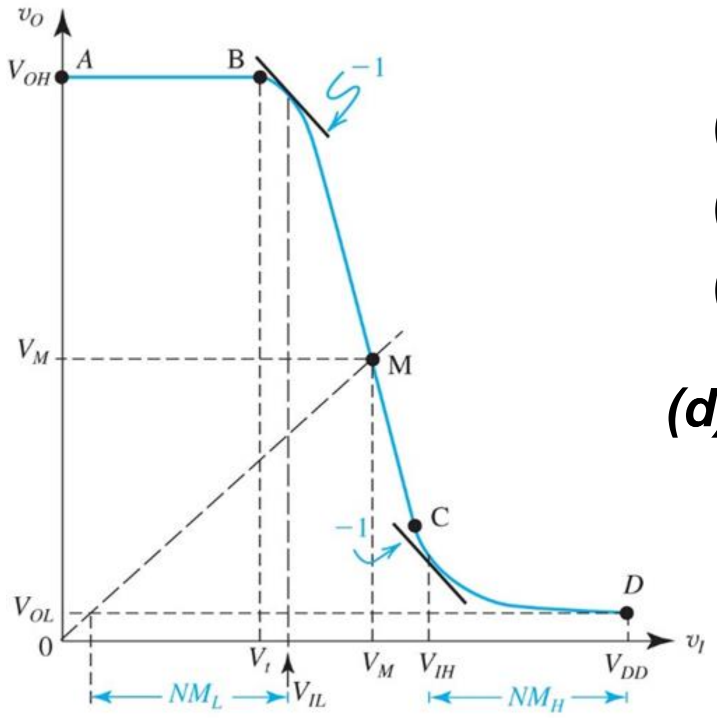
$$\Rightarrow V_x|_{V_M = V_{DD}/2} = \frac{(V_{DD}/2 - V_t)^2}{V_{DD}} \qquad \textbf{(15.25)}$$

(c) If V_{DD}***=1.8V,*** V_t***=0.5V,*** $V_M = V_{DD}/2$

$$V_x|_{V_M = 0.9V} = 0.089V$$



(b)



(b)

V_{OH}= V_{DD}= 1.8V

(15.22) : V_{OL}= 0.12V

(15.12): V_{IL}= 0.59V

(15.20): V_{IH}= 1.06V

NM_L= V_{IL}-V_{OL}= 0.47V

NM_H= V_{OH}-V_{IH}= 0.74V

(d) If k'_n=300uA/V^2 and W/L=1.5, determine R_D

$$k_n R_D = \frac{1}{V_x} \Rightarrow R_D = \frac{1}{k_n V_x} = \frac{1}{k'_n (W/L) V_x}$$

$$= \frac{1}{300 \cdot 10^{-6} \cdot 1.5 \cdot 0.089} = 25k\Omega$$

When v_O=V_{OL}, the current from the supply is

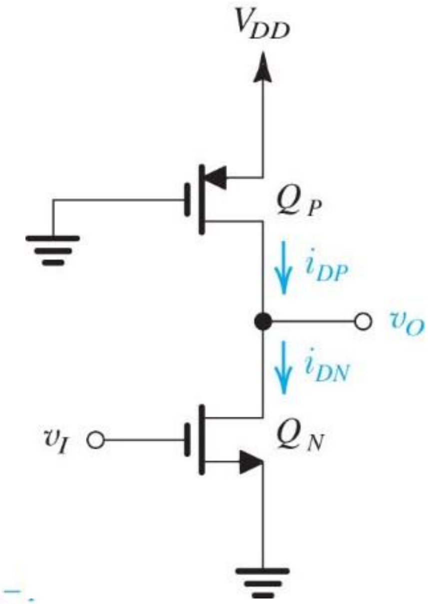
$$I_{DD} = \frac{V_{DD} - V_{OL}}{R_D} = \frac{1.8 - 0.12}{25k} = 67\mu A$$

$$P_D = V_{DD} I_{DD} = 1.8 \times 67 = 121\mu W$$

The inverter spends half of the time in this state:

$$P_{D,average} = P_D / 2 = 60.5\mu W$$

Example 15.3 To eliminate R_D, the pseudo-NMOS Inverter is used.



(a) If V_{DD}=1.8V, V_{tn}=-V_{tp}=V_t=0.4V, k_n=300uA/V², k_n=5k_p,

When $V_I < V_t$

i_{DN}=i_{DP}=0 and V_{OH}= V_{DD}

When $V_I = V_{DD}$

Q_P in Saturation; Q_N in Triode

$$i_{DP} = k_p \left(V_{DD} - V_t\right)^2 / 2$$

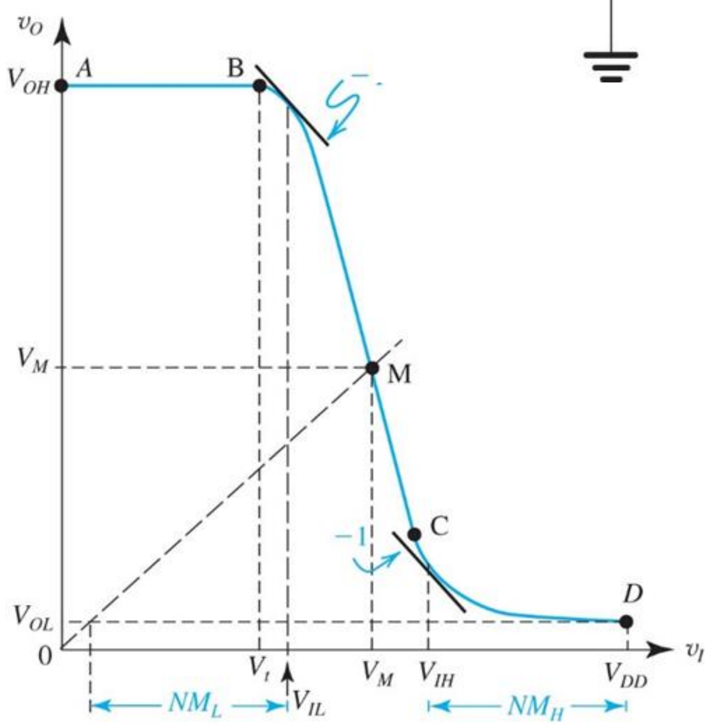
$$i_{DN} = k_n \left[\left(V_{DD} - V_t\right) V_{OL} - \frac{1}{2} V_{OL}^{\ 2} \right] = i_{DP}$$

$$\Rightarrow V_{OL} = \left(V_{DD} - V_t\right)[1 - \sqrt{1 - k_p / k_n}]$$

(b) V_{OH}=V_{DD}=1.8V; V_{OL}=0.15V

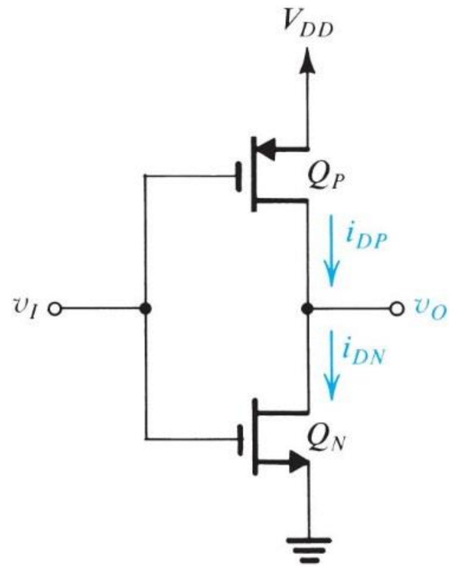
i_{DP}=58.8μA; P_D=$i_{DP}V_{DD}$=105.8μW

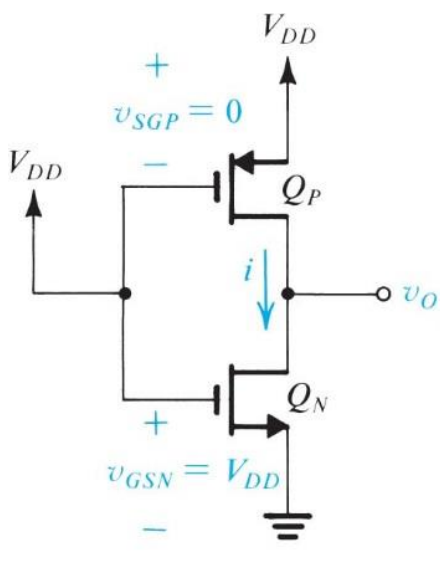
$P_{D,\ average}$=52.9 μW



$$i_{DP} = k_p \left(V_{DD} - V_t\right)^2 / 2 = 300/5(1.8 - 0.4)^2 / 2 = 58.8uA$$

15.3 The CMOS Inverter



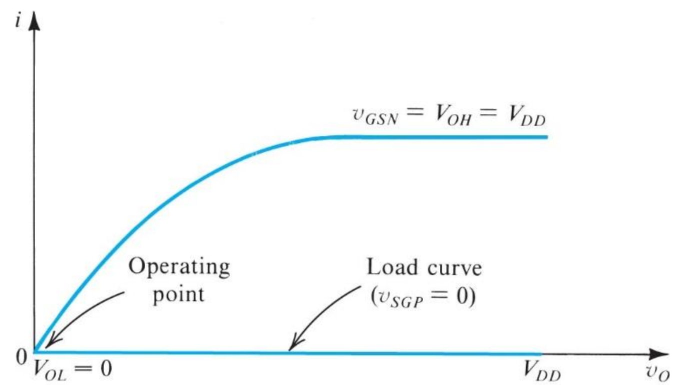


(a)

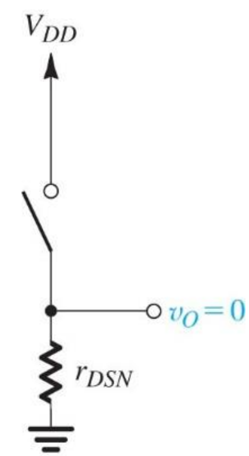
When v_I =0V (Logic 0), V_{OH}= V_{DD}

When v_I =V_{DD} (Logic 1), V_{OL}= 0V

When v_I =V_{DD}, V_{OL}= 0V



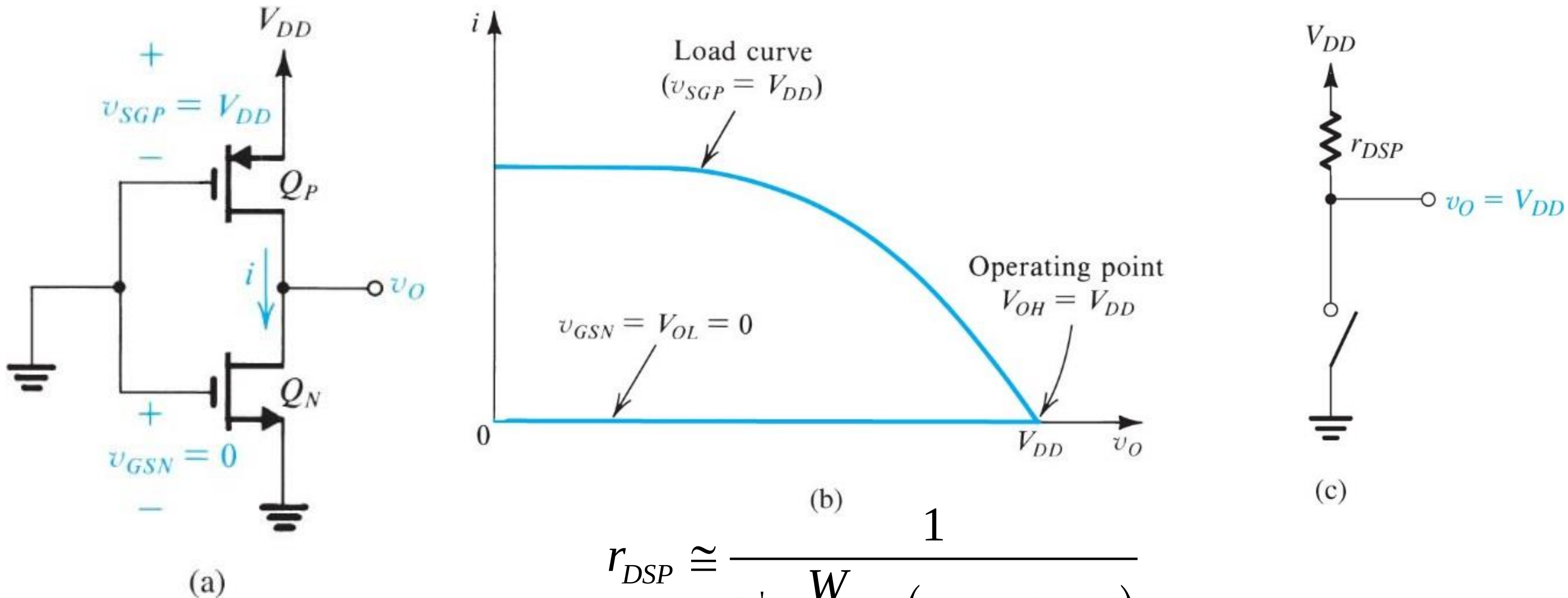
(b)



(c)

$$r_{DSN} \cong \frac{1}{\mu_n C_{ox}(\frac{W}{L})_n (V_{DD} - V_{tn})} = \frac{1}{k'_n(\frac{W}{L})_n (V_{DD} - V_{tn})}$$

When v_I =0V, V_{OH}= V_{DD}



$$r_{DSP} \cong \frac{1}{k'_p (\frac{W}{L})_p \left(V_{DD} - |V_{tp}|\right)}$$

1. The output levels are 0 and V_{DD}

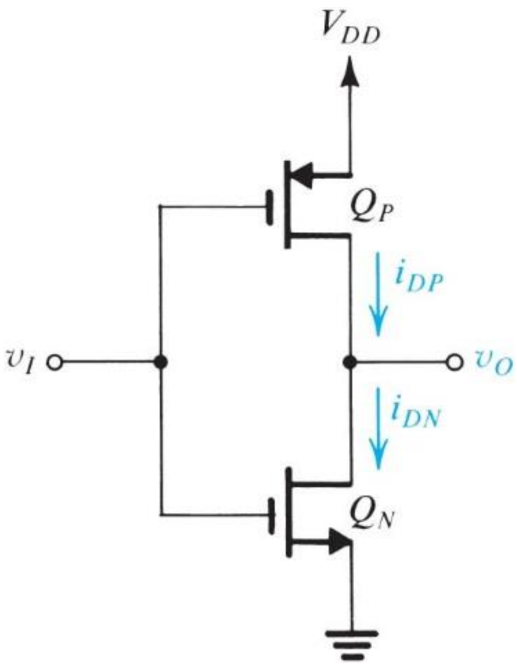
2. Static power=0 in the two states; neglecting the leakage currents

3. The low output resistance makes the inverter less sensitive to the effects of noises and other disturbances

4. The pull-up and pull-down devices provide the high output driving capability in both directions

5. The input resistance of the inverter is high

15.3.2 The VTC



Q_N in Triode, $v_O \le v_I - V_{tn}$

$$i_{DN} = k'_n \left(\frac{W}{L}\right)_n \left[(v_I - V_{tn}) v_O - \frac{1}{2} v_O^2 \right]$$

Q_N in Sat., $v_O \ge v_I - V_{tn}$

$$i_{DN} = k'_n \left(\frac{W}{L}\right)_n (v_I - V_{tn})^2 / 2$$

Q_P in Triode, $v_O \ge v_I + |V_{tp}|$

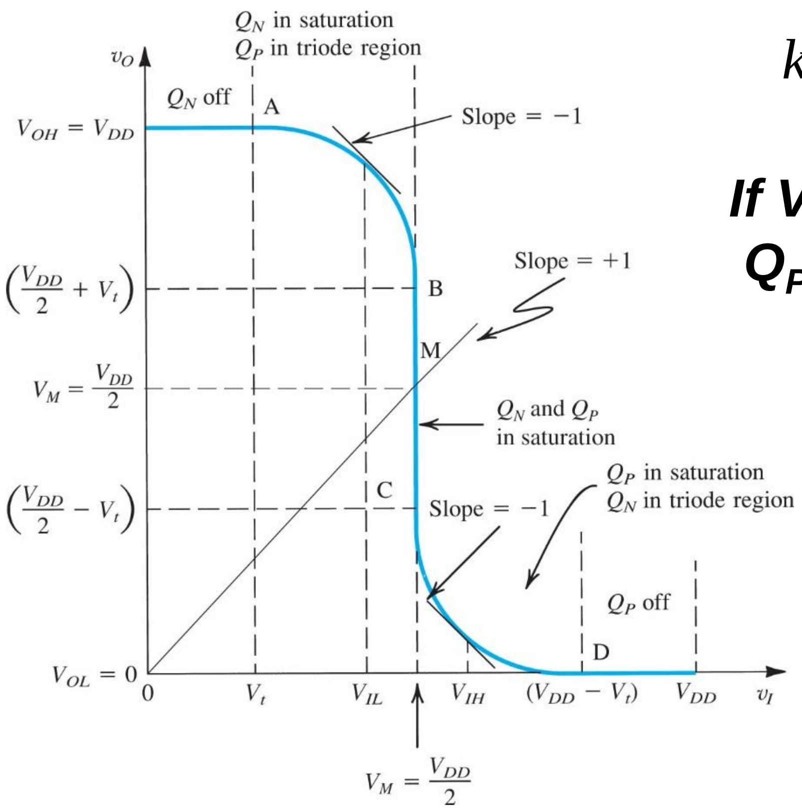
$$i_{DP} = k'_p \left(\frac{W}{L}\right)_p \left[(V_{DD} - v_I - |V_{tp}|)(V_{DD} - v_O) - \frac{1}{2}(V_{DD} - v_O)^2 \right]$$

Q_P in Sat., $v_O \le v_I + |V_{tp}|$

$$i_{DP} = k'_p \left(\frac{W}{L}\right)_p (V_{DD} - v_I - |V_{tp}|)^2 / 2$$

Let Q_p and Q_n have the same channel lengths,

$$k'_n\left(\frac{W}{L}\right)_n = k'_p\left(\frac{W}{L}\right)_p \Rightarrow \frac{\mu_n}{\mu_p} = \frac{W_p}{W_n}$$



If V_{tn}=-V_{tp}=V_t, to determine V_{IH} @ slope=-1
Q_P in Sat. and Q_N in Triode

$$i_{DN} = k'_n\left(\frac{W}{L}\right)_n\left[\left(v_I - V_{tn}\right)v_O - \frac{1}{2}v_O^2\right]$$

$$i_{DP} = k'_p\left(\frac{W}{L}\right)_p\left(V_{DD} - v_I - |V_{tp}|\right)^2 / 2$$

$$\Rightarrow \left(v_I - V_t\right)v_O - \frac{1}{2}v_O^2 = \left(V_{DD} - v_I - V_t\right)^2 / 2$$

(15.33)

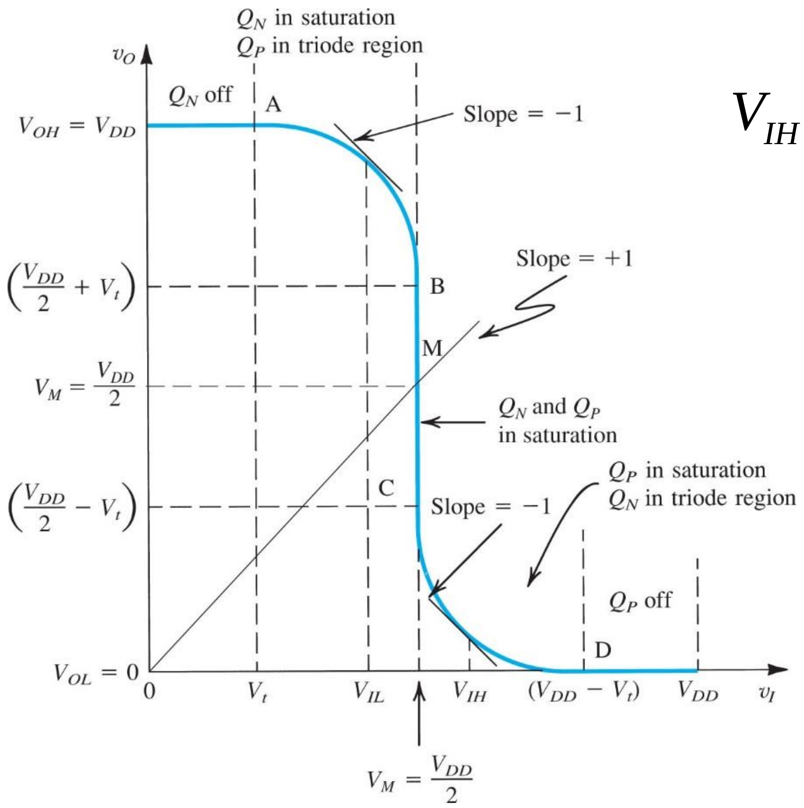
Differentiate (15.33); let v_I=V_{IH} @ slope=-1;

$$\Rightarrow v_O = V_{IH} - \frac{V_{DD}}{2} \quad \textbf{(15.34)}$$

Substituting (15.34) into (15.33); let v_I=V_{IH}

$$\Rightarrow V_{IH} = \frac{5V_{DD} - 2V_t}{8}$$

V_{IL} can be determined similarly. Alternatively, we can use the symmetrical property



$$V_{IH} - \frac{V_{DD}}{2} = \frac{V_{DD}}{2} - V_{IL} \Rightarrow V_{IL} = \frac{3V_{DD} + 2V_t}{8}$$

$$NM_L = V_{IL} - V_{OL} = \frac{3V_{DD} + 2V_t}{8}$$

$$NM_H = V_{OH} - V_{IH} = \frac{3V_{DD} + 2V_t}{8}$$

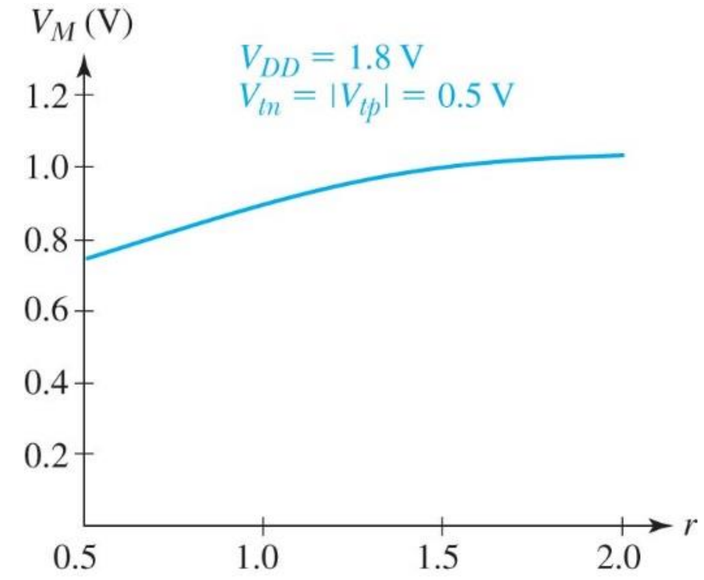
$$(\because V_{IH} = \frac{5V_{DD} - 2V_t}{8})$$

15.3.2 When Q_N and Q_P are not matched

Assume Q_N and Q_P are in Sat., $v_I=V_M$

$$i_{DN} = k'_n \left(\frac{W}{L}\right)_n \left(v_I - V_{tn}\right)^2 / 2$$

$$i_{DP} = k'_p \left(\frac{W}{L}\right)_p \left(V_{DD} - v_I - |V_{tp}|\right)^2 / 2$$



Q_p and Q_n have the same channel lengths,

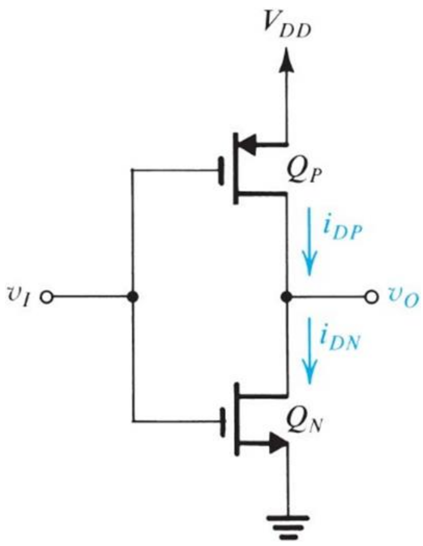
$$i_{DN} = i_{DP} \Rightarrow V_M = \frac{r(V_{DD} - |V_{tp}|) + V_{tn}}{1+r}$$

$$r = \sqrt{\frac{k_p}{k_n}} = \sqrt{\frac{\mu_p W_p}{\mu_n W_n}}$$

For a 0.18um process,

1. ***V_M increases with r, i.e., if $k_p > k_n$, V_M moves to V_{DD}***
2. ***V_M is not a strong function of r. Change r from 1 to 0.5, reduces V_M by 0.13V.***
3. ***For matched case, PMOS's W/L increases → Increase Area But, maximize NM_L and NM_H***

Example 15.4 CMOS Inverter Design



V_{DD}=1.8V, V_{tn}=|V_{tp}|=0.5V, $\mu_n C_{ox}$=300uA/V^2 , μ_n=4μ_p, L=0.18μm, $(W/L)_n$=1.5,

$$V_M = \frac{r(V_{DD} - |V_{tp}|) + V_{tn}}{1+r} \qquad r = \sqrt{\frac{k_p}{k_n}} = \sqrt{\frac{\mu_p W_p}{\mu_n W_n}}$$

Ex. r=1, $V_M = \frac{(1.8-0.5)+0.5}{2} = 0.9V$

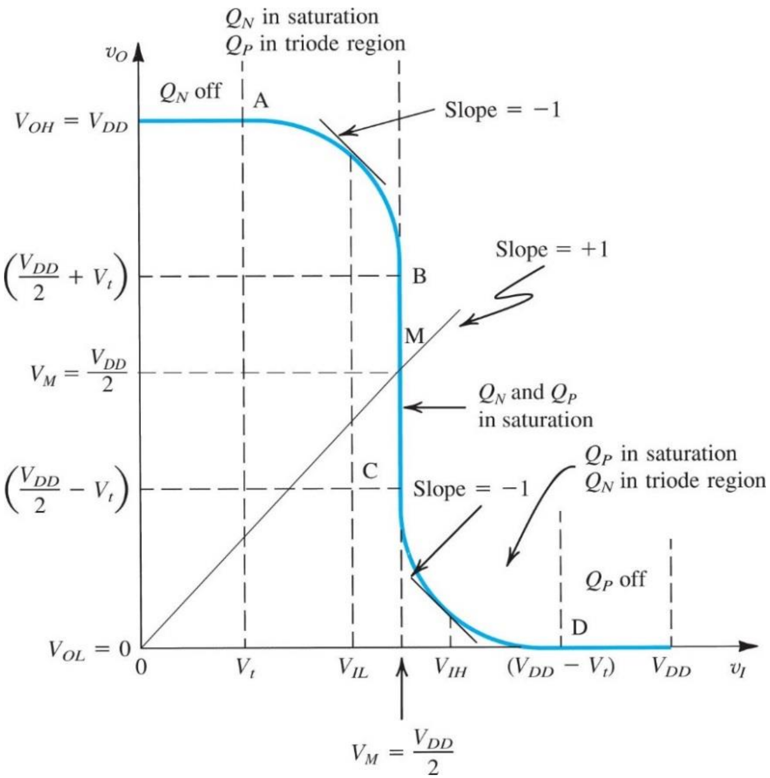
(a) If V_M=0.9V, find W_p=?

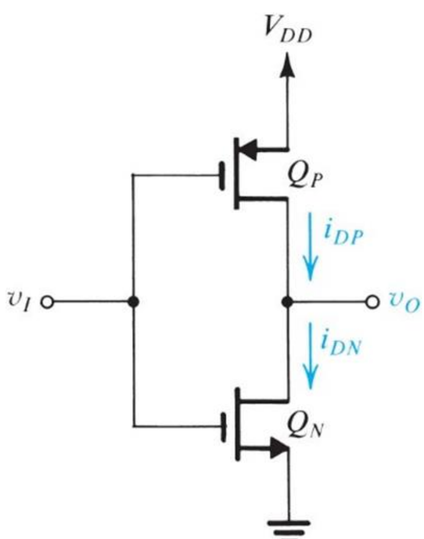
r=1→W_p=4W_n→W_n=0.27 μm and W_p=1.08μm

(b) $V_{IH} = \frac{5V_{DD} - 2V_t}{8} = \frac{5 \cdot 1.8 - 2 \cdot 0.5}{8} = 1V$

$$V_{IL} = \frac{3V_{DD} + 2V_t}{8} = 0.8V$$

$$NM_L = V_{IL} - V_{OL} \;\&\; NM_H = V_{OH} - V_{IH}$$





$$Ideally, NM_H = V_{OH} - V_{IH} = 1.8 - 1 = 0.8V$$

$$NM_L = V_{IL} - V_{OL} = 0.8 - 0 = 0.8V$$

$$\text{at slope=-1}, v_{OL} = V_{IH} - \frac{V_{DD}}{2} \quad \textbf{(15.34)}$$

$$\Rightarrow V_{OL,\max} = 1 - 0.9 = 0.1V$$

$$\text{From symmetry}, V_{OH,\min} = V_{DD} - 0.1 = 1.7V$$

Worst Case

$$NM_H = V_{OH,\min} - V_{IH} = 1.7 - 1 = 0.7V$$

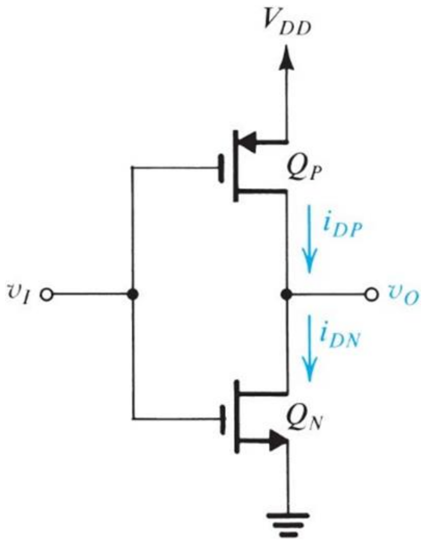
$$NM_L = V_{IL} - V_{OL,\max} = 0.8 - 0.1 = 0.7V$$

(c) Inverter's output resistance at low-state

$$r_{DSN} \cong \frac{1}{\mu_n C_{ox} (\frac{W}{L})_n (V_{DD} - V_{tn})} = \frac{1}{300u \cdot 1.5 \cdot (1.8 - 0.5)} = 1.71k\Omega$$

Since symmetry, Inverter's output resistance at high-state

$$r_{DSP} = r_{DSN} = 1.71k\Omega$$



(d) V_I=V_o=V_M=0.9V, V_{OV}=V_M-V_{tn}=0.4V, Qp and Qn are in sat. λn=λp=0.2 V^{-1}

$$i_{DN} = \mu_n C_{ox} (\frac{W}{L})_n \left(v_I - V_{tn}\right)^2 / 2 = 36\mu A$$

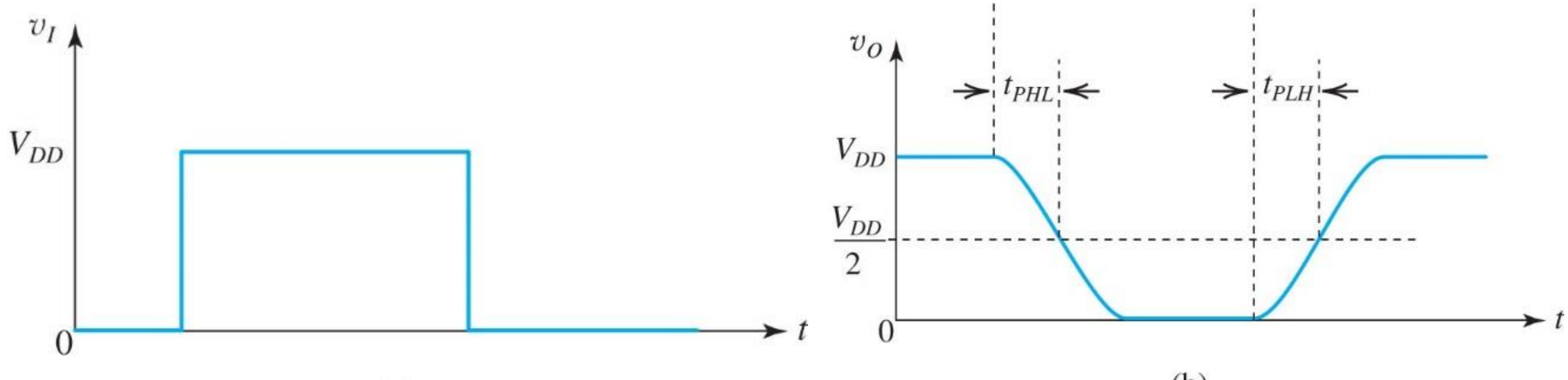
$$g_{mn} = g_{mp} = \frac{I_D}{V_{OV}} = 0.18 mA/V^2$$

$$r_{on} = r_{op} = \frac{1}{\lambda_n I_D} = 139 k\Omega$$

$$A_v = -(g_{mn} + g_{mp})(r_{on} // r_{op}) = -25 V/V$$

15.4 Dynamic Operation of the CMOS Inverter

15.4.1 Propagation Delay



(a) (b)

1. The output signal is not longer an ideal pulse.
2. There is a time delay between the edges of the input and the corresponding inverter output. For example, t_{PHL} and t_{PLH}.

The inverter's Propagation Delay is defined as $t_P = \frac{t_{PHL} + t_{PLH}}{2}$

To consider the inverter's maximum switching frequency;

i.e., the minimum period for each cycle is

$$T_{\min} = t_{PHL} + t_{PLH} = 2t_P \qquad f_{\max} = \frac{1}{T_{\min}} = \frac{1}{2t_P}$$

The propagation delay is owing to the time to charge and discharge the various capacitances in the circuit.

1. ***A fundamental rule to analyze the dynamic operation of a circuit***

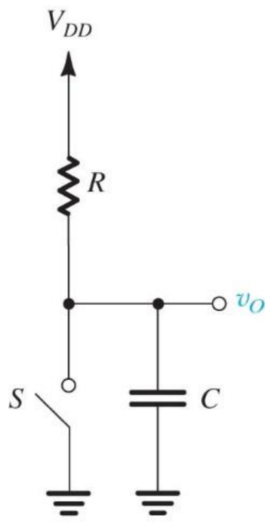
$$I\Delta t = \Delta Q = C\Delta V$$

2. To consider a step input for a single-time-constant (STC) circuit,

$$y(t) = Y_{\infty} - (Y_{\infty} - Y_{0+})e^{-t/\tau}$$

where Y_{∞} is the final value, Y_{o+} is the initial value, and τ is the time constant of an STC circuit.

Example 15.5 Calculating the propagation delay of a simple Inverter

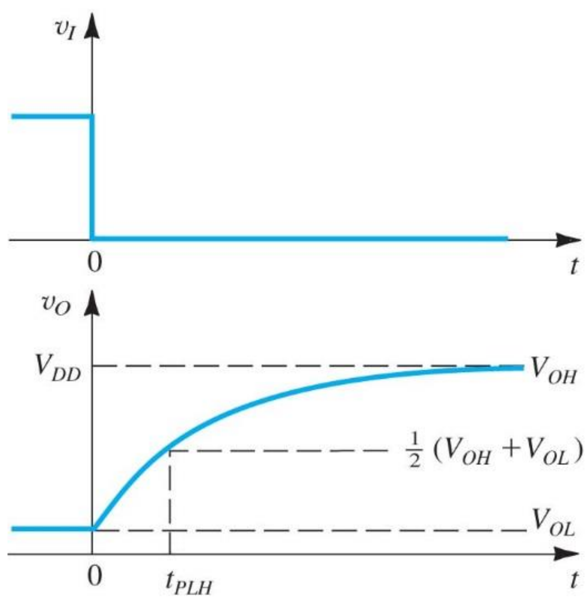


(a)

$$v_o(t) = V_{OH} - (V_{OH} - V_{OL})e^{-t/\tau} \ , \tau = RC$$

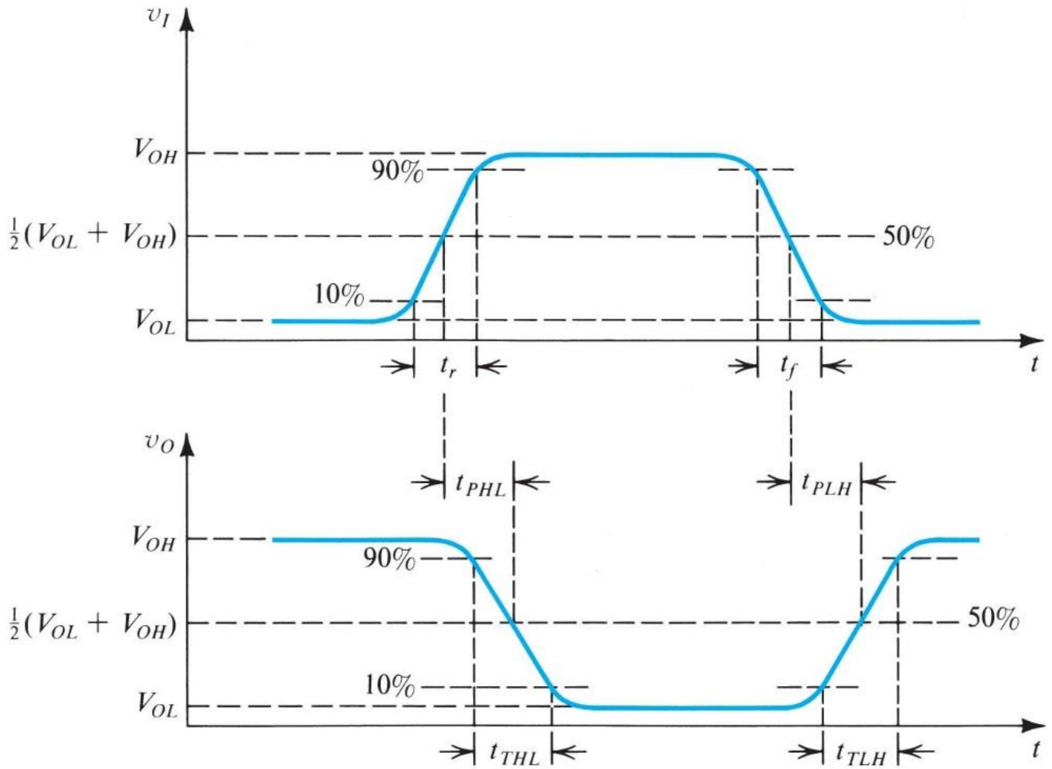
$$v_o(t_{PLH}) = V_{OH} - (V_{OH} - V_{OL})e^{-t_{PLH}/\tau} = \frac{V_{OH} + V_{OL}}{2}$$

$$\Rightarrow t_{PLH} = \tau \ln 2 = 0.69\tau = 0.69RC$$



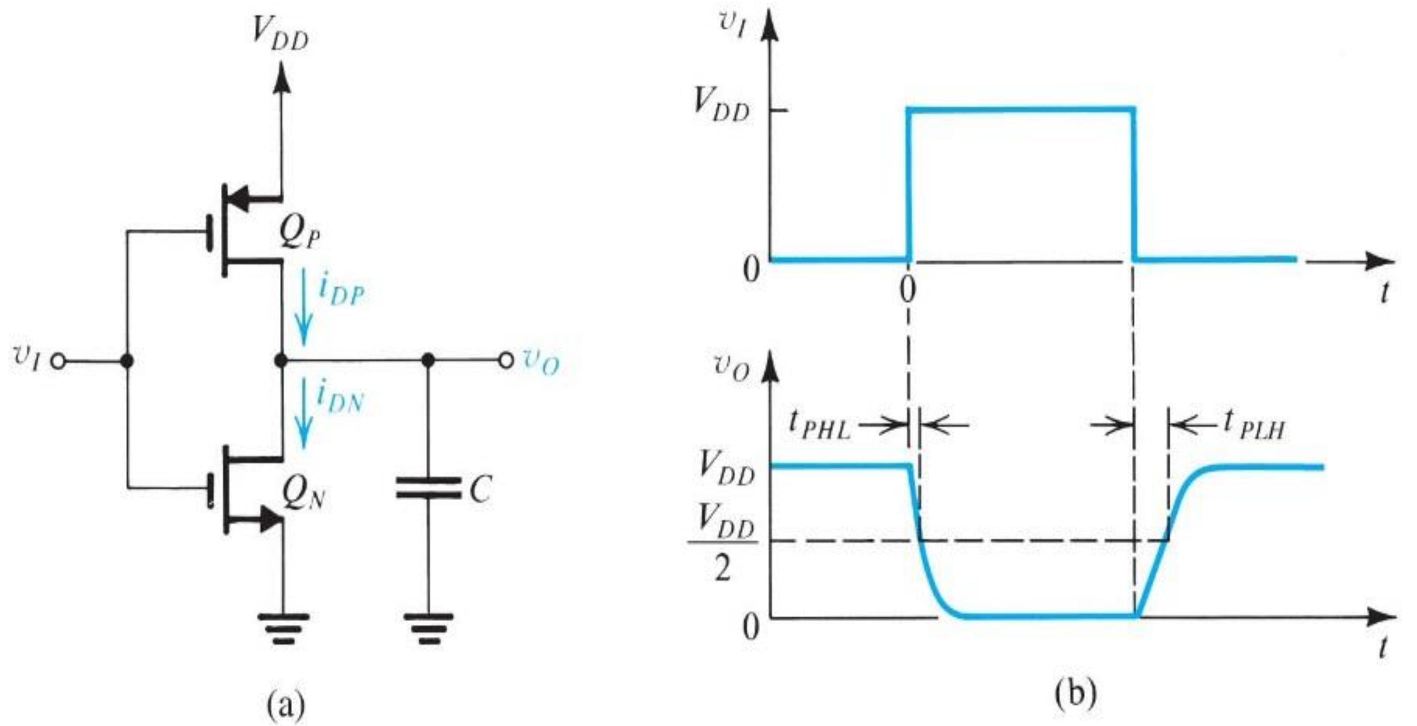
(b)

The propagation delay and the transition time of the logic Inverter

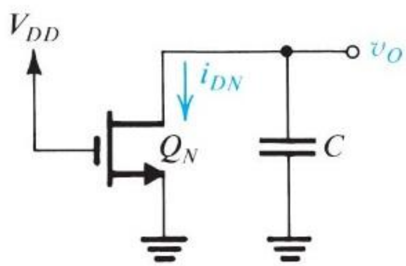


1. ***t_r rise time: The time from 10% to 90% of the input swing (V_{OH}-V_{OL})***
2. ***t_f : fall time: The time from 90% to 10% of the input swing (V_{OH}-V_{OL})***
3. ***t_{PHL} , t_{PLH} : The time from V_I= (V_{OL}+V_{OH})/2 to V_O= (V_{OL}+V_{OH})/2***
4. ***t_{THL} and t_{TLH}: The time from 10% to 90% of the output swing (V_{OH}-V_{OL})***

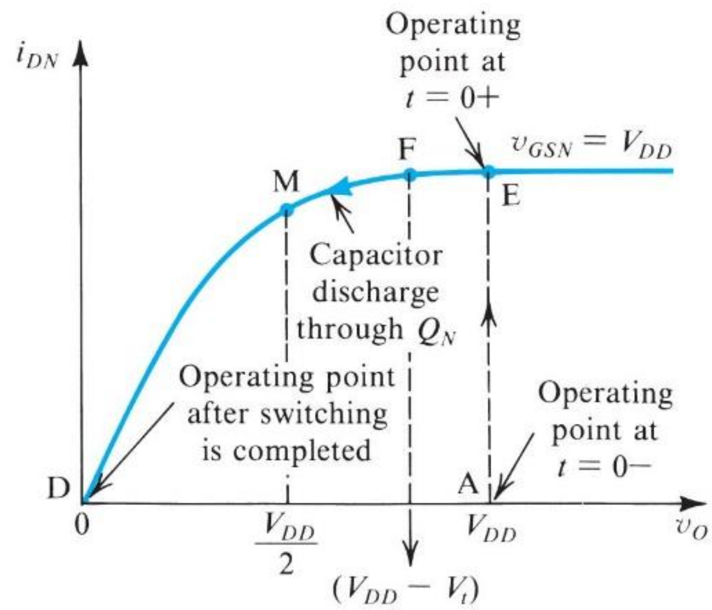
15.4.2 Determining the Propagation Delay of the CMOS Inverter



1. ***Cap. C: consider all the parasitic cap. of Q_N and Q_P, the interconnection cap. and the input cap. of the next logics.***
2. ***To calculate t_{PHL}, t_{PLH}, and t_P***



(c)



(d)

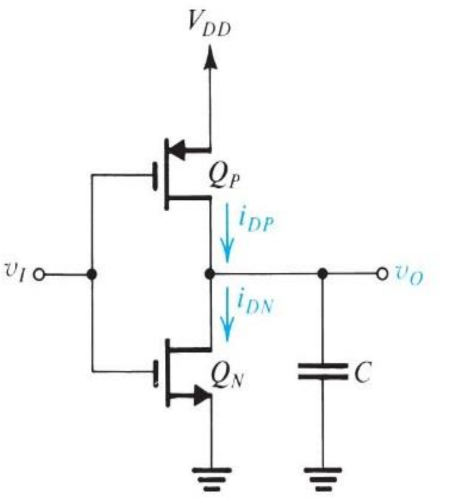
1. ***Let the initial voltage $v_O = V_{DD}$***
2. ***At t=0, $v_I = V_{DD}$ → Q_N on and Q_P off.***
3. ***i_{DN} will discharge C. It operates from E → F → M → D.***
4. ***E-F: Q_N is in saturation.***
5. ***F-M-D: Q_N is in triode.***
6. ***E-M: Assume an average current I_{ave}***

$$I_{ave} = [i_{DN}(E) + i_{DN}(M)]/2, \; i_{DN}(E) = k'_n \left(\frac{W}{L}\right)_n \left(V_{DD} - V_{tn}\right)^2 / 2$$

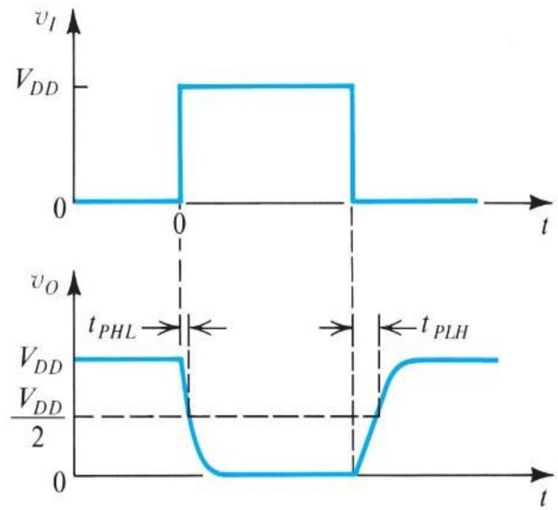
$$i_{DN}(M) = k'_n \left(\frac{W}{L}\right)_n \left[\left(V_{DD} - V_{tn}\right) V_{DD}/2 - \frac{1}{2}(V_{DD}/2)^2\right]$$

$$I_{ave} = \frac{1}{2} k'_n (\frac{W}{L})_n [(V_{DD} - V_{tn})^2 / 2 + (V_{DD} - V_{tn}) V_{DD} / 2 - \frac{1}{2} (V_{DD} / 2)^2]$$

$$= \frac{k'_n (\frac{W}{L})_n V_{DD}{}^2}{4} [(1 - \frac{V_{tn}}{V_{DD}})^2 + (1 - \frac{V_{tn}}{V_{DD}}) - \frac{1}{4}] = \frac{k'_n (\frac{W}{L})_n V_{DD}{}^2}{4} [\frac{7}{4} - \frac{3V_{tn}}{V_{DD}} + (\frac{V_{tn}}{V_{DD}})^2] = \frac{k'_n (\frac{W}{L})_n V_{DD}{}^2}{2\alpha_n}$$



(a)



(b)

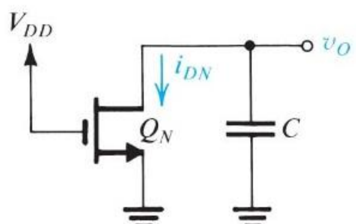
$$\alpha_n = 2 / [\frac{7}{4} - \frac{3V_{tn}}{V_{DD}} + (\frac{V_{tn}}{V_{DD}})^2]$$

$$I_{ave} t_{PHL} = C[V_{DD} - V_{DD} / 2]$$

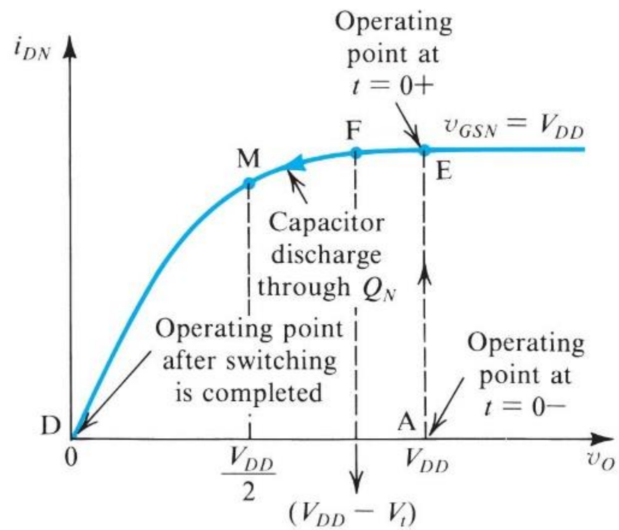
$$t_{PHL} = \frac{CV_{DD}}{2I_{ave}}$$

$$\Rightarrow$$

$$t_{PHL} = \frac{\alpha_n C}{k'_n (W / L)_n V_{DD}}$$



(c)



(d)

$$t_{PLH} = \frac{\alpha_p C}{k'_p (W / L)_p V_{DD}}$$

$$\alpha_p = 2 / [\frac{7}{4} - \frac{3|V_{tp}|}{V_{DD}} + (\frac{|V_{tp}|}{V_{DD}})^2]$$

$$\Rightarrow t_P = \frac{t_{PHL} + t_{PLH}}{2}$$

1. ***When V_{tn}=|V_{tp}|, α_n=α_p. By selecting W/L and $k'_n(W/L)_n$ =k'_p $(W/L)_p$, one can equalize t_{PHL} and t_{PLH} .***

2. ***Since t_P is proportional to C, one shall minimize all the parasitic capacitances; such as devices (minimizing the length), wiring, and coupling cap.***

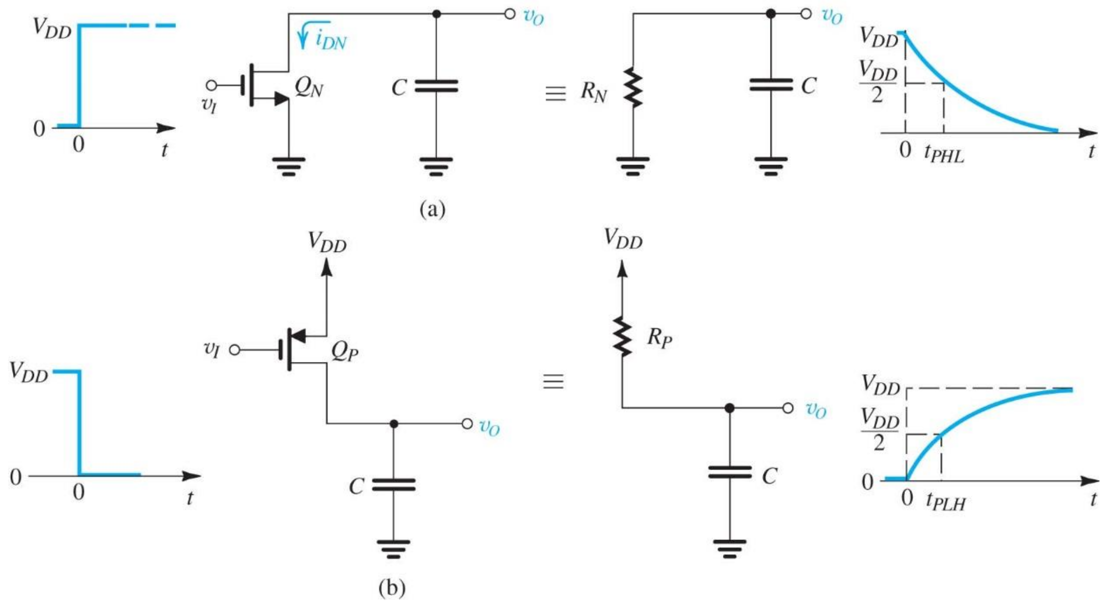
3. ***For 0.25um, 0.18um, and 0.13um processes, $\mu_n C_{ox}$ is 110, 300, 430 $\mu A/V^2$. So, one can select high $\mu_n C_{ox}$ to reduce t_P . But, for such process, C_{ox} is increased.***

4. ***One can increase W/L to reduce t_P . Sometimes, it works, but it may also increase C.***

5. ***One can increase V_{DD} to reduce t_P . But, it depends upon the supply voltage which determined by the process.***

6. ***The conclusion is "there is a trade-off in designing CMOS digital circuits".***

An Alternative Approach



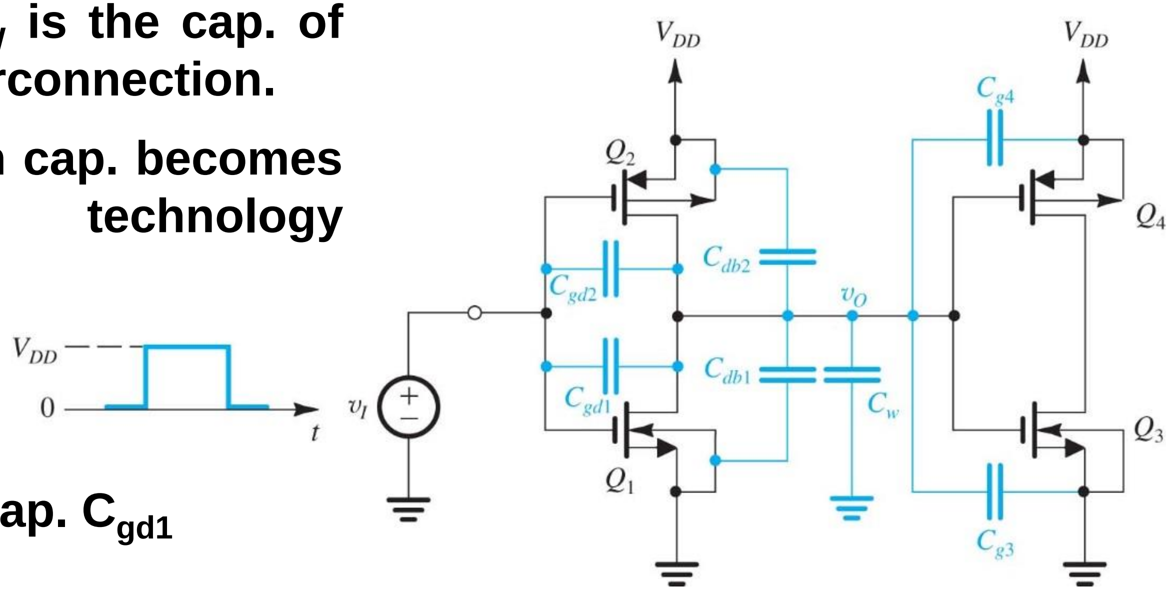
For a step input, $t_{PHL} = \tau \ln 2 = 0.69\tau = 0.69 R_N C \quad \& \quad t_{PLH} = 0.69 R_P C$

Empirical values $R_N = \frac{12.5}{(W/L)_n} k\Omega \quad \& \quad R_P = \frac{30}{(W/L)_p} k\Omega$

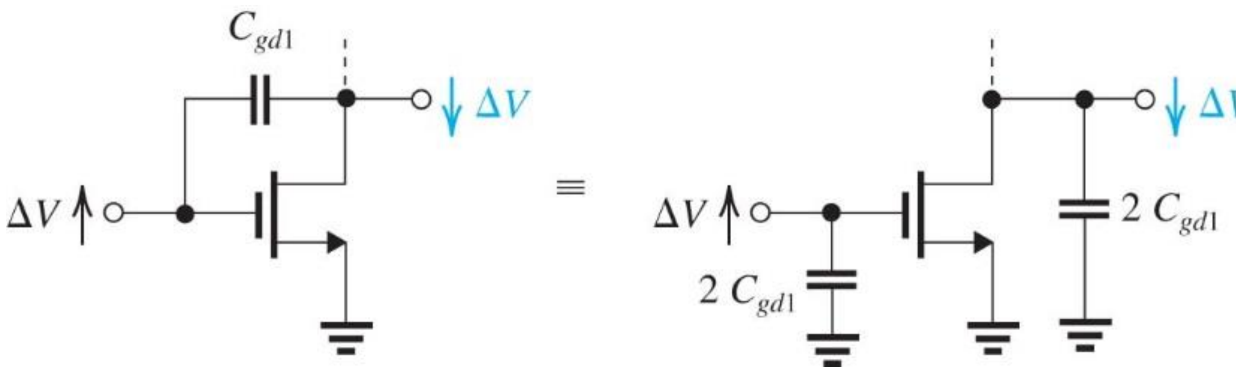
For a ramp input, $t_{PHL} \approx R_N C \quad \& \quad t_{PLH} \approx R_P C$

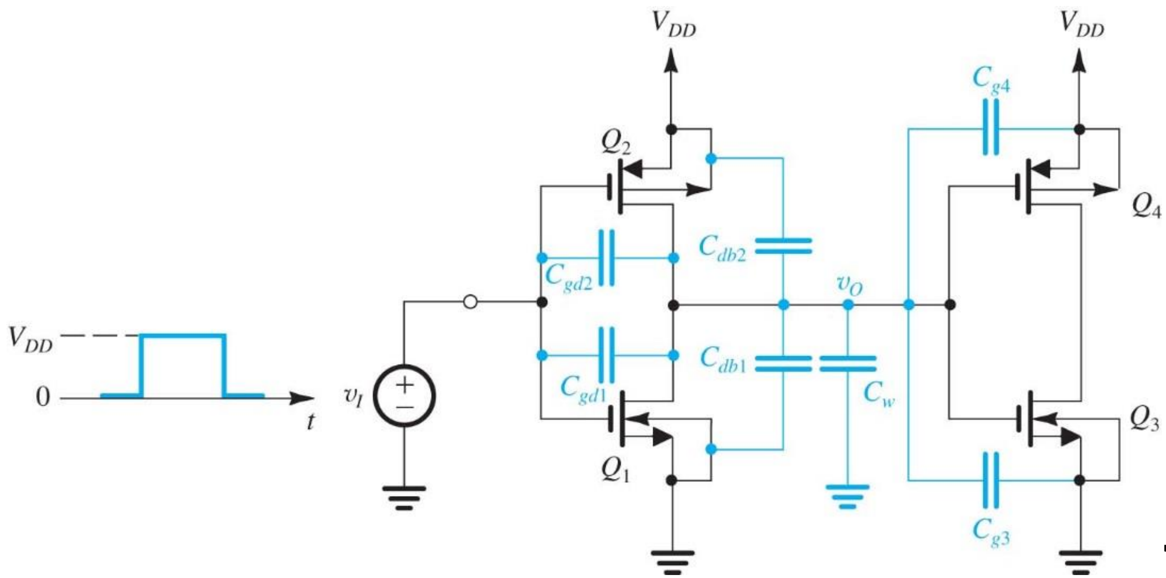
15.4.3 Determining the Equivalent Load Capacitance

1. **Wiring Cap. C_W is the cap. of the wire or interconnection.**
2. **Interconnection cap. becomes dominant as technology scaled down**



3. **Miller Effect for Cap. C_{gd1}**





Junction cap.

$$C_{db} = \frac{C_{db0}}{\sqrt{1+\frac{V_{DB}}{V_o}}} \quad C_{sb} = \frac{C_{sb0}}{\sqrt{1+\frac{V_{SB}}{V_o}}}$$

V_o junction built-in voltage (0.6~0.8V)

V_{DB}, V_{SB} reverse-bias voltage

Cap. C_{db1} and C_{db2} → (9.25)

Cap. C_{g3} and C_{g4}

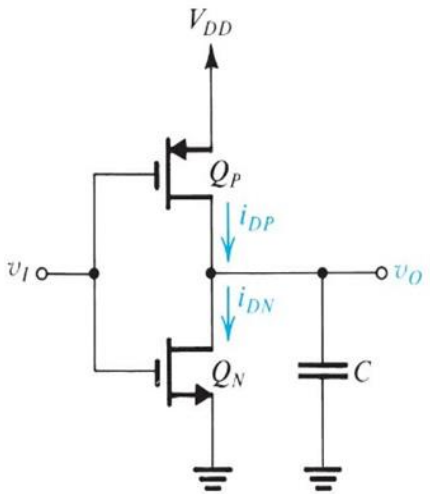
$$C_{g3} + C_{g4} = (WL)_3 C_{ox} + (WL)_4 C_{ox} + C_{gsov3} + C_{gdov3} + C_{gsov4} + C_{gdov4}$$

Equivalent Load Capacitance

$$C = 2C_{gd1} + 2C_{gd2} + C_{db1} + C_{db2} + C_{g3} + C_{g4} + C_W$$

Example 15.7 Determining the Equivalent Load Capacitance and Propagation Delay

To consider a 0.25um process, V_{DD}=2.5V, V_{tn}=-V_{tp}0.5V, $\mu_n C_{ox}$=110uA/V^2, $\mu_p C_{ox}$=30uA/V^2, C_{ox}=6fF/μm^2, Qn's Wn/Ln=0.375μm/0.25μm, , Qp's Wp/Lp=1.125μm/0.25μm, overlap capacitance C_{gdn}=0.3fF/μm x Wn, C_{gdp}=0.3fF/μm x Wp, C_{dbn}=0.1fF, C_{dbp}=0.1fF, wire capacitance C_W=0.2fF



$$C = 2C_{gd1} + 2C_{gd2} + C_{db1} + C_{db2} + C_{g3} + C_{g4} + C_W$$

$$C_{gd1} = 0.3\text{ x}W_n = 0.3\text{ x}0.375\text{=}0.1125\text{fF}$$

$$C_{gd2} = 0.3\text{ x}W_p = 0.3\text{ x}1.125\text{=}0.3375\text{fF}$$

$$C_{g3} = W_n L_n C_{ox} + 2C_{gdn} \text{=}0.375\text{ x }0.25\text{ x}6\text{ +}2\text{ x }0.3\text{ x }0.375\text{=}0.7875\text{fF}$$

$$C_{g4} = W_p L_p C_{ox} + 2C_{gdp} \text{=}1.125\text{ x }0.25\text{ x}6\text{ +}2\text{ x }0.3\text{ x }1.125\text{=}2.3625\text{fF}$$

$$\Rightarrow C = 6.25\,fF$$

$$I_{ave} t_{PHL} = C[V_{DD} - V_{DD} / 2]$$

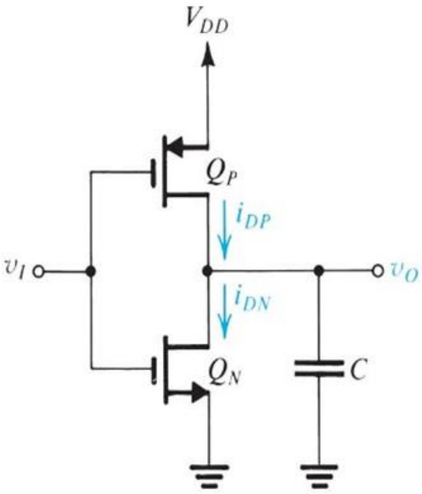
$$t_{PHL} = \frac{CV_{DD}}{2I_{ave}} \quad \Rightarrow \alpha_n = 2 / [\frac{7}{4} - \frac{3V_{tn}}{V_{DD}} + (\frac{V_{tn}}{V_{DD}})^2] = 1.7 \quad \& \quad t_{PHL} = \frac{\alpha_n C}{k'_n (W / L)_n V_{DD}} = 25.8 ps$$

$$\alpha_p = 2 / [\frac{7}{4} - \frac{3 | V_{tp} |}{V_{DD}} + (\frac{| V_{tp} |}{V_{DD}})^2] = 1.7 \quad \& \quad t_{PLH} = \frac{\alpha_p C}{k'_p (W / L)_p V_{DD}} = 31.5 ps$$

$$\Rightarrow t_P = \frac{t_{PHL} + t_{PLH}}{2} = 28.7 ps$$

15.5 Transistor Sizing

15.5.1 Inverter Sizing



1. ***To minimize area, the minimum length given by the technology is selected.***
2. ***To minimize area, $(W/L)_n$ is selected in the range of 1 to 1.5. The selection of $(W/L)_p$ relative to $(W/L)_n$ has an impact on Noise Margin and t_{PLH}. Both are optimized by matching Q_N and Q_P. It wastes area and increases C. Thus, selecting $(W/L)_p$=$(W/L)_n$ or ($_{W/L)p=2(W/L)n}$ for compromise.***
3. ***Having settled on the ratio of $(W/L)_p$ to $(W/L)_n$. Let us consider t_P.***

$C = C_{\text{int}} + C_{ext}$; intrinsic cap. C_{int} and

extrinsic cap. C_{ext} : wire cap. and the input cap. from the driven satge

Increase $(W/L)_p$ and $(W/L)_n$ by a factor of S relative to the minimum-size inverter by which $C_{int}=C_{int0}$.

$$C = C_{\text{int}} + C_{ext} = S \cdot C_{\text{int}0} + C_{ext}$$

For a given equivalent resistance,

$$R_{eq} = \frac{1}{2}(R_N + R_P) \Rightarrow t_P = 0.69 R_{eq} C$$

If the minimum-size inverter has R_{eq0}, increasing $(W/L)_p$ and $(W/L)_n$ by a factor of S reduces $R_{eq}= R_{eq0}/S$.

$$\Rightarrow t_P = 0.69 \frac{R_{eq0}}{S}(S \cdot C_{\text{int}0} + C_{ext}) = 0.69 R_{eq0} \cdot C_{\text{int}0} + 0.69 \frac{R_{eq0}}{S} \cdot C_{ext}$$

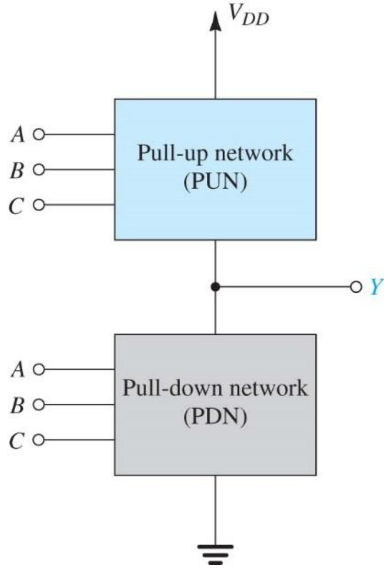
Thus, this scaling does not change the part of t_P caused by Q_N and Q_P.

It reduces the part of t_P caused by C_{ext}. Of course, the area will be increased.

15.5.2 Transistor Sizing in CMOS Logic Gates

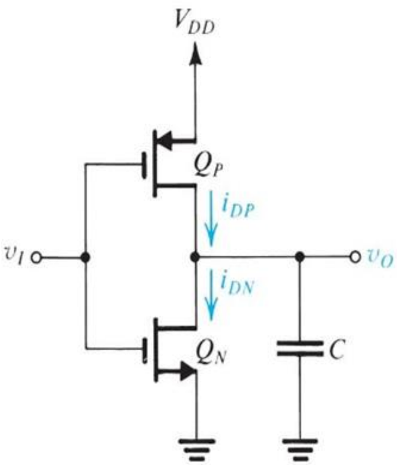
1. For *a basic inverter, $(W/L)_n$ =n and $(W/L)_p$=p where n is usually 1 to 1.5.*

*For match design p=(μ_n/μ_p) *n; often p=2n, and for minimum design, p=n.*



PDN has a discharging current equal to that of $(W/L)_n$=n

and PUN has a charging current equal to that of $(W/L)_p$=p



2. If a number of MOSFETs with *$(W/L)_1$, $(W/L)_2$, … are in series,*

$$R_{Series} = R_{N1} + R_{N2} + \ldots = \frac{\text{constant}}{(W/L)_1} + \frac{\text{constant}}{(W/L)_2} + \ldots = \frac{\text{constant}}{(W/L)_{eq}}$$

$$\Rightarrow (W/L)_{eq} = \frac{1}{\frac{1}{(W/L)_1} + \frac{1}{(W/L)_2} + \ldots}$$

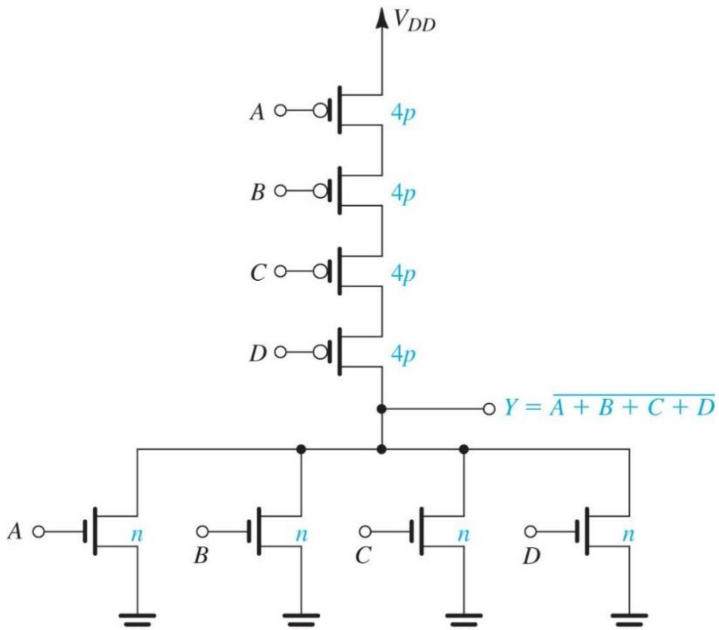
E.g., Two transistors in series, *$(W/L)_{eq}$= $(W/L)_{1,2}/2$*

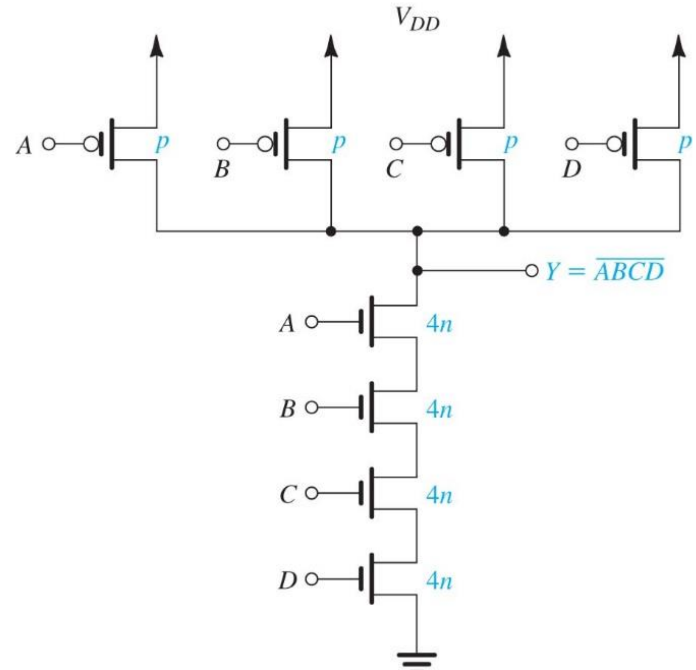
If a number of MOSFETs with *$(W/L)_1$, $(W/L)_2$* ,
… are in parallel,

$$(W/L)_{eq} = (W/L)_1 + (W/L)_2 + \ldots$$

E.g., Two transistors in parallel, *$(W/L)_{eq}$=2 $(W/L)_{1,2}$*

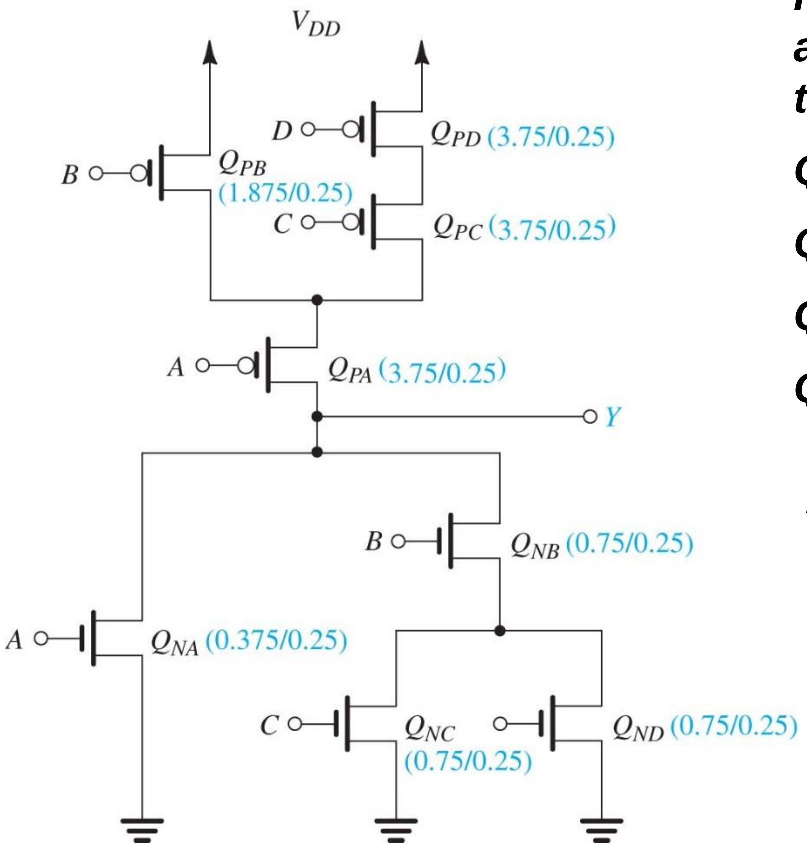
For example, for a 4-input OR gate in the worst case (the lower current), only a NMOS with $(W/L)_n$=n is on. To have the same charging current compared to a basic inverter, PMOS has $(W/L)_p$=4p.
Similarly, for a 4-input NAND gate, NMOS has $(W/L)_n$=4n.





Example 15.8 Transistor Sizing of a CMOS Gate

For a basic inverter, n=1.5 and p=5 and L=0.25um.



PDN: to consider a worst case, Q_{NB} is active and either Q_{NC} or Q_{ND} is active. Thus, we have two transistors in series.

Q_{NB}: W/L=2n=3=0.75/0.25

Q_{NC}: W/L=2n=3=0.75/0.25

Q_{ND}: W/L=2n=3=0.75/0.25

Q_{NA}: W/L=n=1.5=0.375/0.25

PUN: to consider a worst case, three transistors are in series.

Q_{PD}: W/L=3p=15=3.75/0.25

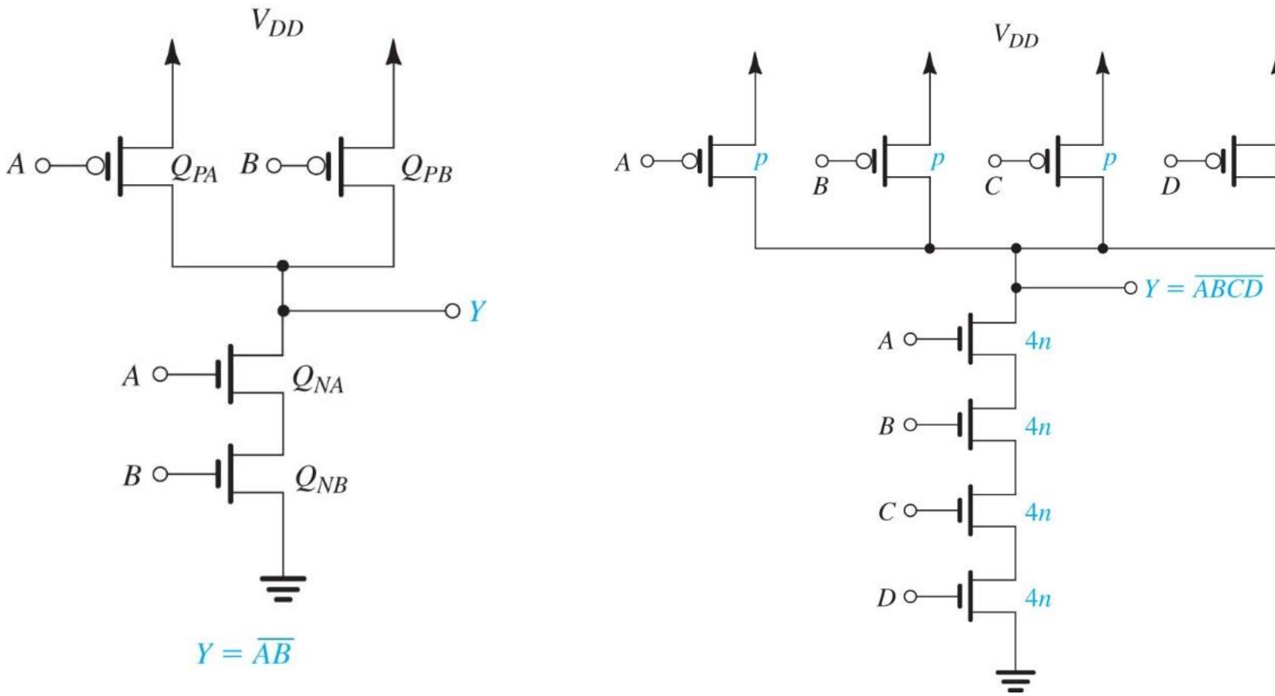
Q_{PC}: W/L=3p=15=3.75/0.25

Q_{PA}: W/L=3p=15=3.75/0.25

The equivalent W/L of the series connection of Q_{PB} and Q_{PA} should be equal to p.

Q_{PB}: W/L=1.5p=7.5=1.875/0.25

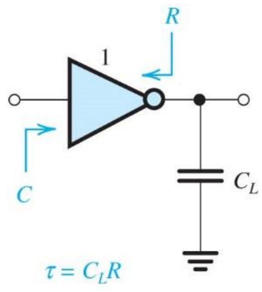
15.5.3 Effects of Fan-in and Fan-out on Propagation Delay



1. ***Each additional input to a CMOS gate, two transistors are required (ex. 2-NAND and 4-NAND). To increase with fan-in, it increases the chip area, capacitance, and propagation delay. Thus, the fan-in of a NAND gate is limited to 4.***
2. ***When a CMOS gate increases its fan-out, the capacitance will be increase which increases the propagation delay. If a higher number of inputs is required, one can realize the Boolean function with the gates of no more than 4-inputs.***

15.5.4 Driving a Large Capacitance

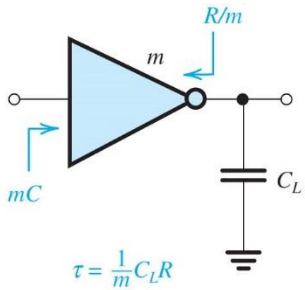
Assume a ramp input,



(a)

$$t_P = \tau = C_L R$$
$$C_{in} = C$$

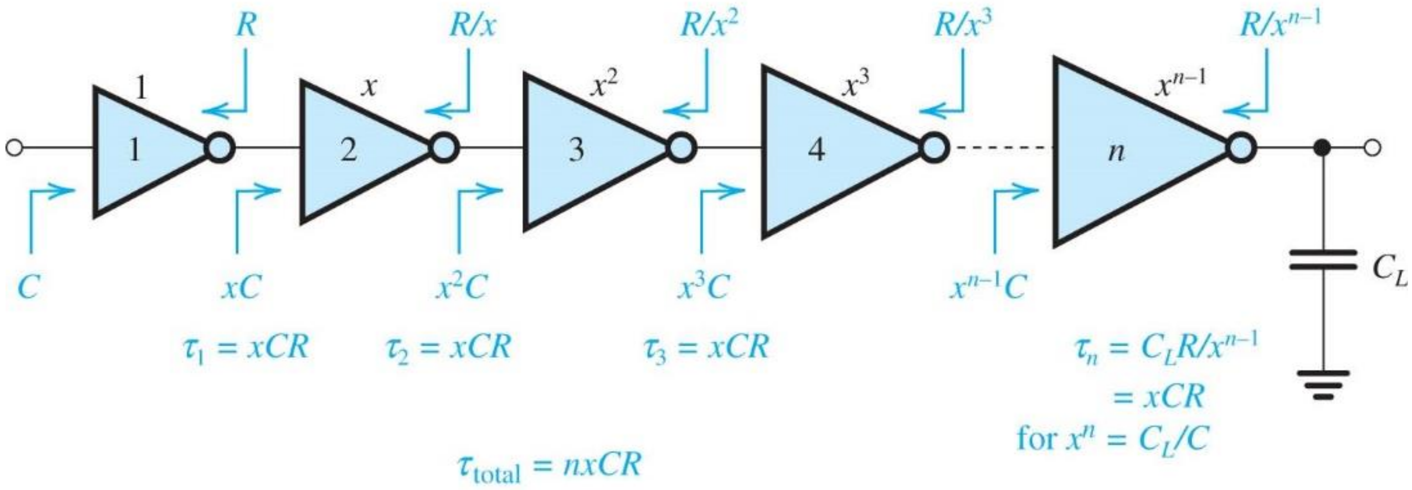
To drive a large capacitance load, one can increase the size to reduce the equivalent resistance. But, the input capacitance Increases.



(b)

$$t_P = \tau = C_L (R / m)$$
$$C_{in} = mC$$

A chain of inverters in cascade is used.



Each inverter in the chain is scaled by a factor of x.

For example, the input capacitance of the n-th inverter is

$$C_{in,n-th} = x^{n-1}C$$

For the 1st~(n-1)th inverters, the time constant is $\tau = xCR$

For the n-th inverter, the time constant is $\tau_n = C_L R / x^{n-1}$

To have the minimum delay (will be verified later),

$$\tau_n = \tau \quad \Rightarrow x^n = \frac{C_L}{C}$$

The total propagation delay is $t_P = n \cdot x \cdot CR$

$$t_P = (n-1)xRC + \frac{1}{x^{n-1}}RC_L \qquad \text{Q.E.D.} \qquad (1)$$

(b) Differenting t_P in Eq. (1) relative to x gives

$$\frac{\partial t_P}{\partial x} = (n-1)RC - \frac{(n-1)}{x^n}RC_L$$

Equating $\frac{\partial t_P}{\partial x}$ to zero gives

$$x^n = \frac{C_L}{C} \qquad \text{Q.E.D.} \qquad (2)$$

(c) Differenting t_P in Eq. (1) relative to n gives

$$\frac{\partial t_P}{\partial n} = xRC - \frac{1}{x^{n-1}}(\ln x)RC_L$$

Equating $\frac{\partial t_P}{\partial n}$ to zero gives

$$x^n\left(\frac{C}{C_L}\right) = \ln x \qquad \text{Q.E.D.} \qquad (3)$$

To obtain the value of x for optimum performance, we combine the two optimality conditions in (2) and (3). Thus

$$\ln x = 1$$

$$\Rightarrow x = e \qquad \text{Q.E.D.}$$

x=e=2.718

In practice, x=2.5~4

Example 15.8 Design an inverter chain to drive a large load capacitance

An inverter has an input capacitance C=10fF and an equivalent output resistance R=1kΩ to drive a load capacitance C_L=1pF.

1. An inverter directly drives a C_L. The propagation delay is around

$$t_P = C_L R = 1ns$$

2. An inverter chain is selected to drive C_L.

$$x^n = \frac{C_L}{C} = 100 \Rightarrow \text{if } x = e = 2.718, \text{ then } n = 4.6$$

Assume n=5,

$$x^5 = \frac{C_L}{C} = 100 \Rightarrow \text{if } x = 2.51$$

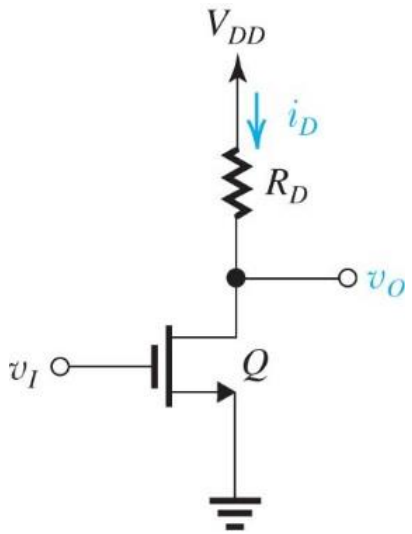
The total propagation delay is

$$t_P = n \cdot x \cdot CR = 5 \cdot 2.51 \cdot (10 \cdot 10^{-15}) \cdot 1k = 125.5\, ps$$

It reduces the total propagation delay by a factor of about 8.

15.6 Power Dissipation

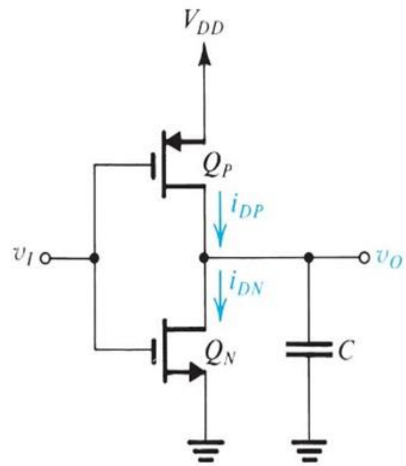
15.6.1 Sources of Power Dissipation



1. When v_I is low, Q is off. → No power dissipation
2. When v_I is high, Q is on. The power is around

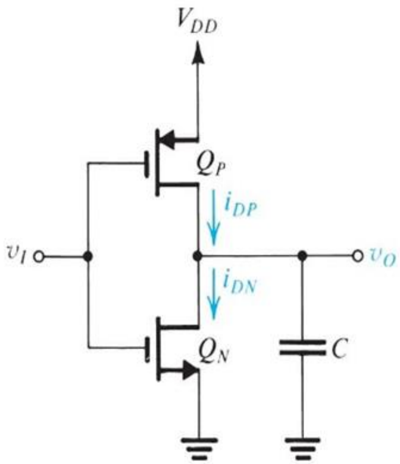
$$V_{DD}^2 / R$$

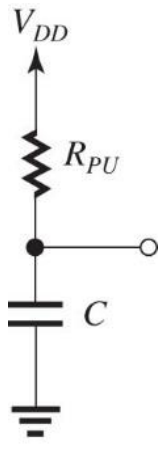
3. If the inverter is not switching, the power dissipates. → **Static Power Dissipation**



1. If the inverter is not switching → no **Static Power Dissipation**
2. If the inverter switching, the current will charge or discharge the load capacitance.

→ **Dynamic Power Dissipation**





(a)

1. **When v_I is low, Q_P (or R_{PU}) is active.**

$$P_{DD}(t) = V_{DD} \cdot i_D(t)$$

Within a charging time T_C, the power supply delivered the energy to the load is

$$E_{DD} = \int_0^{T_C} V_{DD} \cdot i_D(t)dt = V_{DD} \int_0^{T_C} i_D(t)dt = V_{DD} \cdot Q$$

Assume the initial voltage on C is zero, the charge Q is

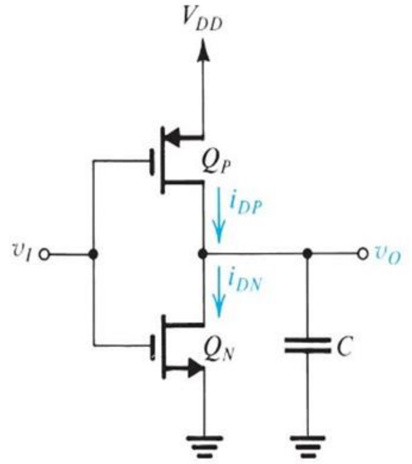
$$Q = V_{DD} \cdot C \quad \Rightarrow \quad E_{DD} = C \cdot V_{DD}^{\ 2}$$

At the end of the charging process, the energy stored on C is

$$E_{stored} = \frac{C \cdot V_{DD}^{\ 2}}{2}$$

The energy dissipated in the pull-up switch is

$$E_{dissipated} = E_{DD} - E_{stored} = \frac{C \cdot V_{DD}^{\ 2}}{2}$$

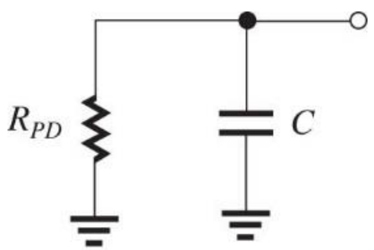


2. When v_I is high, Q_N (or R_{PD}) is active. The energy dissipated in the pull-down switch is

$$C \cdot V_{DD}^{2} / 2$$

Thus, the total energy dissipated per cycle is

$$E_{dissipated} / cycle = C \cdot V_{DD}^{2}$$



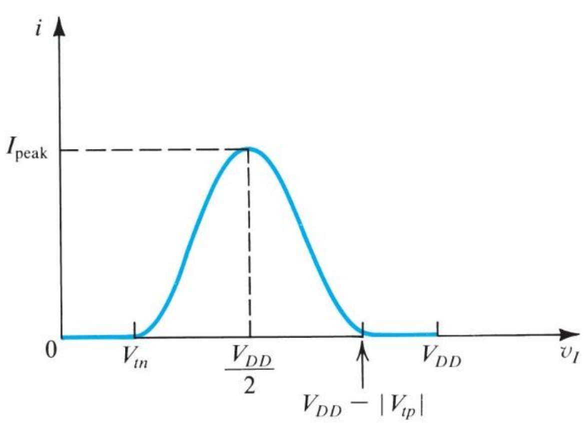
(b)

If the inverter is switching at the frequency of *f* Hz, the dynamic power dissipation of the inverter

$$P_{dyn} = f \cdot C \cdot V_{DD}^{2}$$

To reduce the dynamic power, C or/and V_{DD} must be reduced.

3. Another power dissipation results from the current flows through Q_N and Q_P during the switching. The current versus v_I is given for a matched inverter. The peak current occurs at $v_I = V_{DD}/2$.



$$I_{peak} = \frac{\mu_n C_{OX}}{2} \left(\frac{W}{L}\right)_n \left(\frac{V_{DD}}{2} - V_{tn}\right)^2$$

The width of the current pulse depends upon the rate of change of v_I with time. In general, this power is less than P_{dyn}.

15.6.2 Power–Delay and Energy-Delay Products

The power dissipation of an inverter is P_D. Power–Delay Product (PDP) of the inverter is

$$PDP = P_D \cdot t_P$$

Assume the static power dissipation of an inverter is zero. Then, P_D will be equal to the dynamic power dissipation P_{dyn}.

$$P_{dyn} = f \cdot C \cdot V_{DD}{}^2 = P_D \quad \Rightarrow PDP = f \cdot C \cdot V_{DD}{}^2 \cdot t_P$$

When the inverter is operated at the maximum switching speed; i.e., $f=1/(2t_P)$.

$$PDP = \frac{1}{2} \cdot C \cdot V_{DD}{}^2$$

PDP→ It is the energy consumed by the inverter for each output transition.

One can reduce V_{DD} to minimize PDP. But, it may not be true since t_P is increased while V_{DD} is reduced. So, Energy-Delay Product (EDP) is better and given as

$$EDP = \text{Energy per transition x } t_P = \frac{1}{2} \cdot C \cdot V_{DD}{}^2 \cdot t_P$$