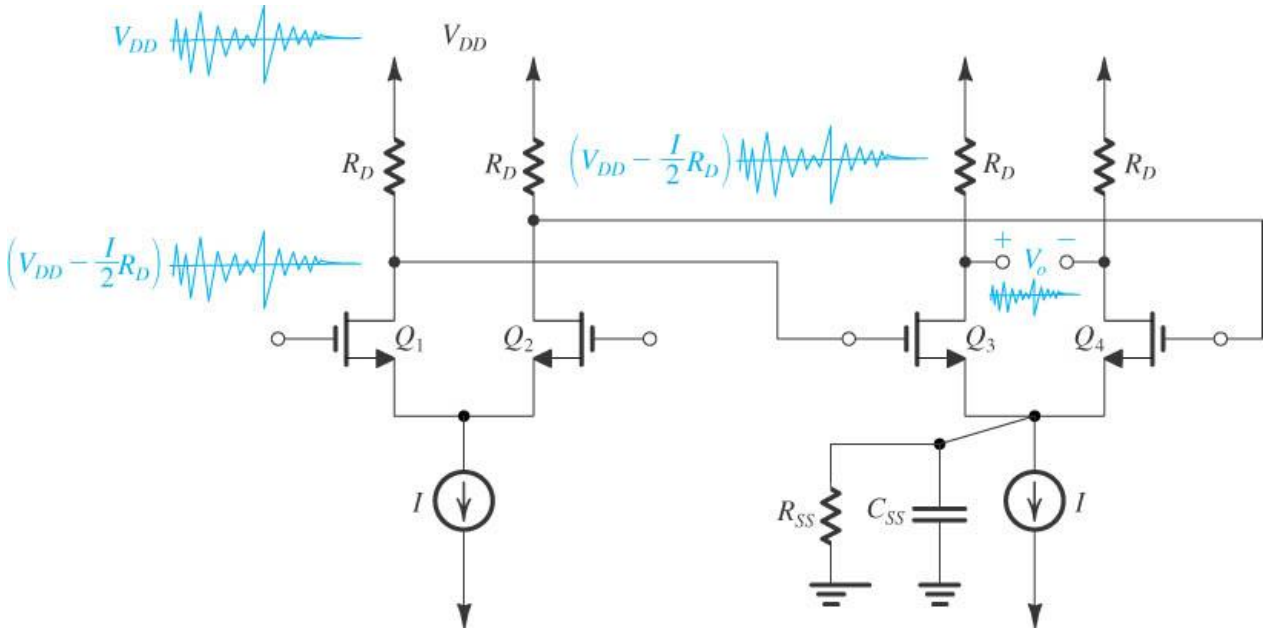
Chapter 8 Differential and Multistage Amplifiers

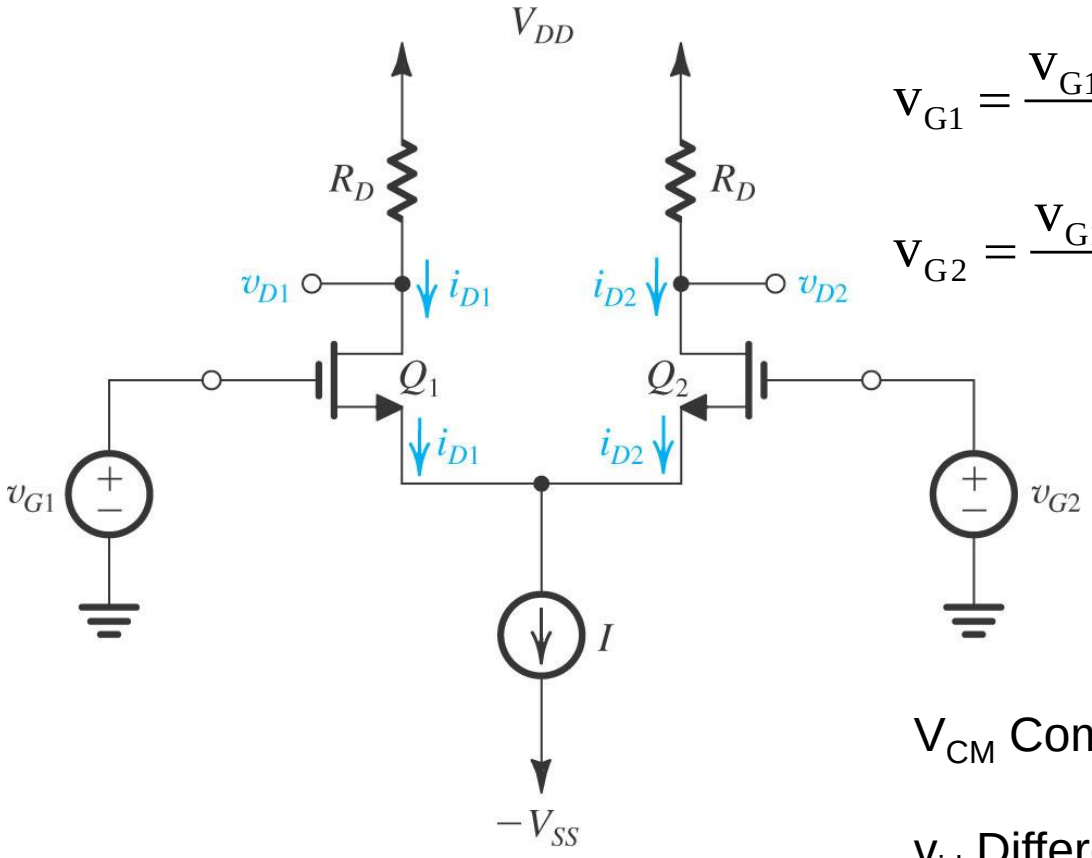
- Reasons for using “differential” instead of “single-end”:

→Differential circuits are much less sensitive to noise and interference than single-ended circuits;

→In general, the bias of differential circuit is suitable for “direct couple”, no bypass and coupling capacitors needed.



8.1 The MOS Differential Pair



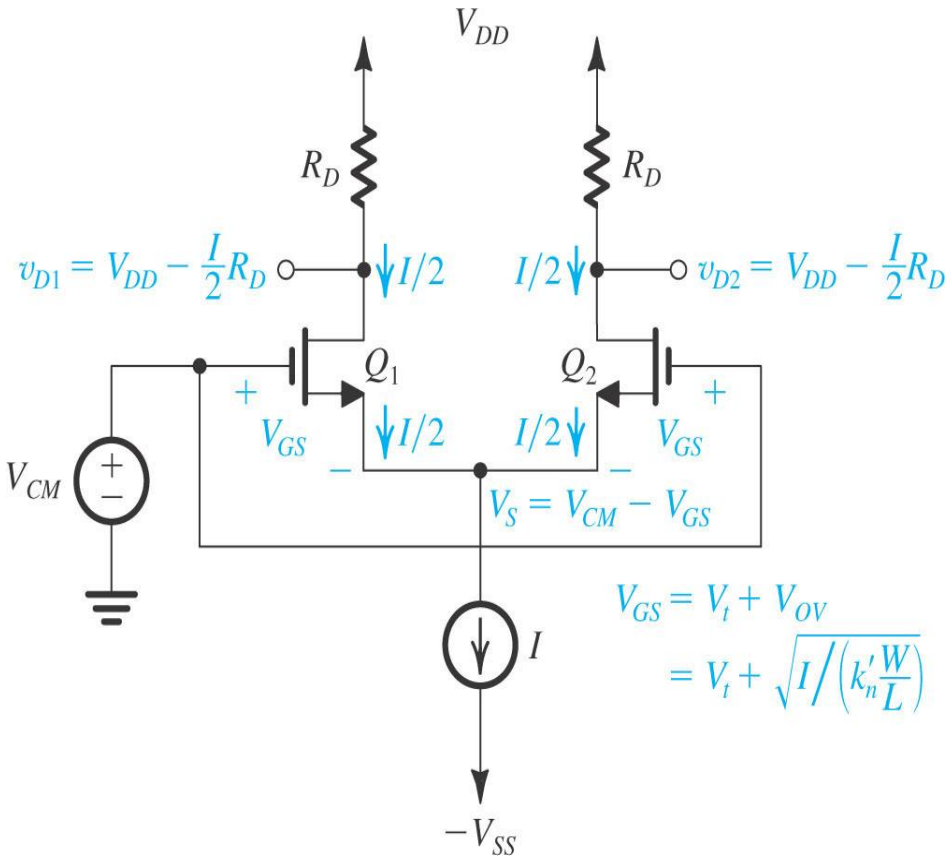
$$v_{G1} = \frac{v_{G1} + v_{G2}}{2} + \frac{v_{G1} - v_{G2}}{2} \equiv v_{CM} + \frac{v_{id}}{2}$$

$$v_{G2} = \frac{v_{G1} + v_{G2}}{2} + \frac{v_{G2} - v_{G1}}{2} \equiv v_{CM} - \frac{v_{id}}{2}$$

V_{CM} Common-Mode (Input) Voltage

v_{id} Differential-Mode (Input) Voltage

8.1.1 Operation with a Common-Mode Input Voltage



$$v_{G1} = v_{G2} = V_{CM}$$

$$V_S = V_{CM} - V_{GS}$$

$$\frac{I}{2} = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2$$

$$= \frac{1}{2} k_n' \frac{W}{L} (V_{OV})^2$$

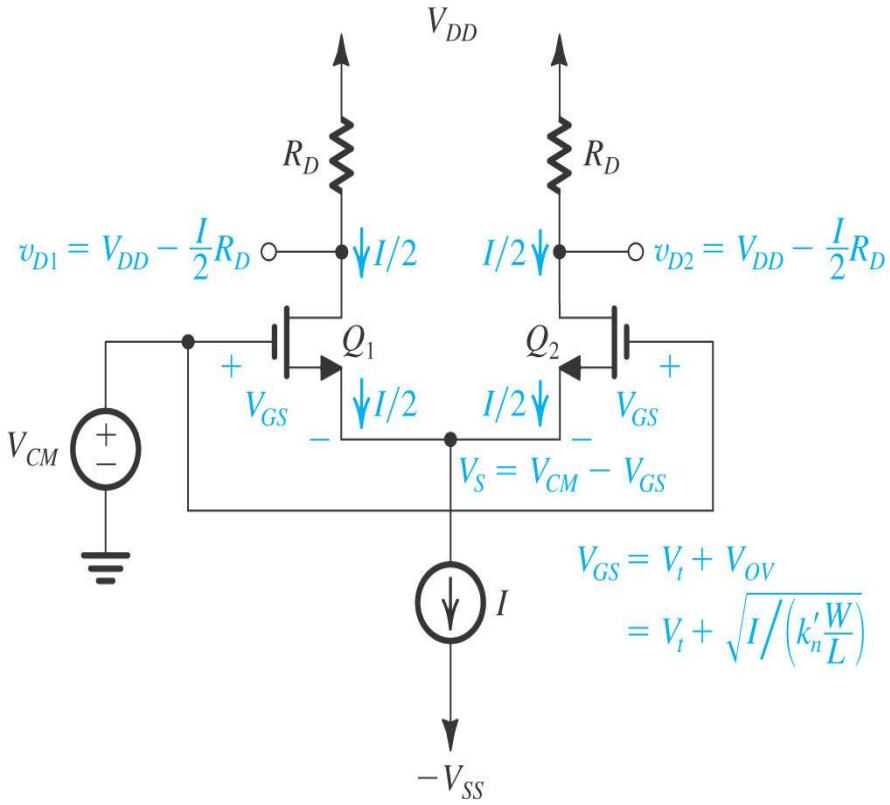
$$\Rightarrow$$

$$V_{OV} = \sqrt{\frac{I}{k_n' (\frac{W}{L})}} \quad \textbf{and}$$

$$v_{D1} = v_{D2} = V_{DD} - \frac{I}{2} R_D$$

$$k_n' = \mu_n C_{ox}$$

•Input common-mode range:



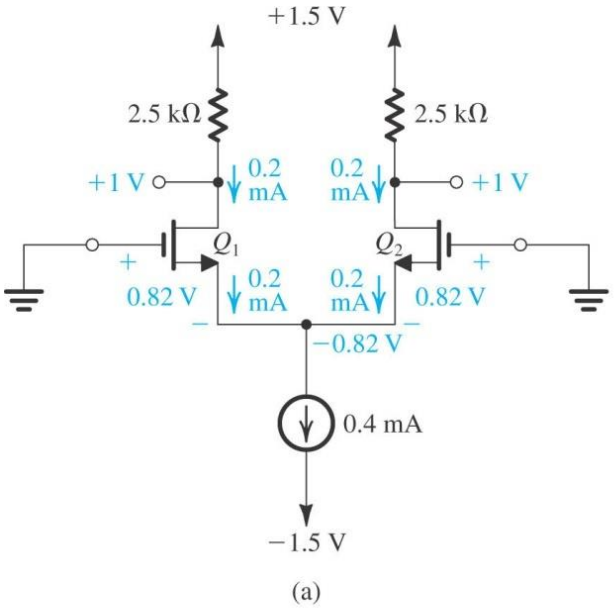
$$v_{CM,max} = V_{DD} - \frac{I}{2}R_D + V_t$$

and

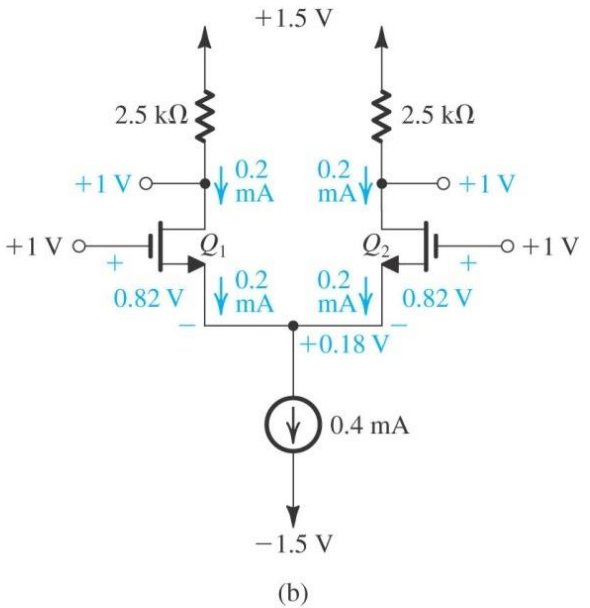
$$v_{CM,min} = -V_{SS} + V_{DS,current\_source} + V_{GS}$$

$$= -V_{ss} + V_{DS,sat} + V_{OV} + V_t$$

Take an example 8.1



(a)



(b)

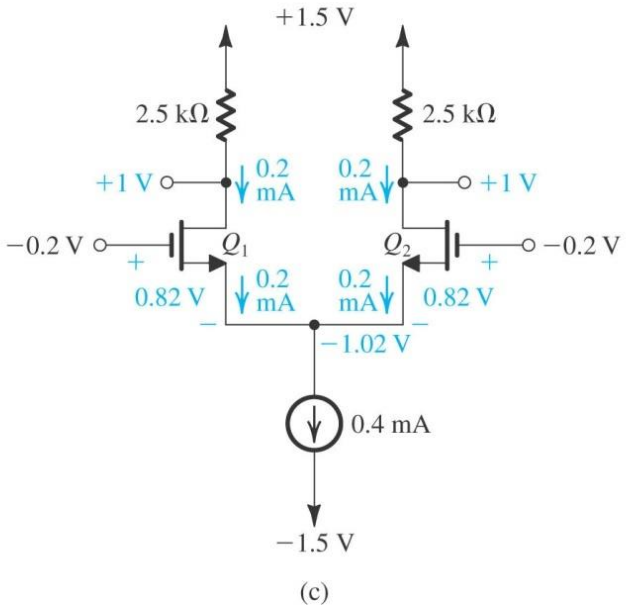
$$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{OV})^2$$

$$k_n' \frac{W}{L} = 4\text{mA}/\text{V}^2 \textbf{ and } I_D = 0.2\text{mA}$$

$$\Rightarrow V_{OV} = 0.316\text{V}$$

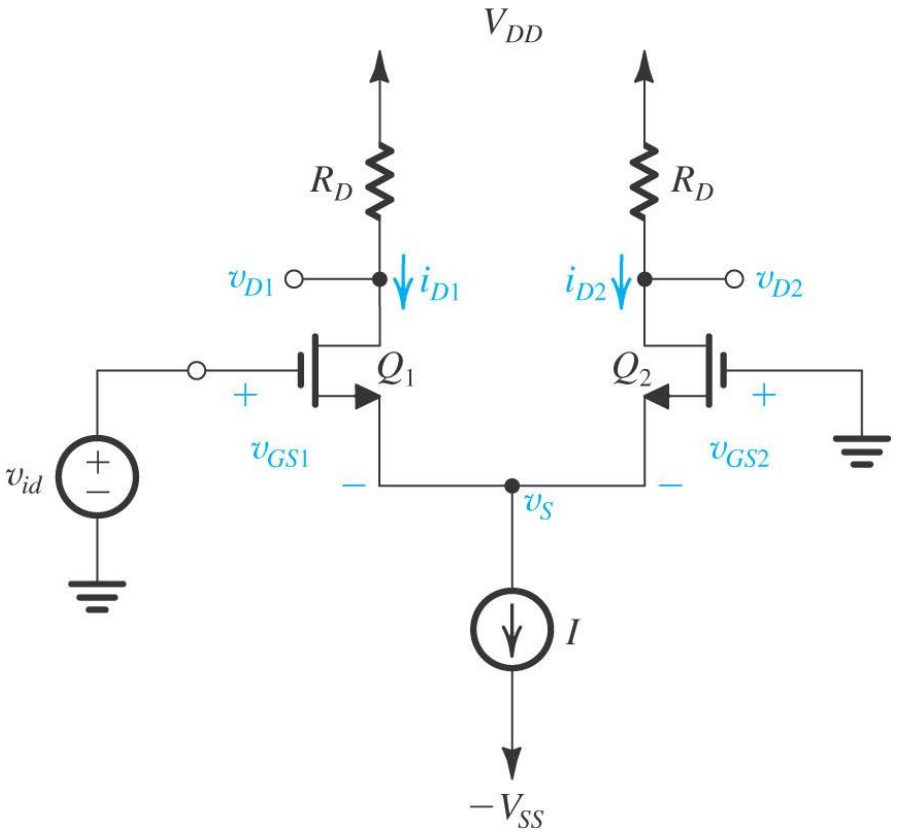
$$V_t = 0.5\text{V}$$

$$\Rightarrow V_{GS} = 0.816\text{V} \approx 0.82\text{V}$$



(c)

8.1.2 Operation with a Differential Input Voltage



Assume $V_{GS2} = V_t \Rightarrow I_{D1} = I$

Assume the gate of Q_2 is grounded, thus the critical boundary

$v_s = -V_t$ *(*from **the viewpoint of Q_2** *)*

as **for Q_1,**

$$I = \frac{1}{2} k_n' \frac{W}{L} (v_{GS1} - V_t)^2$$

$$\Rightarrow v_{GS1} = V_t + \sqrt{2} \cdot V_{OV} \quad \textbf{where } V_{OV} = \sqrt{\frac{I}{k_n'(\frac{W}{L})}}$$

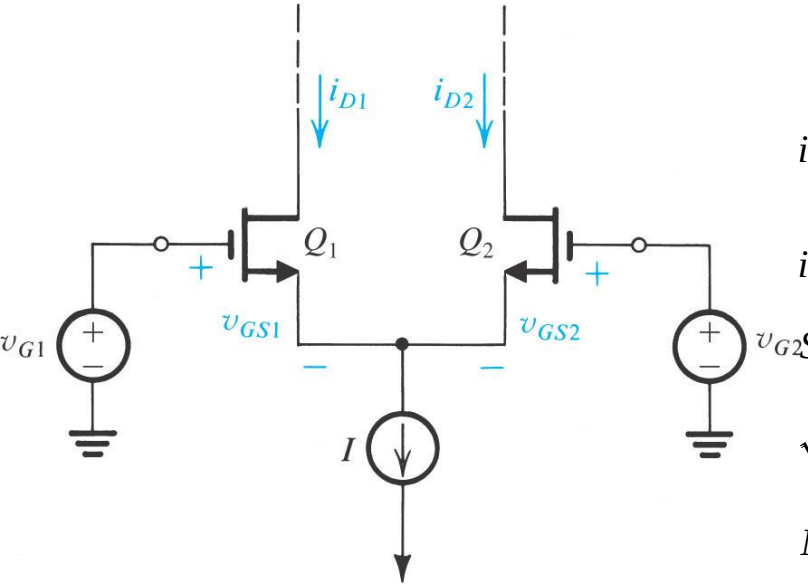
and

$$v_{id,max} = v_{GS1} + v_s = \sqrt{2} \cdot V_{OV}$$

$v_{id,min} = -\sqrt{2} \cdot V_{OV}$ **(in a similar concept, Q_1 is OFF)**

$$-\sqrt{2} \cdot V_{OV} \le v_{id} \le \sqrt{2} \cdot V_{OV}$$

8.1.3 Large-Signal Operation



$$i_{D1} = \frac{1}{2}k_n' \frac{W}{L}(v_{GS1} - V_t)^2 \quad \Leftrightarrow \quad \sqrt{i_{D1}} = \sqrt{\frac{1}{2}k_n' \frac{W}{L}} \cdot (v_{GS1} - V_t)$$

$$i_{D2} = \frac{1}{2}k_n' \frac{W}{L}(v_{GS2} - V_t)^2 \quad \Leftrightarrow \quad \sqrt{i_{D2}} = \sqrt{\frac{1}{2}k_n' \frac{W}{L}} \cdot (v_{GS2} - V_t)$$

Since $v_{id} = v_{GS1} - v_{GS2} = v_{G1} - v_{G2}$

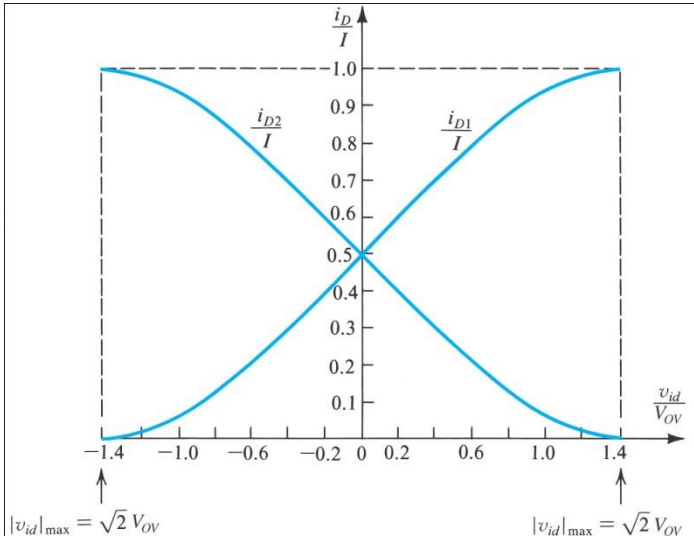
$$\sqrt{i_{D1}} - \sqrt{i_{D2}} = \sqrt{\frac{1}{2}k_n' \frac{W}{L}} \cdot v_{id} = \sqrt{\frac{K}{2}} \cdot v_{id} \quad , K = k_n' \frac{W}{L}$$

Meanwhile, $i_{D1} + i_{D2} = I \quad \Rightarrow \quad 2\sqrt{i_{D1} \cdot i_{D2}} = I - \frac{K}{2} \cdot v_{id}^2 = 2\sqrt{i_{D1} \cdot (I - i_{D1})}$

It makes $i_{D1} = \frac{I}{2} \pm \sqrt{K \cdot I}\,(\frac{v_{id}}{2})\sqrt{1 - \frac{K \cdot (v_{id}/2)^2}{I}}$

since $i_{D1} \propto v_{id}$,

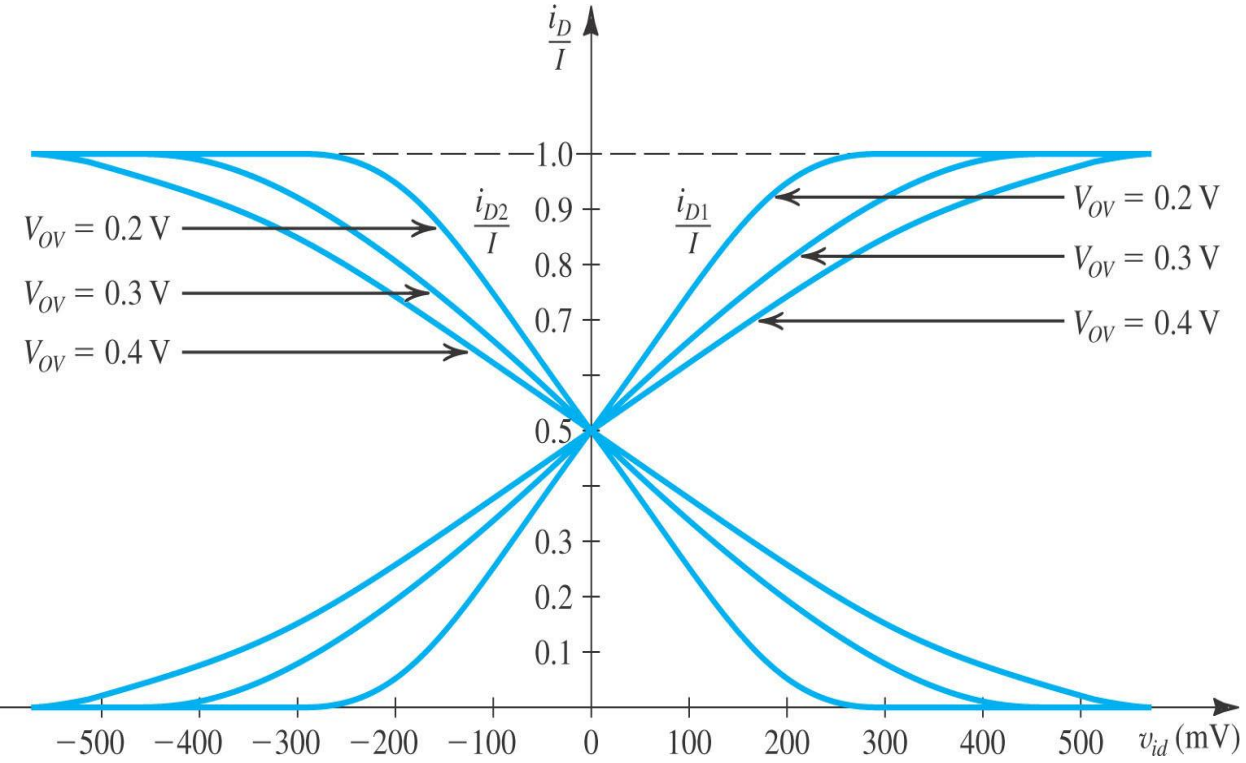
$$\begin{cases} i_{D1} = \frac{I}{2} + \sqrt{K \cdot I}\,(\frac{v_{id}}{2})\sqrt{1 - \frac{K \cdot (v_{id}/2)^2}{I}} \\ i_{D2} = \frac{I}{2} - \sqrt{K \cdot I}\,(\frac{v_{id}}{2})\sqrt{1 - \frac{K \cdot (v_{id}/2)^2}{I}} \end{cases}$$



Since $\frac{I}{2} = \frac{1}{2} K \cdot V_{OV}^2$

$$i_{D1} = \frac{I}{2} + \left(\frac{I}{V_{OV}}\right) \cdot \left(\frac{v_{id}}{2}\right) \cdot \sqrt{1 - \left[\frac{(v_{id}/2)}{V_{OV}}\right]^2} \approx \frac{I}{2} + \left(\frac{I}{V_{OV}}\right) \cdot \left(\frac{v_{id}}{2}\right)$$

$$i_{D2} = \frac{I}{2} - \left(\frac{I}{V_{OV}}\right) \cdot \left(\frac{v_{id}}{2}\right) \cdot \sqrt{1 - \left[\frac{(v_{id}/2)}{V_{OV}}\right]^2} \approx \frac{I}{2} - \left(\frac{I}{V_{OV}}\right) \cdot \left(\frac{v_{id}}{2}\right)$$



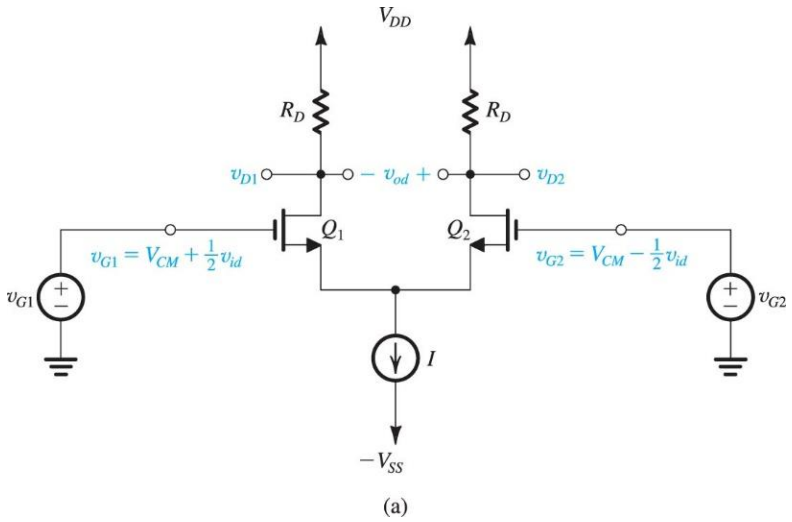
If $\frac{v_{id}}{2V_{OV}} << 1$

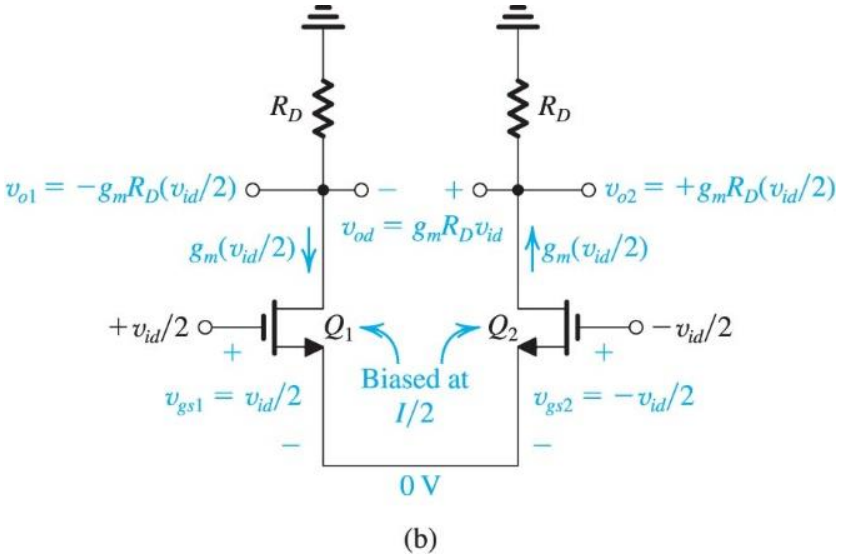
The small-signal current

$$i_d = \left(\frac{I}{V_{OV}}\right) \cdot \left(\frac{v_{id}}{2}\right) = g_m \cdot \left(\frac{v_{id}}{2}\right)$$

8.1.4 Small-Signal Operation of the MOS Differential Pair

Differential Gain

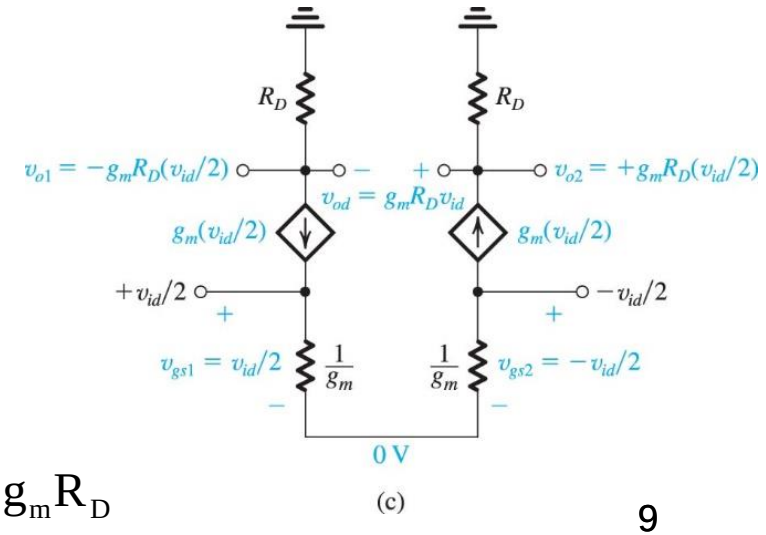




$$v_{G1} = v_{CM} + \frac{1}{2}v_{id} \quad \text{and} \quad v_{G2} = v_{CM} - \frac{1}{2}v_{id}$$

$$g_m = \frac{2I_D}{V_{OV}} = \frac{I}{V_{OV}} \text{ for } \textbf{the single-ended signal}$$

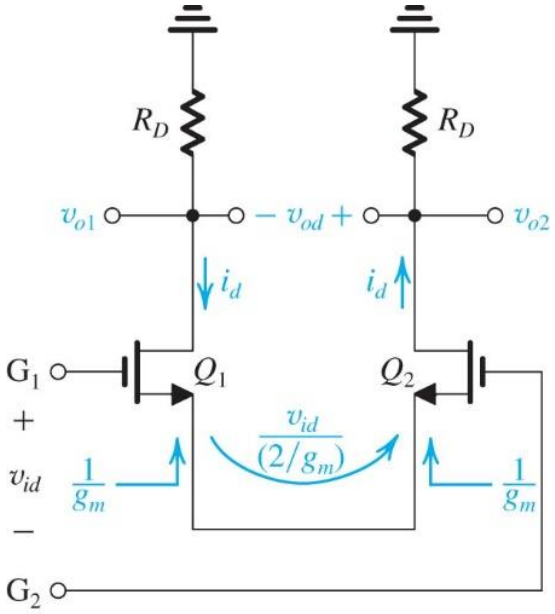
$$v_{o1} = -g_m\left(\frac{v_{id}}{2}\right)\cdot R_D \quad \text{and} \quad v_{o2} = +g_m\left(\frac{v_{id}}{2}\right)\cdot R_D$$



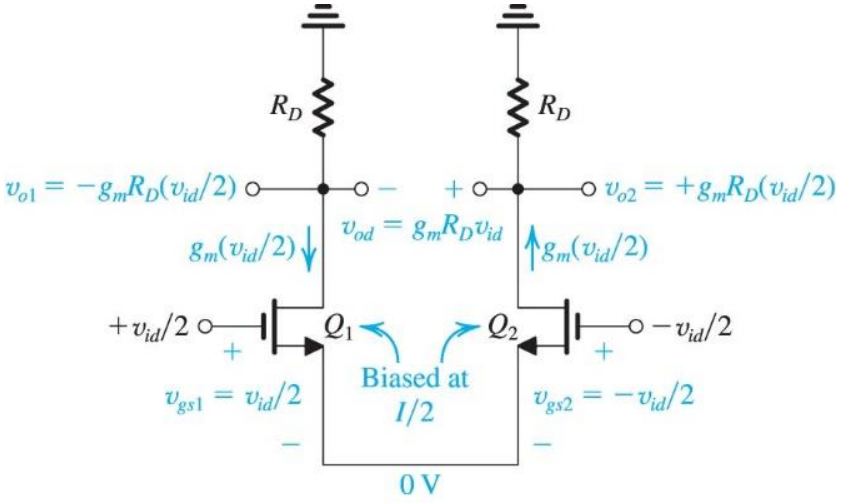
the differential voltage gain

$$A_d = \frac{v_{o2} - v_{o1}}{v_{id}} = \frac{v_{o2}}{v_{id}} - \frac{v_{o1}}{v_{id}} = \frac{1}{2}g_m R_D - \left(-\frac{1}{2}g_m R_D\right) = g_m R_D$$

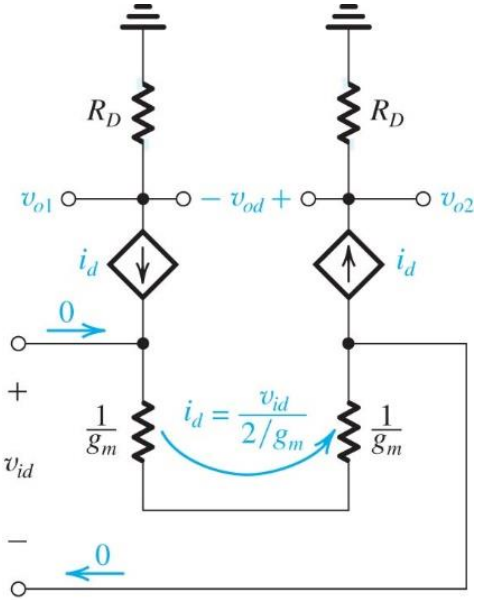
The Differential Half-Circuit



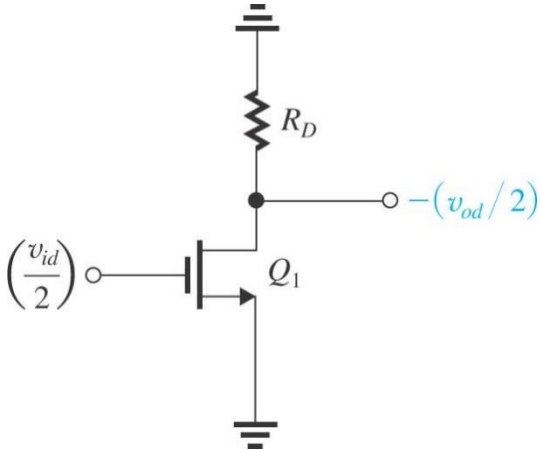
(a)



(b)

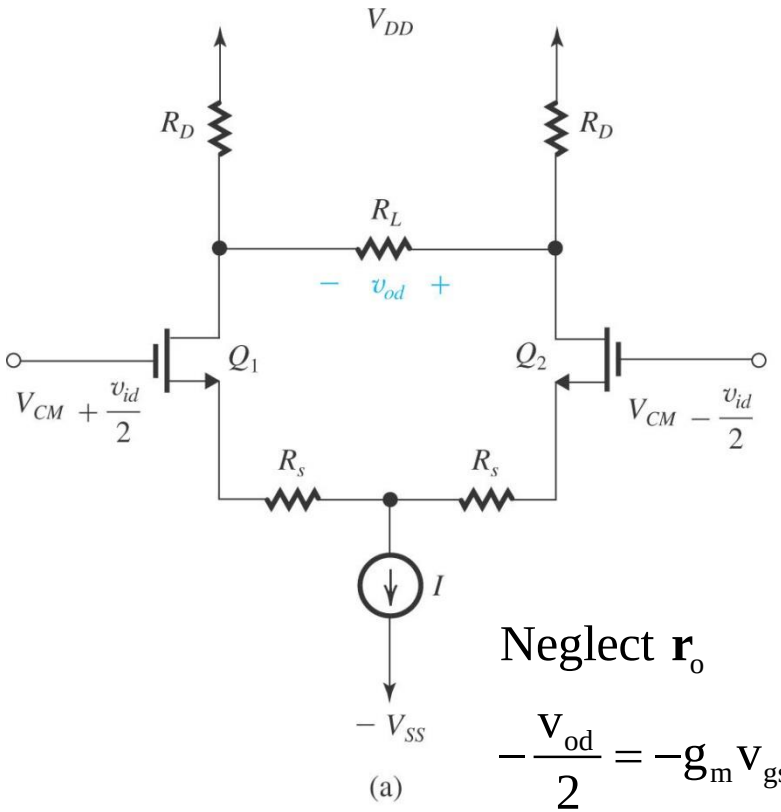


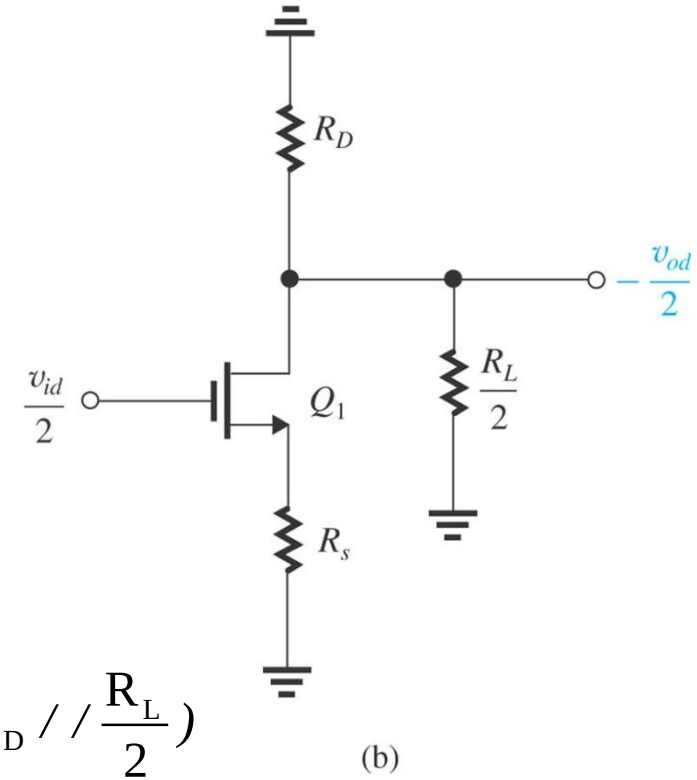
(b)



$$A_d = g_m(R_D // r_o)$$

Example 8.2





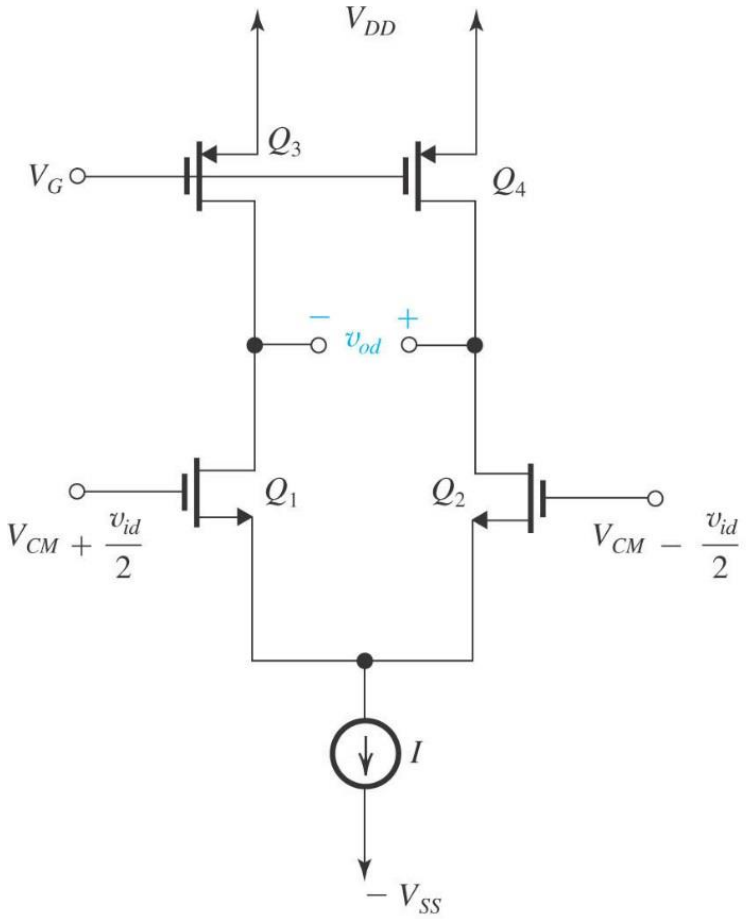
Neglect $\mathbf{r}_o$

$$-\frac{v_{od}}{2} = -g_m v_{gs}\left(R_D // \frac{R_L}{2}\right)$$

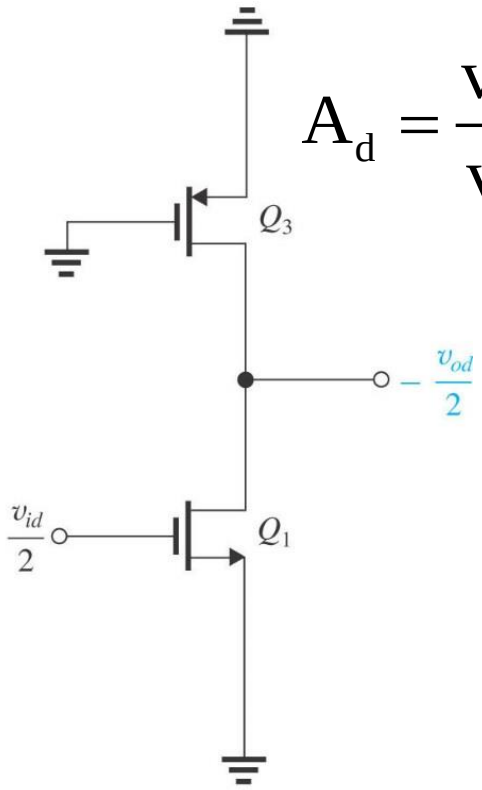
$$\frac{v_{id}}{2} = g_m v_{gs} R_S + v_{gs}$$

$$\Rightarrow A_d = \frac{v_{od}}{v_{id}} = \frac{R_D // \frac{R_L}{2}}{1/g_m + R_S}$$

8.1.5 The Differential Amplifier with Current-Source Loads



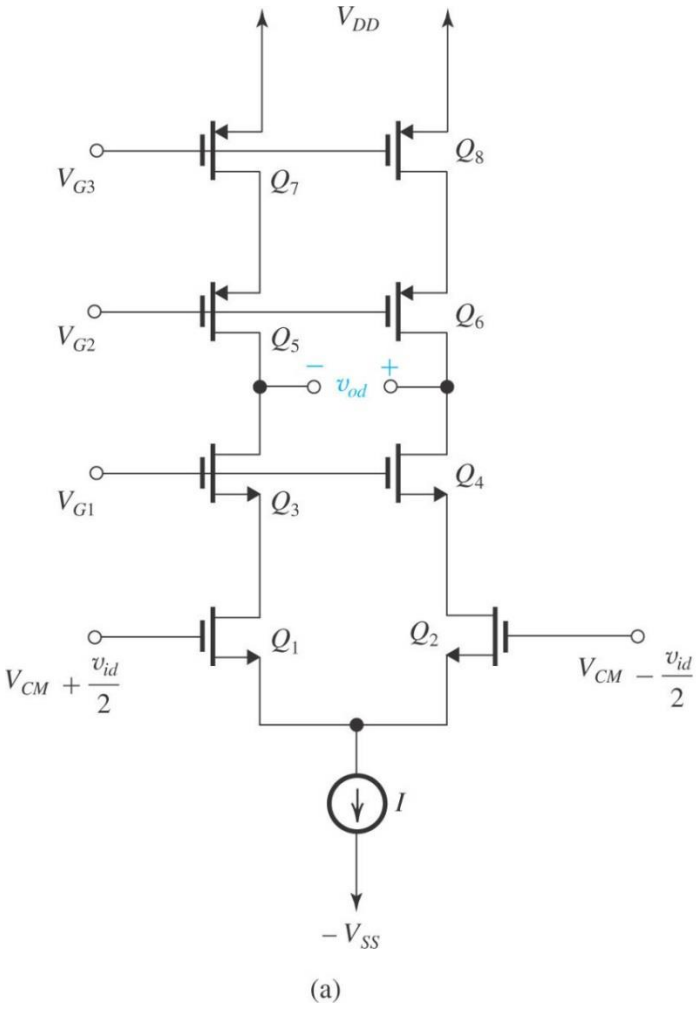
(a)



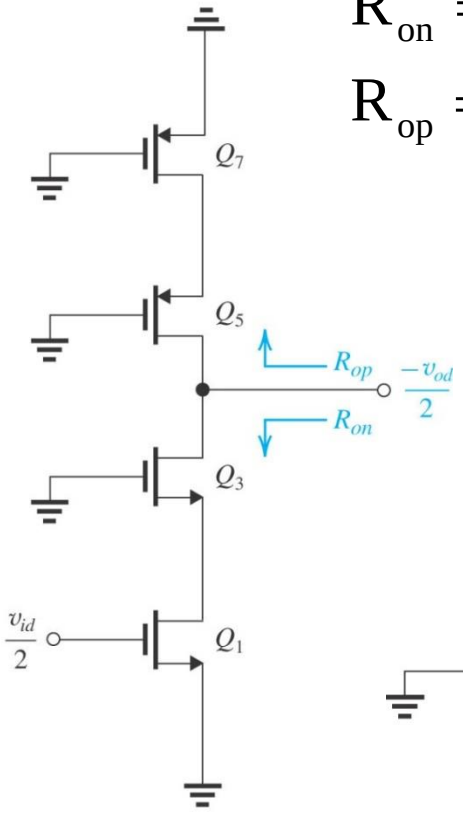
(b)

$$A_d = \frac{v_{od}}{v_{id}} = g_{m1}(r_{o1} // r_{o3})$$

8.1.6 Cascode Differential Amplifier



(a)

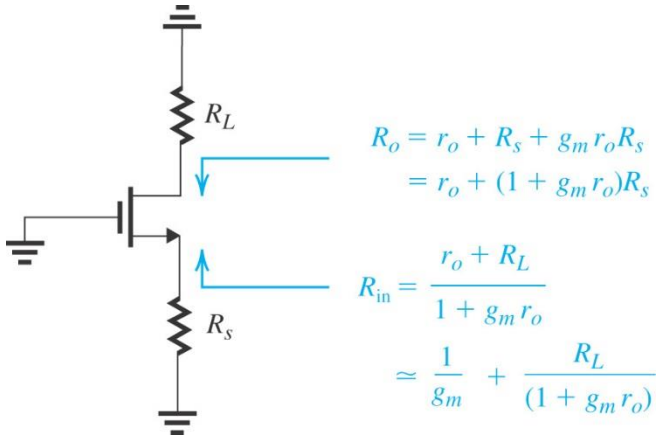


(b)

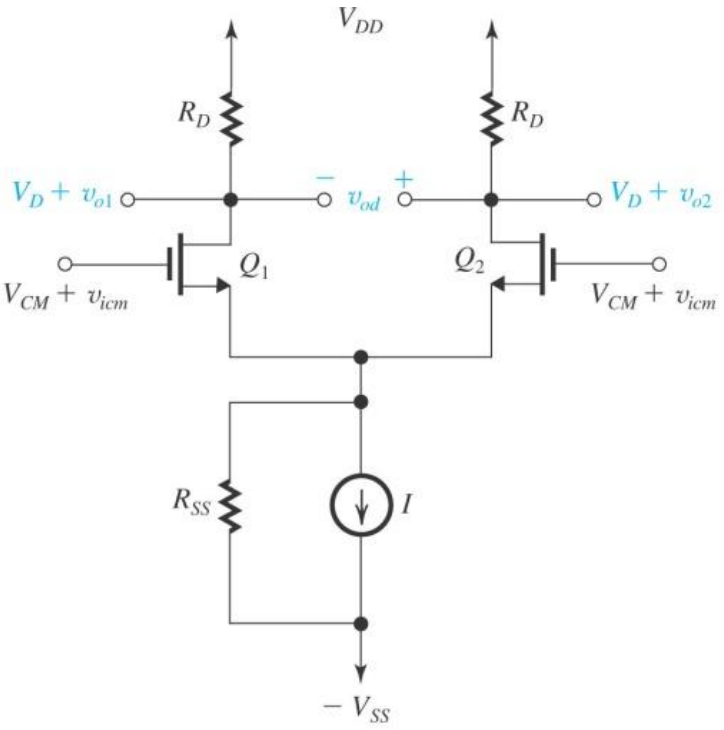
$$A_d = \frac{v_{od}}{v_{id}} = g_{m1}(R_{on} // R_{op})$$

$$R_{on} = (g_{m3} r_{o3}) r_{o1}$$

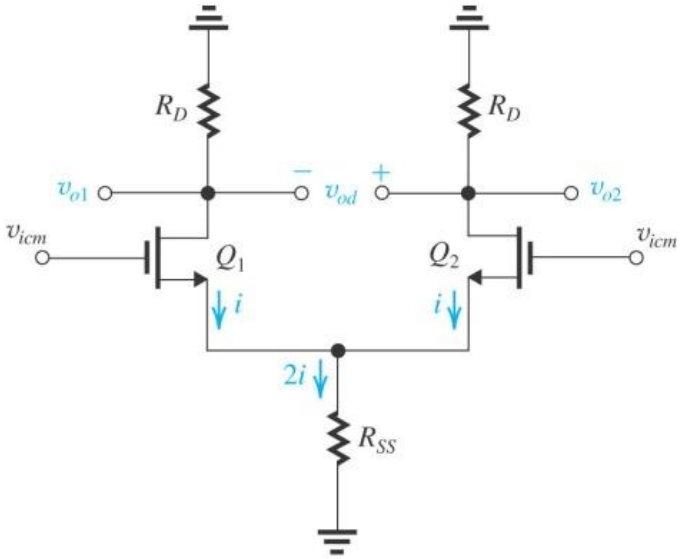
$$R_{op} = (g_{m5} r_{o5}) r_{o7}$$



8.3 Common-Mode Rejection
8.3.1 The MOS Case



(a)



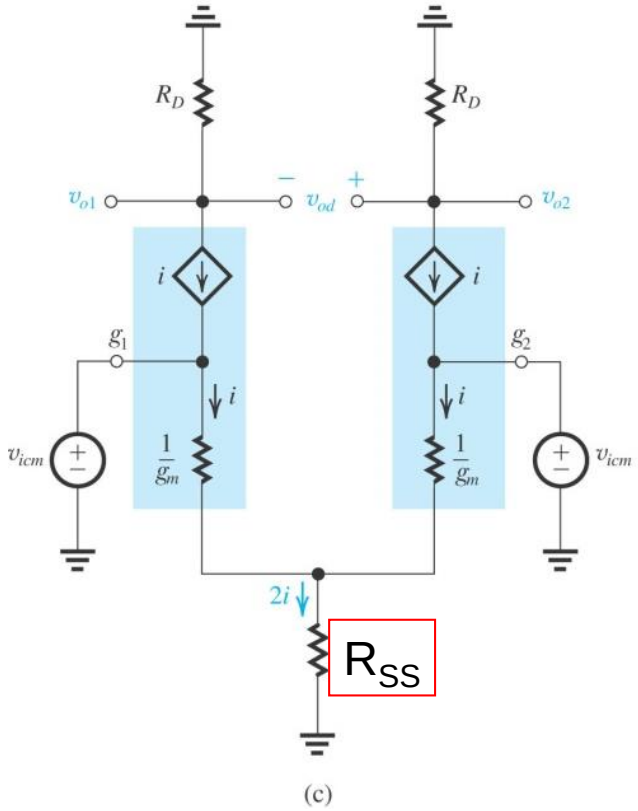
(b)

Method 1

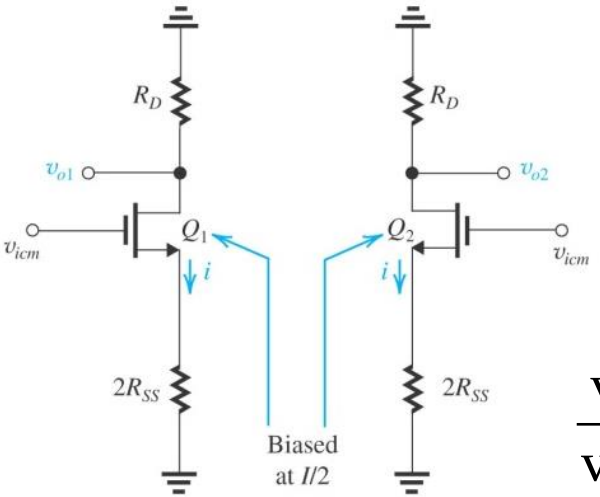
$$v_{icm} = v_{gs} + (2g_m v_{gs})R_{SS} = v_{gs}(1 + 2g_m R_{SS})$$

$$v_{o1} = v_{o2} = -g_m v_{gs} R_D$$

$$\frac{v_{o1}}{v_{icm}} = \frac{v_{o2}}{v_{icm}} = -\frac{R_D}{1/g_m + 2R_{SS}}$$



(c)



(d)

Method 2

$$v_{icm} = \frac{i}{g_m} + 2i \cdot R_{SS} \Rightarrow i = \frac{v_{icm}}{1/g_m + 2R_{SS}}$$

$$v_{o1} = v_{o2} = -i \cdot R_D = -\frac{v_{icm} \cdot R_D}{1/g_m + 2R_{SS}}$$

$$\frac{v_{o1}}{v_{icm}} = \frac{v_{o2}}{v_{icm}}$$

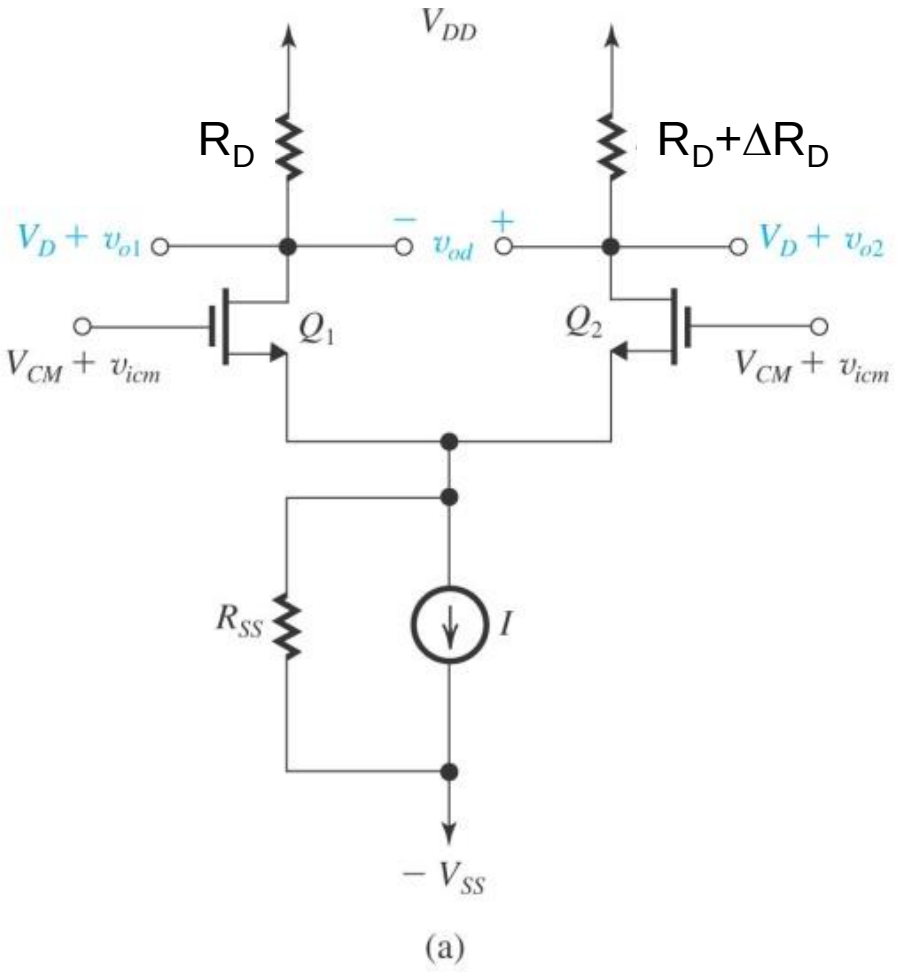
$$= -\frac{R_D}{\frac{1}{g_m} + 2R_{SS}} \approx -\frac{R_D}{2R_{SS}} \quad (\because 2R_{SS} >> 1/g_m)$$

Ideally, free of common-mode interference

$$v_{od} = v_{o2} - v_{o1} = 0$$

$$\frac{v_{o1}}{v_{icm}} = \frac{v_{o2}}{v_{icm}} \equiv -\frac{\textbf{Total resistances in the drain}}{\textbf{Total resistances in the source}}$$

Effect of R_D Mismatch



(a)

Common-Mode Rejection Ratio (CMRR)

$$\frac{v_{o1}}{v_{icm}} = -\frac{R_D}{2R_{SS}}$$

$$\frac{v_{o2}}{v_{icm}} = -\frac{R_D + \Delta R_D}{2R_{SS}}$$

$$v_{od} = v_{o2} - v_{o1} = -\frac{\Delta R_D}{2R_{SS}} v_{icm}$$

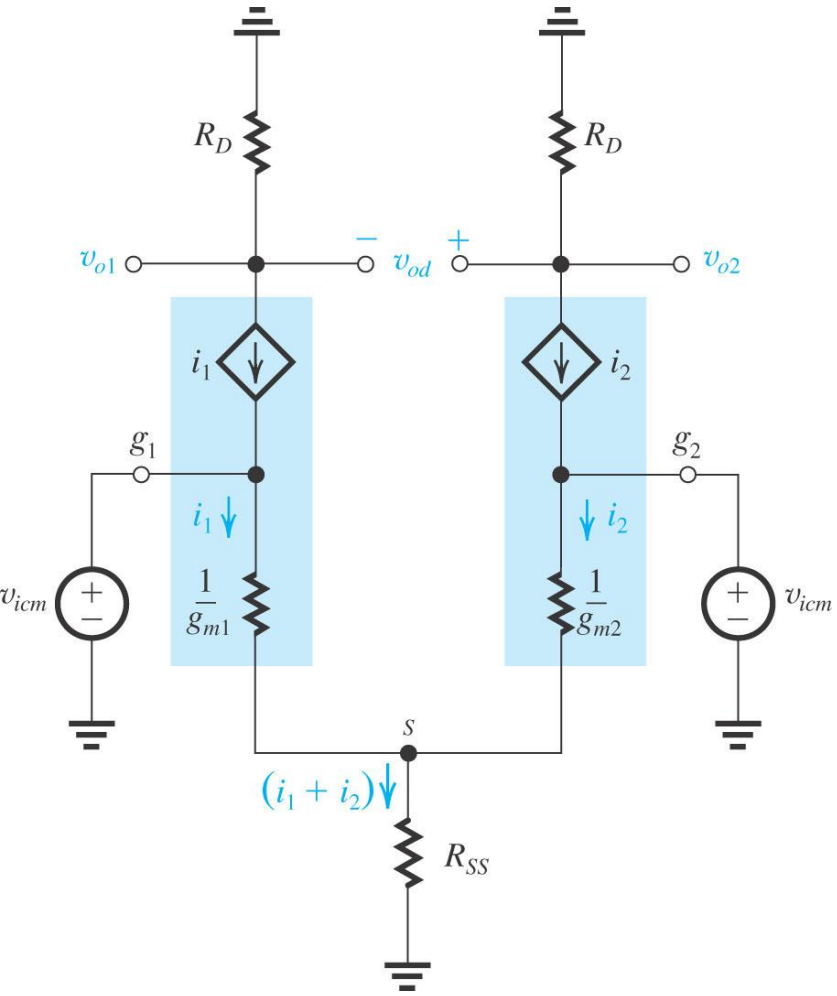
$$A_{cm} = \frac{v_{od}}{v_{icm}} = -\frac{\Delta R_D}{2R_{SS}} = -\frac{R_D}{2R_{SS}} \cdot \frac{\Delta R_D}{R_D}$$

$$\text{CMRR} \equiv \left|\frac{A_d}{A_{cm}}\right| \quad \textbf{or} \quad \text{CMRR}(\text{dB}) \equiv 20\,log\left|\frac{A_d}{A_{cm}}\right|$$

$$\because A_d = g_m R_D$$

$$\text{CMRR} \equiv \frac{2g_m R_{SS}}{(\Delta R_D / R_D)}$$

Effect of g_m Mismatch



$$g_{m1} = g_m + \frac{\Delta g_m}{2} \quad \textbf{and} \quad g_{m2} = g_m - \frac{\Delta g_m}{2}$$

$$\frac{i_1}{g_{m1}} = \frac{i_2}{g_{m2}} \quad \text{thus} \quad \frac{i_1}{i_2} = \frac{g_{m1}}{g_{m2}}$$

$$v_{icm} = \frac{i_1}{g_{m1}} + (i_1 + i_2)R_{SS} = \frac{i_1}{g_{m1}} + (i_1 + \frac{i_1}{g_{m1}} g_{m2})R_{SS}$$

$$i_1 = \frac{g_{m1} v_{icm}}{1 + (g_{m1} + g_{m2})R_{SS}} \quad \textbf{and} \quad i_2 = \frac{g_{m2} v_{icm}}{1 + (g_{m1} + g_{m2})R_{SS}}$$

$$v_{o1} = -i_1 R_D = -\frac{g_{m1} v_{icm} R_D}{1 + (g_{m1} + g_{m2})R_{SS}}$$

$$v_{o2} = -i_2 R_D = -\frac{g_{m2} v_{icm} R_D}{1 + (g_{m1} + g_{m2})R_{SS}}$$

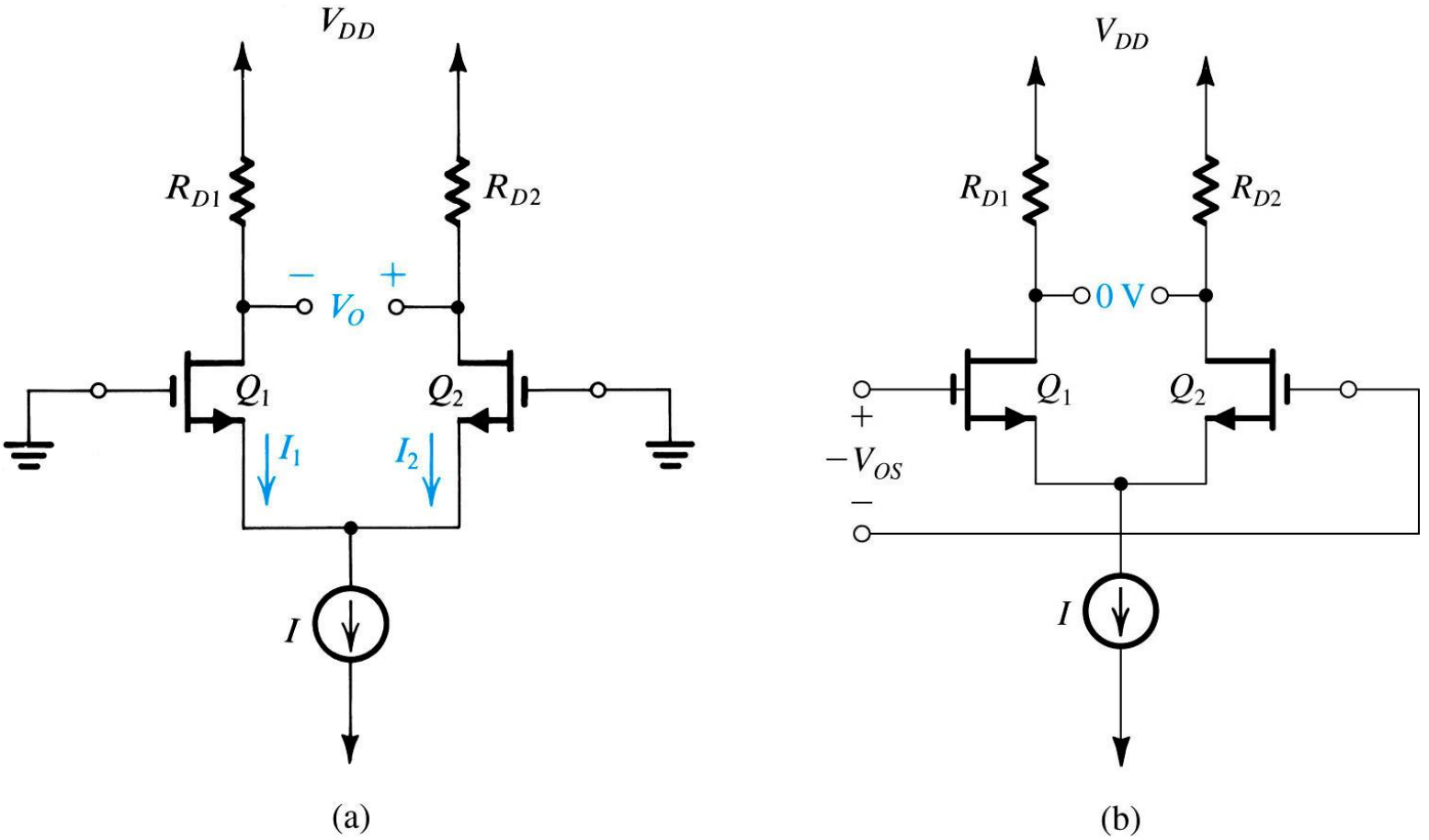
$$v_{od} = v_{o2} - v_{o1} = \frac{\Delta g_m R_D}{1 + (g_{m1} + g_{m2})R_{SS}} v_{icm} = \frac{\Delta g_m R_D}{1 + 2 g_m R_{SS}} v_{icm}$$

$$\Rightarrow A_{cm} = \frac{v_{od}}{v_{icm}} = \frac{\Delta g_m R_D}{1 + 2 g_m R_{SS}} \approx \frac{\Delta g_m R_D}{2 g_m R_{SS}} \quad (\because A_d = g_m R_D)$$

$$\text{CMRR} = \left| \frac{A_d}{A_{cm}} \right| = \frac{2 g_m R_{SS}}{(\Delta g_m / g_m)}$$

8.4 DC Offset

8.4.1 Input Offset Voltage of the MOS Differential Amplifier



•Output dc offset voltage Vo → Input referred dc offset voltage Vos

$$V_{os} = V_o / A_d \quad where \quad A_d = g_m R_D$$

(a) Mismatch in load resistance:

$$R_{D1} = R_D + \frac{\Delta R_D}{2} \quad \text{and} \quad R_{D2} = R_D - \frac{\Delta R_D}{2}$$

The output voltages:

$$V_{D1} = V_{DD} - \frac{I}{2}\left(R_D + \frac{\Delta R_D}{2} \right)$$

$$V_{D2} = V_{DD} - \frac{I}{2}\left(R_D - \frac{\Delta R_D}{2} \right)$$

$$\Rightarrow V_O = V_{D2} - V_{D1} = \frac{I}{2}\Delta R_D$$

On **the other hand,**

$$V_{OS} = V_O / A_d = \frac{\frac{I}{2}\ \Delta R_D}{g_{m,diff} R_D} = \frac{\left(\frac{I}{2}\right)}{\left(\frac{I}{V_{OV}}\right)} \frac{\Delta R_D}{R_D} = \left(\frac{V_{OV}}{2}\right) \cdot \frac{\Delta R_D}{R_D}$$

If V_{ov}=0.2V, mismatch in load resistance is +-1% ;i.e., $\frac{\Delta R_D}{R_D} = 0.02$

→$|V_{OS}|$=2mV

(b) Mismatch in W/L:

$$\left(\frac{W}{L}\right)_1 = \frac{W}{L} + \frac{1}{2}\Delta\left(\frac{W}{L}\right) = \frac{W}{L}\left[1 + \frac{\Delta(W/L)}{2\cdot(W/L)}\right] \quad \textit{and}$$

$$\left(\frac{W}{L}\right)_2 = \frac{W}{L} - \frac{1}{2}\Delta\left(\frac{W}{L}\right) = \frac{W}{L}\left[1 - \frac{\Delta(W/L)}{2\cdot(W/L)}\right]$$

makes

$$I_1 = \frac{I}{2}\left[1 + \frac{\Delta(W/L)}{2\cdot(W/L)}\right]$$

$$I_2 = \frac{I}{2}\left[1 - \frac{\Delta(W/L)}{2\cdot(W/L)}\right]$$

On the other hand,

$$V_{os} = \frac{V_o}{A_d} = \frac{(V_{DD} - I_2R_D) - (V_{DD} - I_1R_D)}{\left(\frac{I}{V_{OV}}\right)R_D} = \frac{(I_1 - I_2)}{I/V_{OV}} = \left(\frac{V_{OV}}{2}\right)\cdot\frac{\Delta(W/L)}{(W/L)}$$

(c) Mismatch in V_t:

$$V_{t1} = V_t + \frac{\Delta V_t}{2} \quad and \quad V_{t2} = V_t - \frac{\Delta V_t}{2}$$

$$\Rightarrow$$

$$I_1 = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t - \frac{\Delta V_t}{2})^2 = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2 [1 - \frac{\Delta V_t}{2(V_{GS} - V_t)}]^2$$

$$= I_D [1 - 2 \cdot \frac{\Delta V_t}{2(V_{GS} - V_t)} + \left(\frac{\Delta V_t}{2(V_{GS} - V_t)} \right)^2]$$

$$\approx \frac{I}{2} [1 - \frac{\Delta V_t}{(V_{GS} - V_t)}] = \frac{I}{2} [1 - \frac{\Delta V_t}{V_{OV}}]$$

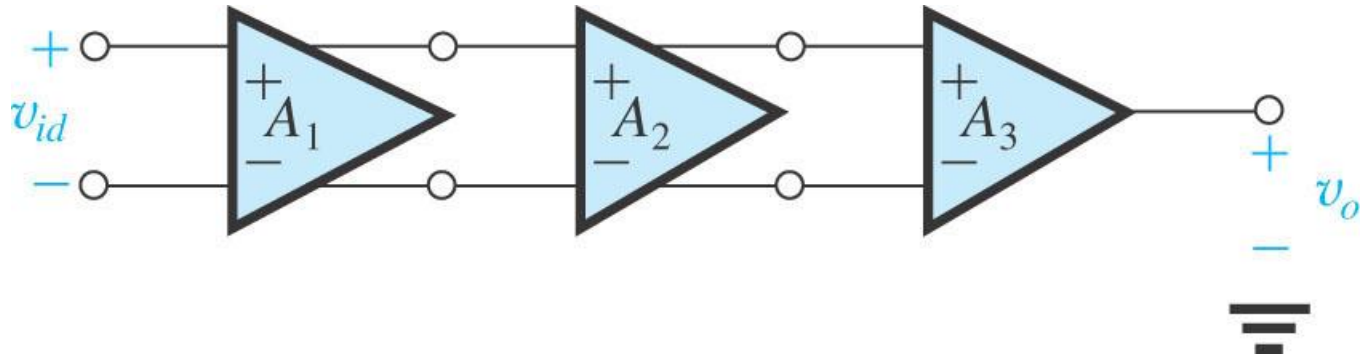
$$I_2 = \frac{I}{2} [1 + \frac{\Delta V_t}{(V_{GS} - V_t)}] = \frac{I}{2} [1 + \frac{\Delta V_t}{V_{OV}}]$$

$$Therefore, \; V_{OS} = \frac{V_O}{A_d} = \frac{I_1 - I_2}{(I / V_{OV})} = -\Delta V_t$$

By *rms* value:

$$V_{OS} = \sqrt{\left(\frac{V_{OV}}{2} \frac{\Delta R_D}{R_D} \right)^2 + \left(\frac{V_{OV}}{2} \frac{\Delta (W/L)}{(W/L)} \right)^2 + \left(\Delta V_t \right)^2}$$

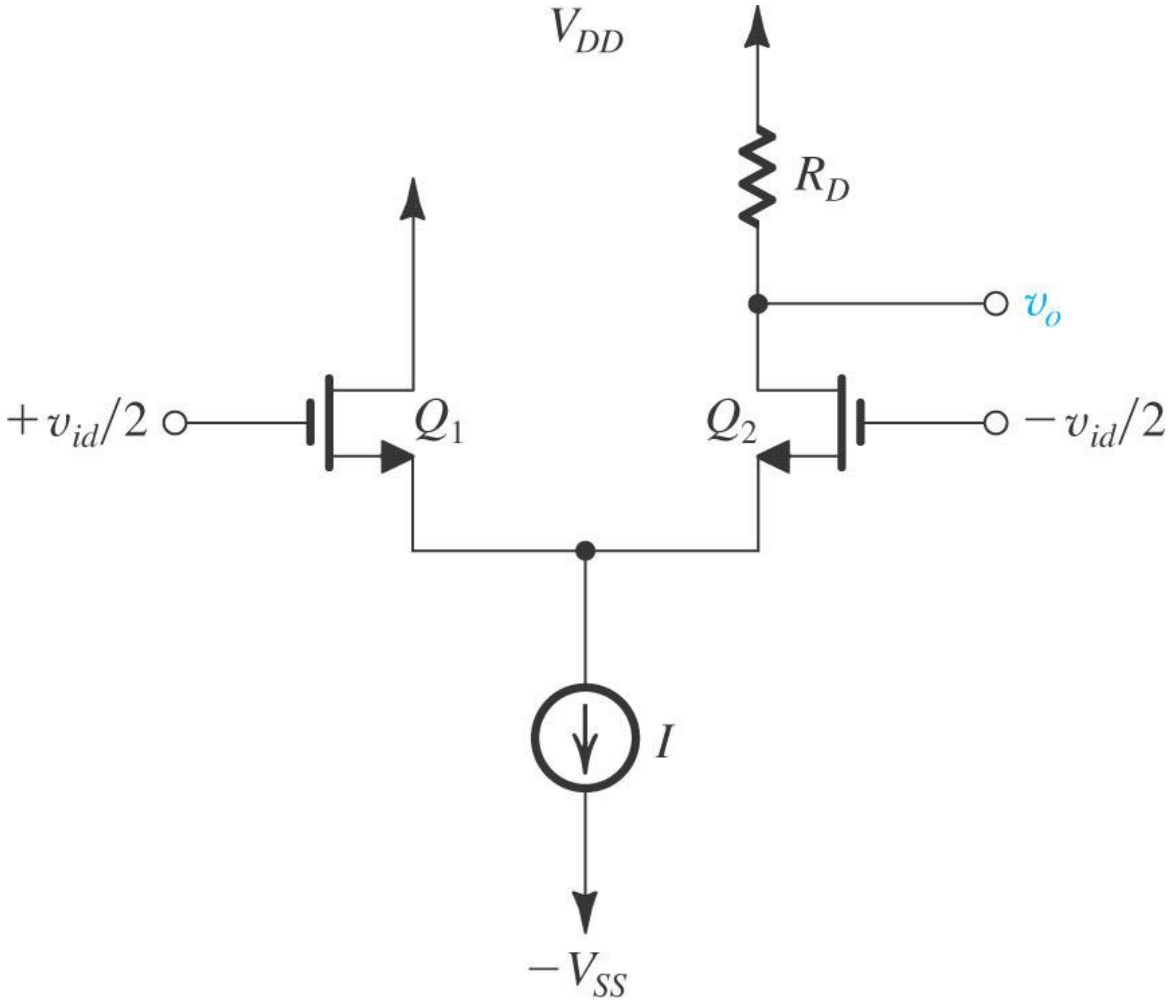
8.5 The Differential Amplifier with Current-Mirror Load



A three-stage amplifier consisting of two differential-in, differential-out stages, A_1 and A_2, and a differential-in, single-ended-out stage A_3.

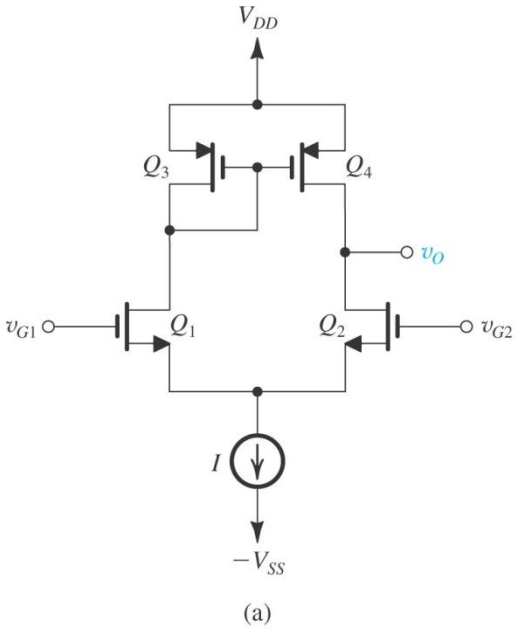
- Decrease common-mode gain and increase CMRR
- Differential gain increases by a factor of 2 (i.e.,6dB);

8.5.1 Differential to Single-Ended Conversion

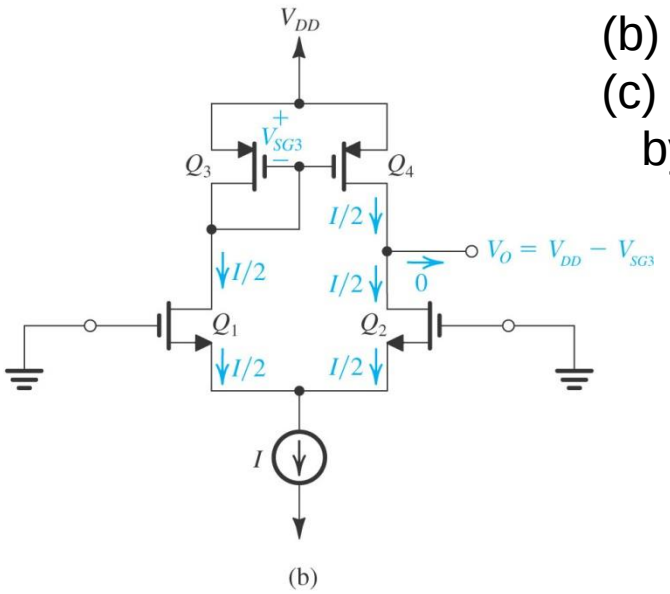


•Lose a gain by a factor of 2 (i.e.,6dB);

8.5.2 The Current-Mirror-Loaded MOS Differential Pair

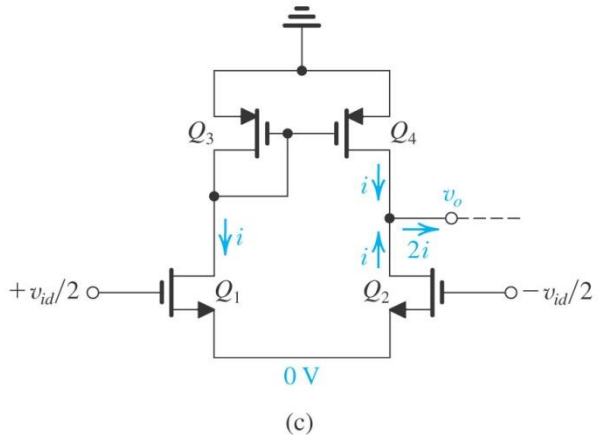


(a)

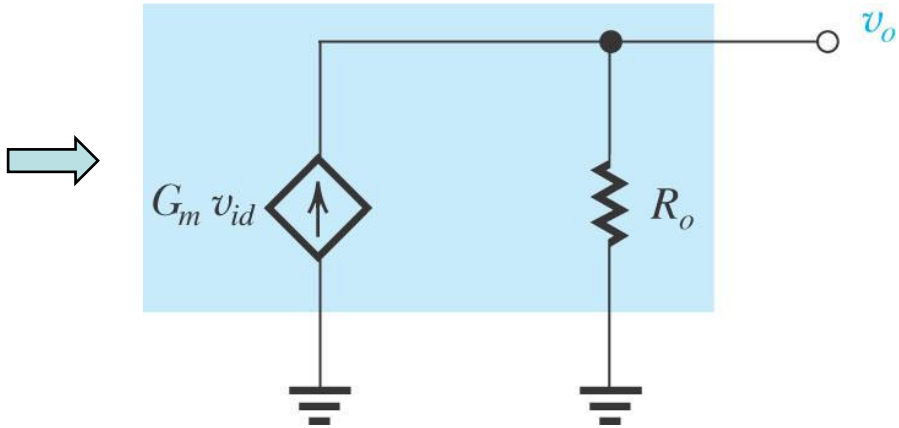


(b)

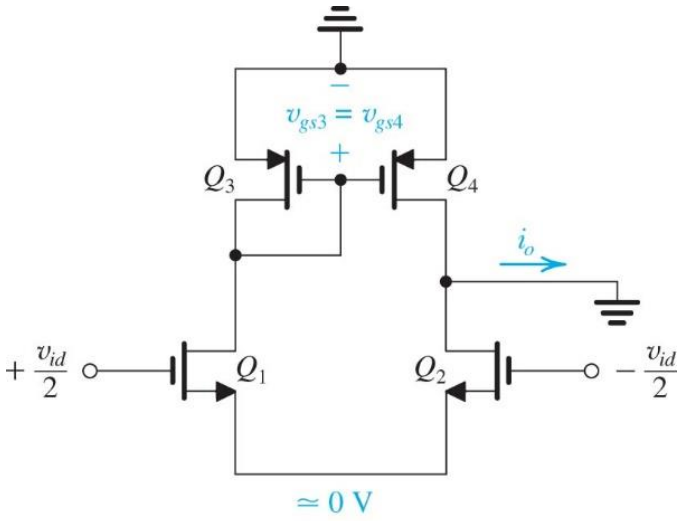
Note:
(b) Assume matched device;
(c) Output current: 2x I
by using a current mirror.



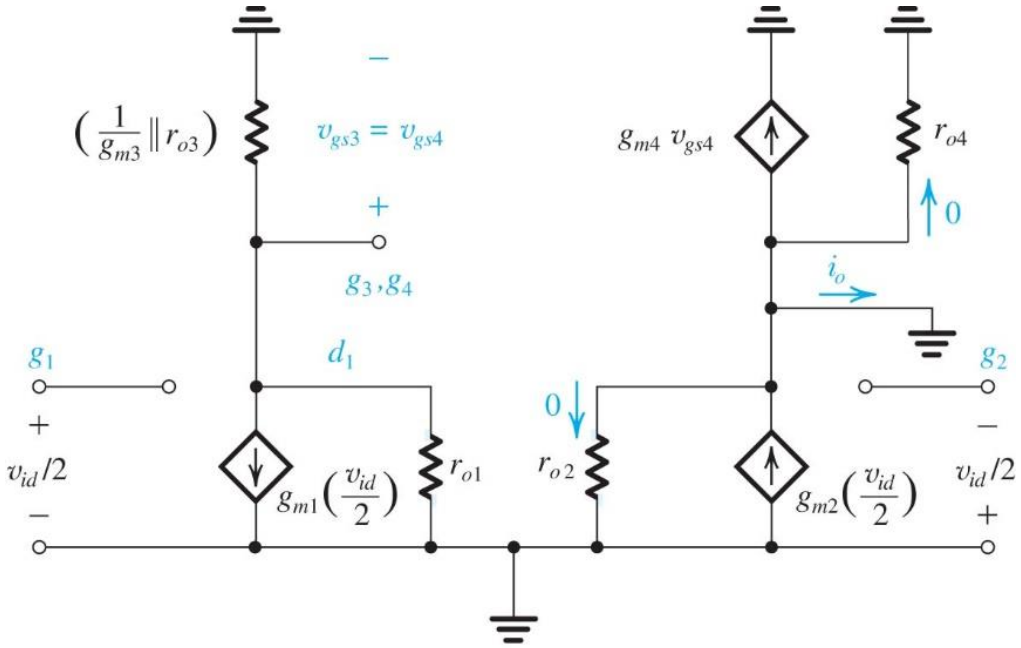
(c)



8.5.3 Differential Gain of the Current-Mirror-Loaded MOS Pair



(a)



(b)

$$v_{g3} = -g_{m1}(\frac{v_{id}}{2})\left(\frac{1}{g_{m3}} // r_{o3} // r_{o1}\right) \approx -\frac{g_{m1}}{g_{m3}}(\frac{v_{id}}{2})$$

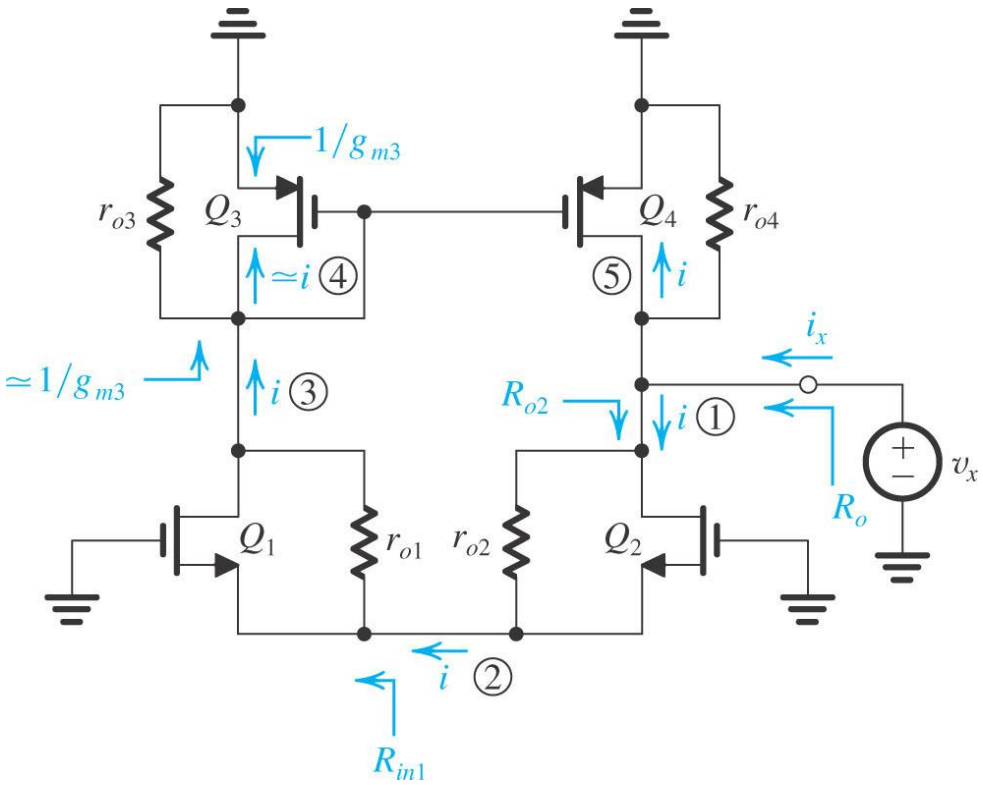
$$i_o = -g_{m4}v_{g3} + g_{m2}(\frac{v_{id}}{2}) \approx g_{m1}\left(\frac{g_{m4}}{g_{m3}}\right)\left(\frac{v_{id}}{2}\right) + g_{m2}\left(\frac{v_{id}}{2}\right) = g_m v_{id}$$

$(\because g_{m3} = g_{m4},\ g_{m1} = g_{m2} = g_m)$

the equivalent transconductance of the differential pair

$$G_m = g_m.$$

The output resistance R_o



$$R_{in1} = \frac{r_{o1} + R_L}{g_{m1} r_{o1}} = \frac{r_{o1} + 1/g_{m3}}{g_{m1} r_{o1}} \cong \frac{1}{g_{m1}}$$

$$R_{o2} = \frac{v_x}{i}$$

$$R_{o2} = r_{o2} + (1 + g_{m2} r_{o2})(\frac{1}{g_{m1}})$$

$$\cong 2 r_{o2}$$

for $g_{m1} = g_{m2} = g_m$ and $g_{m2} r_{o2} >> 1$.

Meanwhile,

$$i_x = i + i + \frac{v_x}{r_{o4}} = 2i + \frac{v_x}{r_{o4}}$$

$$= 2\frac{v_x}{R_{o2}} + \frac{v_x}{r_{o4}} = \frac{v_x}{r_{o2}} + \frac{v_x}{r_{o4}}$$

It makes

$$R_o \equiv \frac{v_x}{i_x} = r_{o2} // r_{o4}$$

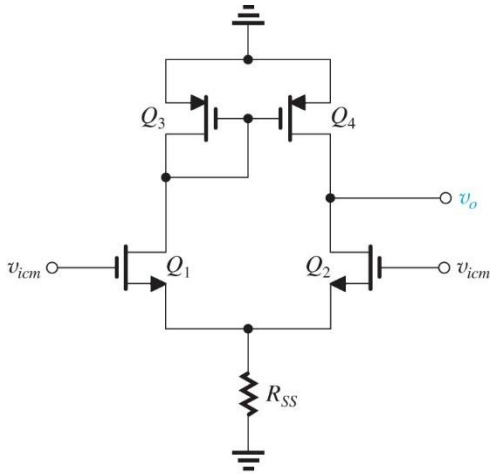
The differential gain

$$A_d \equiv \frac{v_o}{v_{id}} = G_m R_o = g_m (r_{o2} // r_{o4}) = g_m (\frac{r_o}{2}) = \frac{A_o}{2}$$

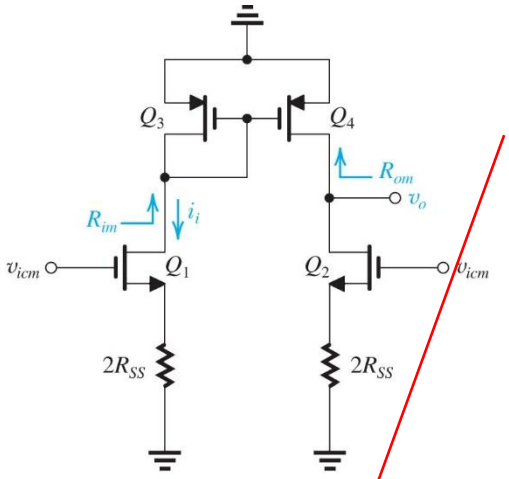
$$if \quad Q_1, Q_2, Q_3, and\ Q_4\ are\ identical!$$

Note: (a) A_o is the intrinsic gain of the MOS transistor;
(b) Using the differential pair with active load, the differential gain is half of the intrinsic gain of the MOS transistor, if Q_1, Q_2, Q_3, and Q_4 are identical.

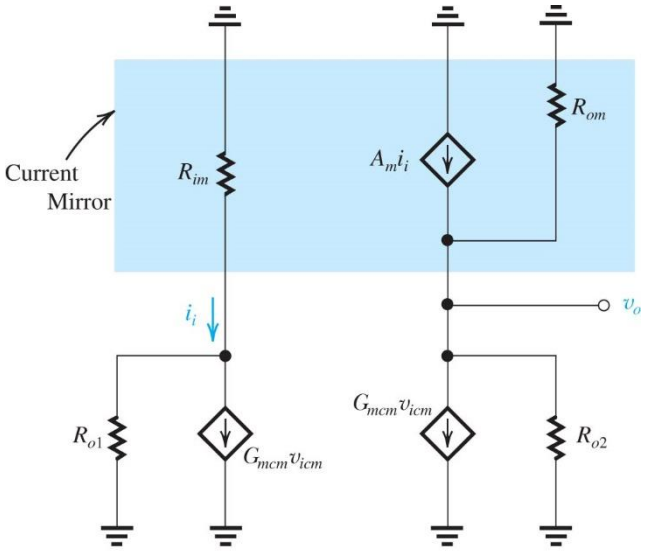
8.5.5 Common-Mode Gain and CMRR



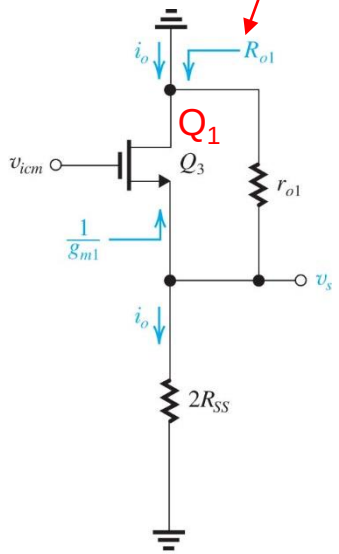
(a)



(b)



(c)



(d)

Calculate $G_{mcm} = \dfrac{i_o}{v_{icm}}$

$$v_s = i_o 2R_{SS}$$

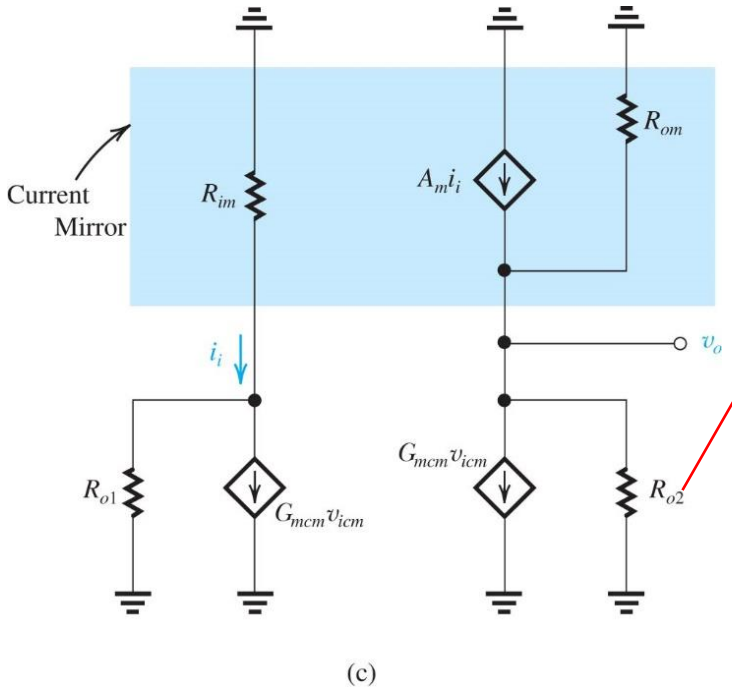
$$v_{icm} = v_{gs} + v_s$$

$$g_{m1} v_{gs} = \frac{v_s}{2R_{SS}} + \frac{v_s}{r_{o1}} = \frac{v_s}{2R_{SS} // r_{o1}}$$

$$v_{icm} = \frac{v_s}{2R_{SS} // r_{o1}} \frac{1}{g_{m1}} + v_s$$

$$\Rightarrow v_s = v_{icm} \frac{(2R_{SS} // r_{o1})}{(2R_{SS} // r_{o1}) + 1/g_{m1}} \approx v_{icm}$$

$$\Rightarrow G_{mcm} = \frac{i_o}{v_{icm}} = \frac{1}{2R_{SS}}$$



(c)

$$R_{o1} = r_{o1} + (1 + g_{m1} r_{o1}) \cdot 2R_{SS}$$

$$R_{o2} = r_{o2} + (1 + g_{m2} r_{o2}) \cdot 2R_{SS}$$

$$A_m i_i = -g_{m4} v_{gs4} = -g_{m4} v_{gs3}, \text{ if } g_{m3} = g_{m4}$$

$$v_{gs3} = -i_i R_{im} \Rightarrow A_m = g_{m4} R_{im} = \frac{1}{1 + 1/(g_{m3} r_{o3})}$$

$$R_{im} = \frac{1}{g_{m3}} \| r_{o3}, \quad R_{om} = r_{o4}, \quad G_{mcm} = \frac{1}{2R_{SS}}$$

$$A_{cm} = \frac{v_o}{v_{icm}} = -\frac{1}{1 + g_{m3} r_{o3}} G_{mcm} (R_{om} \| R_{o2})$$

$$R_{im} << R_{o1}$$

$$i_i \cong G_{mcm} v_{icm}$$

$$v_o = (A_m i_i - G_{mcm} v_{icm})(R_{om} \| R_{o2})$$

$$A_{cm} = \frac{v_o}{v_{icm}} = -(1 - A_m) G_{mcm} (R_{om} \| R_{o2})$$

$$A_{cm} \cong -\frac{1}{2 g_{m3} R_{SS}} \quad (\because r_{o4} << R_{o2}, g_{m3} r_{o3} >> 1)$$

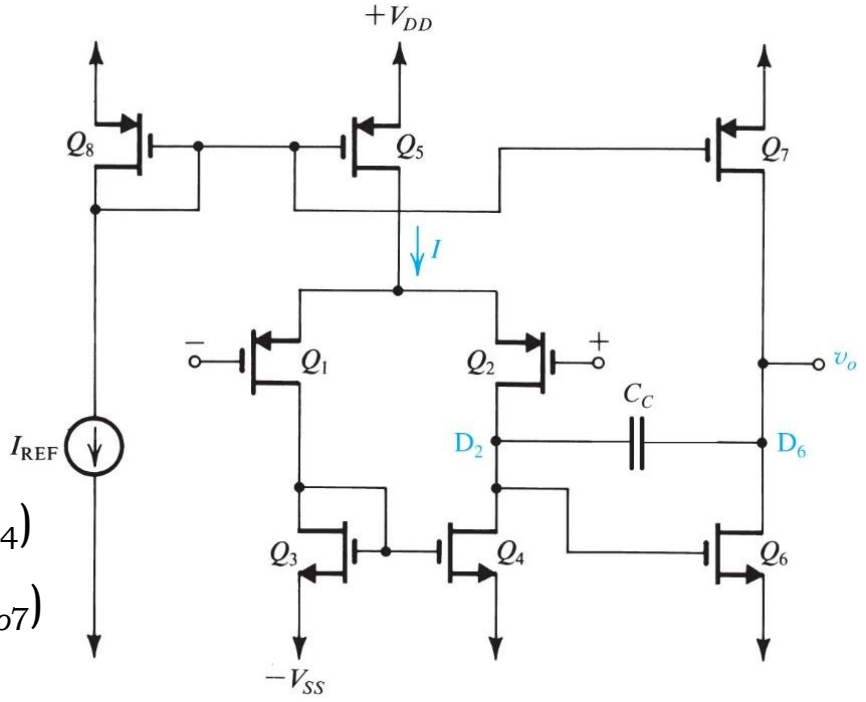
$$\text{CMRR} = \frac{|A_d|}{|A_{cm}|} = [g_m (r_{o2} // r_{o4})][2 g_{m3} R_{SS}]$$

For $r_{o2} = r_{o4} = r_o$ **and** $g_{m3} = g_m$,

$$\text{CMRR} = (g_m r_o)(g_{m3} R_{SS})$$

8.6 Multistage Amplifiers

8.6.1 A Two-Stage CMOS OP Amp



- Voltage gain
  - Voltage gain of 1st stage: $A_1 = -g_{m1}(r_{o2} \parallel r_{o4})$
  - Voltage gain of 2nd stage: $A_2 = -g_{m6}(r_{o6} \parallel r_{o7})$
  - DC open-loop gain: $A_v = A_1 \times A_2$
- Input offset voltage
  - *Random offset*: device mismatches as random in nature
  - Systematic offset: due to design technique ⇨ predictable

⇨ $$\frac{(W/L)_6}{(W/L)_4} = 2\frac{(W/L)_7}{(W/L)_5}$$ If this condition is not met, a systematic offset will result.

- C_C is Miller-multiplied by the gain of the second stage to provide the required dominant pole.