History of Phase-Locked Loop

- An early mechanical version of a phase-locked loop was used in 1921 in the Shortt-Synchronome clock.

Shortt clock in US National Institute of Standards and Technology museum, Gaithersburg, Maryland. This clock was purchased in 1929 and used in physicist Paul R. Heyl's measurement of the gravitational constant.

https://en.wikipedia.org/wiki/Shortt%E2%80%93Synchronome_clock

Shortt clocks kept time with two pendulums, a master pendulum swinging in a vacuum tank and a slave pendulum in a separate clock, which was synchronized to the master by an electric circuit and electromagnets. The slave pendulum was attached to the timekeeping mechanisms of the clock, leaving the master pendulum virtually free of external disturbances.

The master and slave pendulums were linked together in a feedback loop which kept the slave synchronized with the master.

Master pendulum tank

- Automatic synchronization of electronic oscillators was described in 1923 [1]

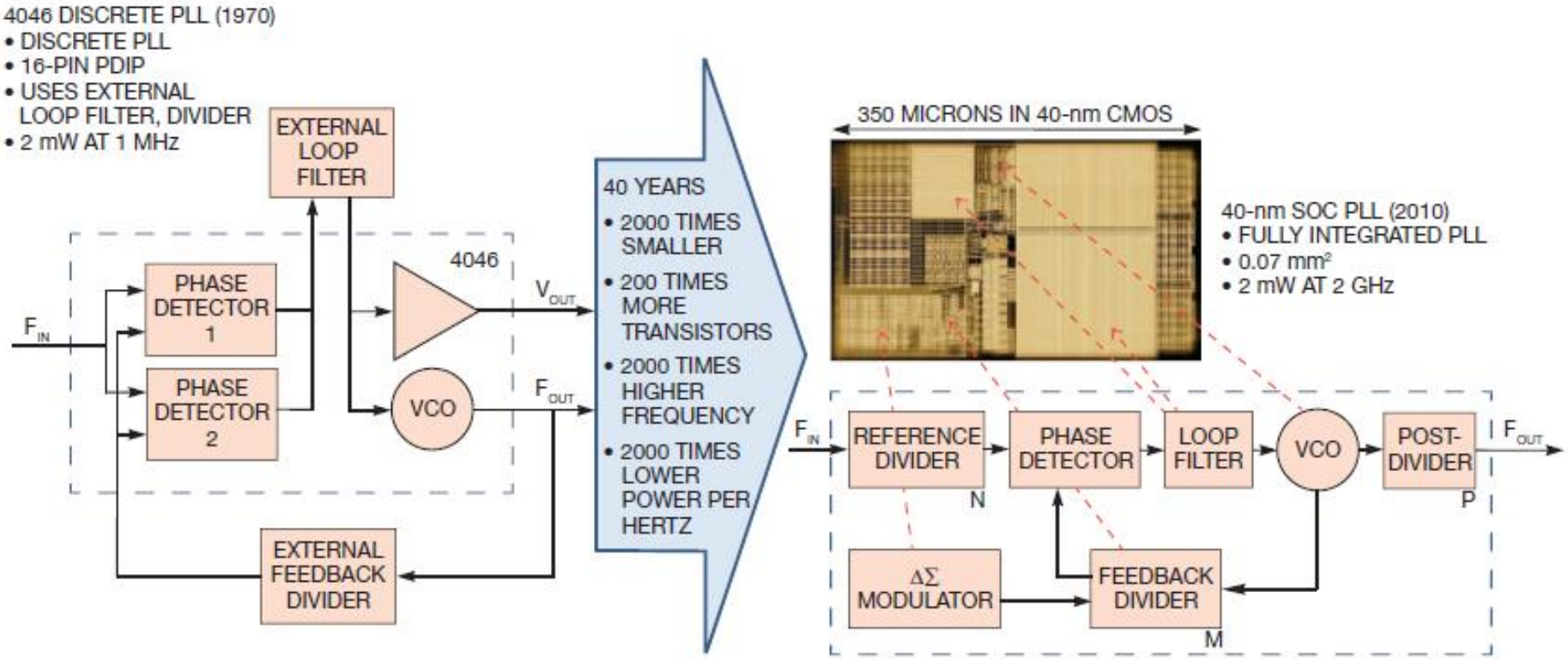
[1] E. V. Appleton, *Automatic synchronization of triode oscillators*, Proc. Cambridge Phil. Soc., 21(Part III):231 (1922-1923)

- In 1932, British researchers developed an alternative to Edwin Armstrong's superheterodyne receiver, the Homodyne or direct-conversion receiver.

- The technique was described in 1932, in a paper by Henri de Bellescize, in the French journal *L'Onde Électrique*.

- A. B. Grebene, H. R. Camenzind, “Phase Locking As A New Approach For Tuned Integrated Circuits”, ISSCC, pp. 100-101, Feb. 1969.

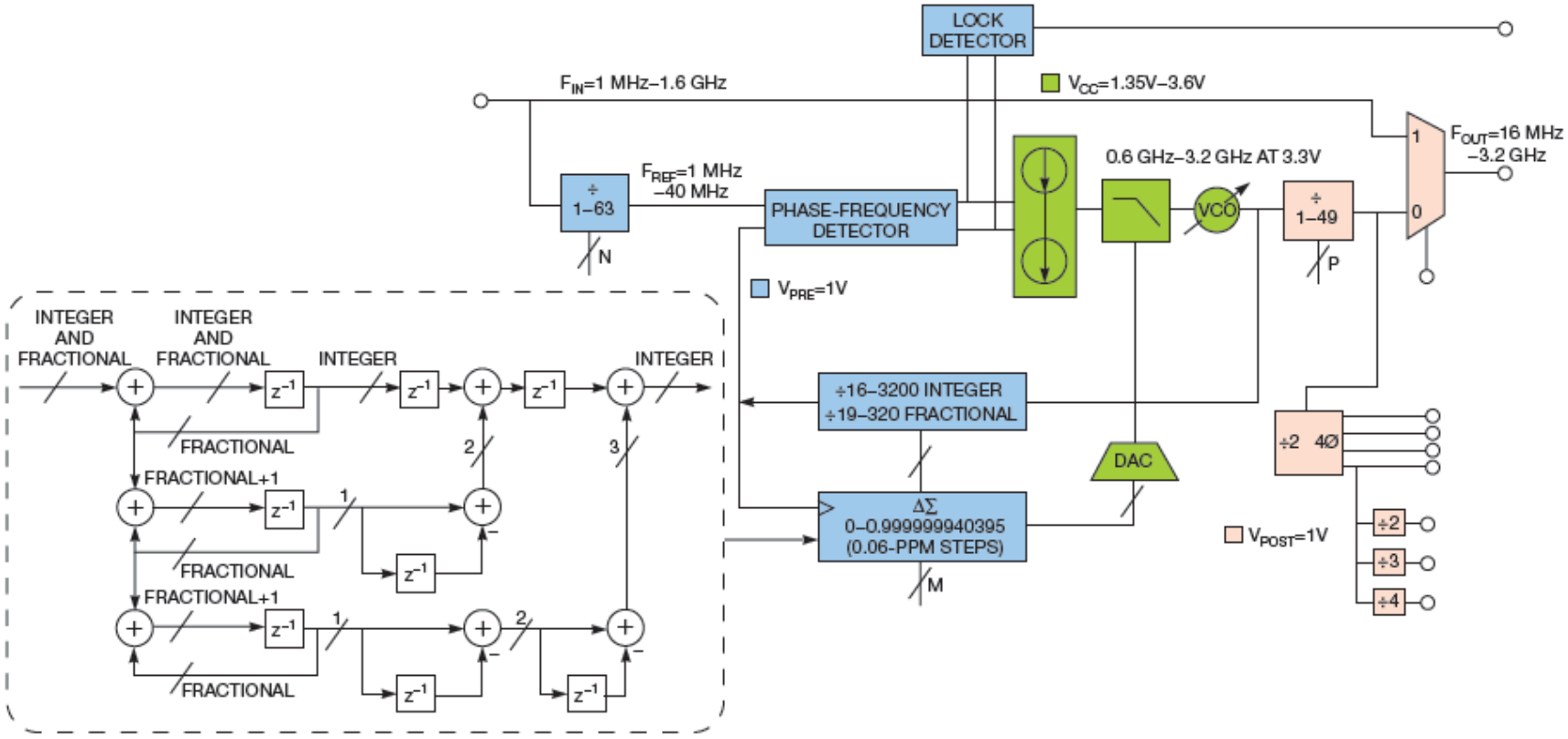
- In 1970s, RCA introduced the "CD4046" CMOS PLL.



Jeff Galloway and Andrew Cole, “Tracking PLL design through the decades “, EDN July 14, 2011

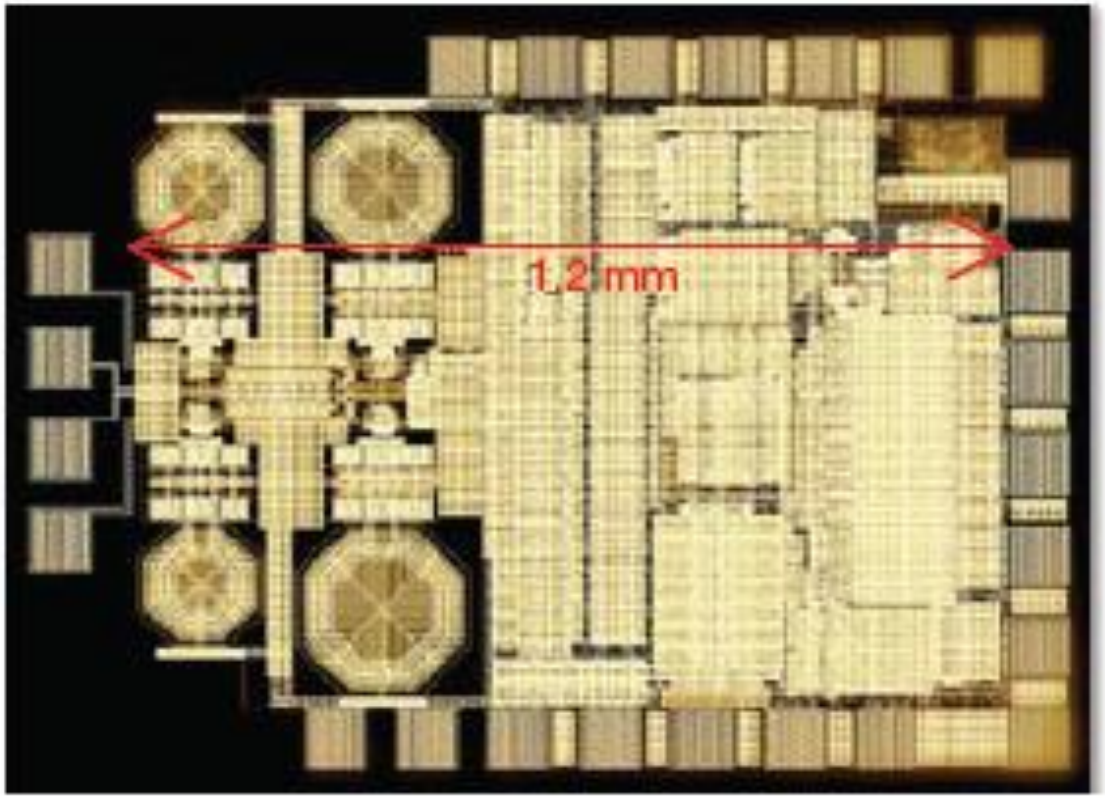
■Breakthrough

A fractional-N PLL in 1993 adopted delta-sigma modulation to the dithering of the feedback divider

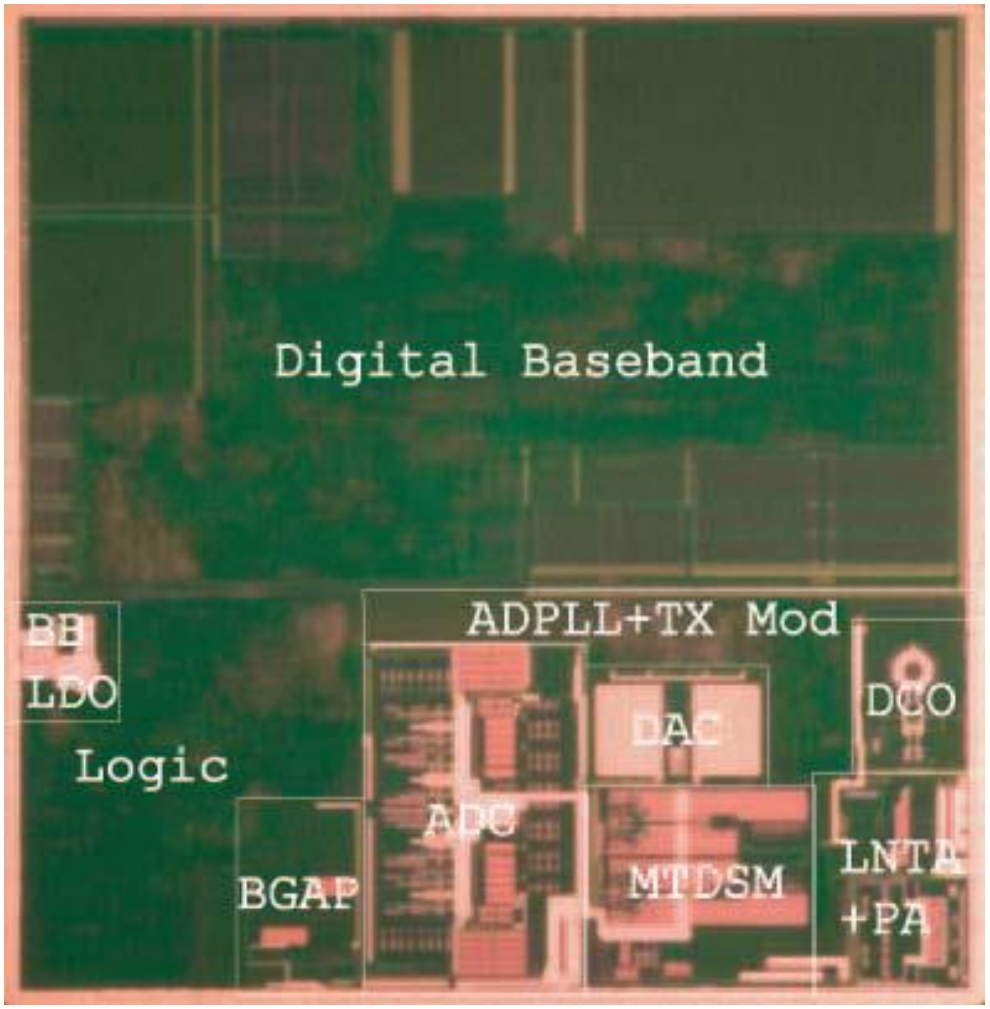


T. Riley, M. A. Copeland; and T. A. Kwasniewski, “Delta-sigma modulation in fractional-N frequency synthesis,” IEEE Journal of Solid-State Circuits, Vol.5, , pp. 553-, May 1993.

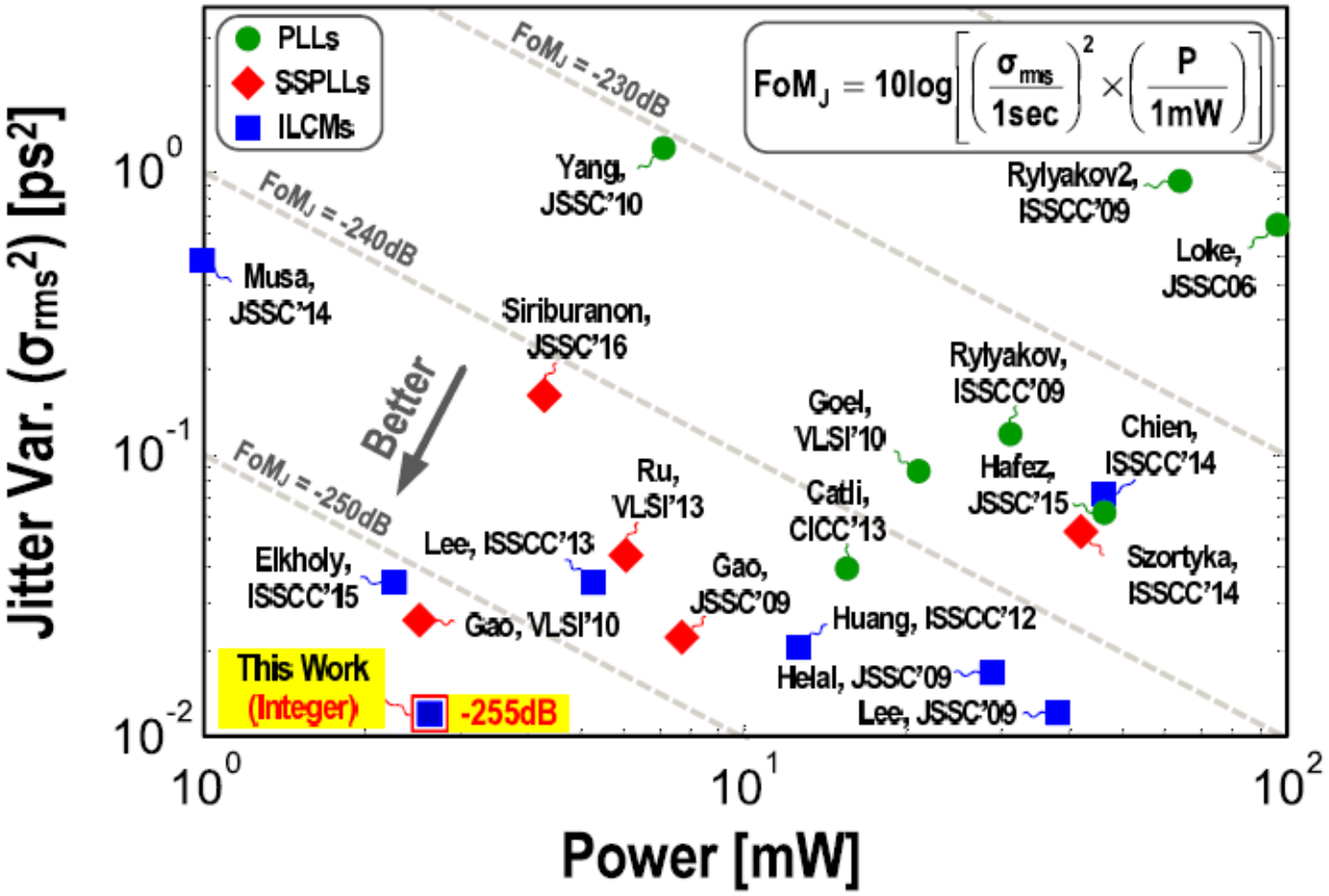
■ In the early ’90s, IC designers began to incorporate passive inductors into ICs fabricated in generic CMOS-logic processes



■2002 TI Bluetooth SoC in 130 nm using an all-digital PLL

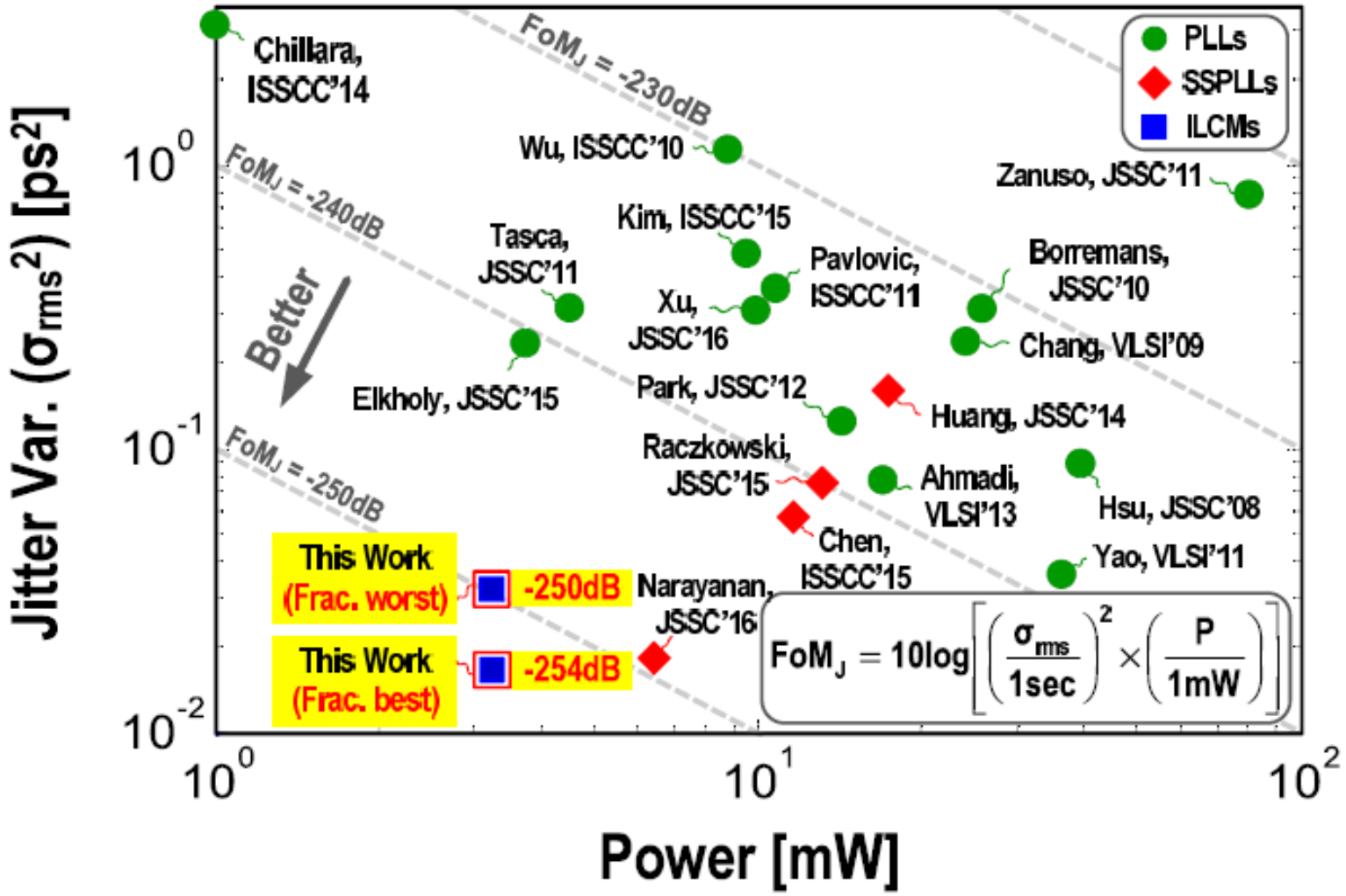


FOM; An integer-N PLL



IEEE JSSC, pp.1818-, June 2018

FOM; A Fractional-N PLL



IEEE JSSC, pp.1818-, June 2018