Low-Voltage CMOS Frequency Synthesizer for ERMES Pager Application

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***Abstract*—A low-voltage frequency synthesizer fabricated with a 0.35-μm standard CMOS technology is presented. A1-V dual-modulus prescaler using the dynamic back-gate forward bias method has been developed for low-voltage operation. The prescaler, including a preamplifier, measured at 1-V supply voltage has a maximum operating frequency of 170 MHz, and its power dissipation is only 0.9 mW. The voltage-controlled oscillator (VCO) in the frequency synthesizer is an *LC*-tank based oscillator. When locked at the oscillation frequency of 148 MHz, the measured phase noise of the VCO is −106 dBc/Hz at 100-kHz from the carrier. The whole power consumption of the frequency synthesizer is 10.5 mW.**

I. Introduction

IN MODERN communications, the phase-locked loop (PLL) based frequency synthesizer is an important building block for frequency translation. The high-speed prescaler and voltage-controlled oscillator (VCO) are two critical components in a frequency synthesizer. Although they have usually been implemented in bipolar or GaAs technologies before, advanced standard CMOS technology has been widely used to design such circuits for several years in order to realize single-chip RF-to-baseband systems [1], [2].

One of the important design goals of the synthesizer is low power consumption for battery-operated portable applications. For CMOS digital circuits, the dynamic power dissipation is proportional to the square of supply voltage and thus the goal can be efficiently achieved by lowering the supply voltage. For example, a 1-V frequency synthesizer implemented in a special CMOS process has been used for pager systems [3]. However, $V_{\rm DD}$ can't be lowered further as further reduction in threshold voltage is not easy because of the exponentially increasing subthreshold leakage current. For example, the typical threshold voltages of the NMOS and PMOS transistors in our 0.35-μm technology are 0.55 and −0.7 V, respectively. Thus, the operating speed of low-voltage digital circuits will be limited. Recently, a novel back-gate forward bias (BGFB) scheme has been introduced as an efficient tradeoff between operating speed and subthreshold leakage current [4]–[7]. This circuit technique can be used in present standard bulk CMOS processes to reduce the threshold voltage electrically without any mask or process modifications.

In this paper, low-voltage static and dynamic logic circuits using a dynamic BGFB method are presented. A novel DFF using this technique is also proposed. A low-voltage dual-modulus prescaler using the proposed DFFs has been fabricated in a standard 0.35-μm CMOS technology. Besides, a frequency synthesizer for European Radio Message System (ERMES) pager application with the proposed prescaler is also implemented. It integrates a *LC*-tank based VCO using an external inductor.

The paper is divided into four additional parts. Section II describes the conventional BGFB method and the proposed dynamic BGFB technique. Section III describes the components in the synthesizer, including the proposed dynamic BGFB prescaler. Section IV describes the measured results. Finally, Section V gives the conclusions.

II. New Dynamic Back-Gate Forward Bias Method

Some experimental results about the conventional BGFB method have been presented in [4]. A few important conclusions are briefly introduced below. In circuit designs, we often short the source and the body of MOS transistors or reverse bias the diode formed between the MOS source and bulk. However, take a NMOS transistor for example, if we forwardly bias the body-source p-n junction by adding a small voltage on the body with respect to the source, there is a small increase in the drain current. This result can be viewed as a reduction in effective threshold voltage V_t. The scheme is called back-gate forward bias method. To understand the advantage of BGFB, the fall time of a CMOS inverter is listed below [8]

$$t_{PHL} = \frac{C}{K_n(V_{DD}-V_t)} \cdot\left[\frac{V_t}{V_{DD}-V_t}+\frac{1}{2}\ln\left(\frac{3V_{DD}-4V_t}{V_{DD}}\right)\right] \quad (1)$$

where $K_n = 1/2(\mu_n C_{ox} W/L)$ and C is the load capacitor. This equation can reduce to be $C/(K_n V_{\rm DD})$ and $0.8C/(K_n V_{\rm DD})$ when $V_t = 0.3V_{\rm DD}$ and $V_t = 0.2V_{\rm DD}$, respectively. It is obvious that the delay of a CMOS inverter can be reduced when V_t is decreased. Thus, reducing effective V_t using the BGFB method can reduce the rise time and the fall time of a logic gate, and thus the operating speed of digital circuits can be increased, especially at low supply voltage. However, the small forward bias voltage should not be larger

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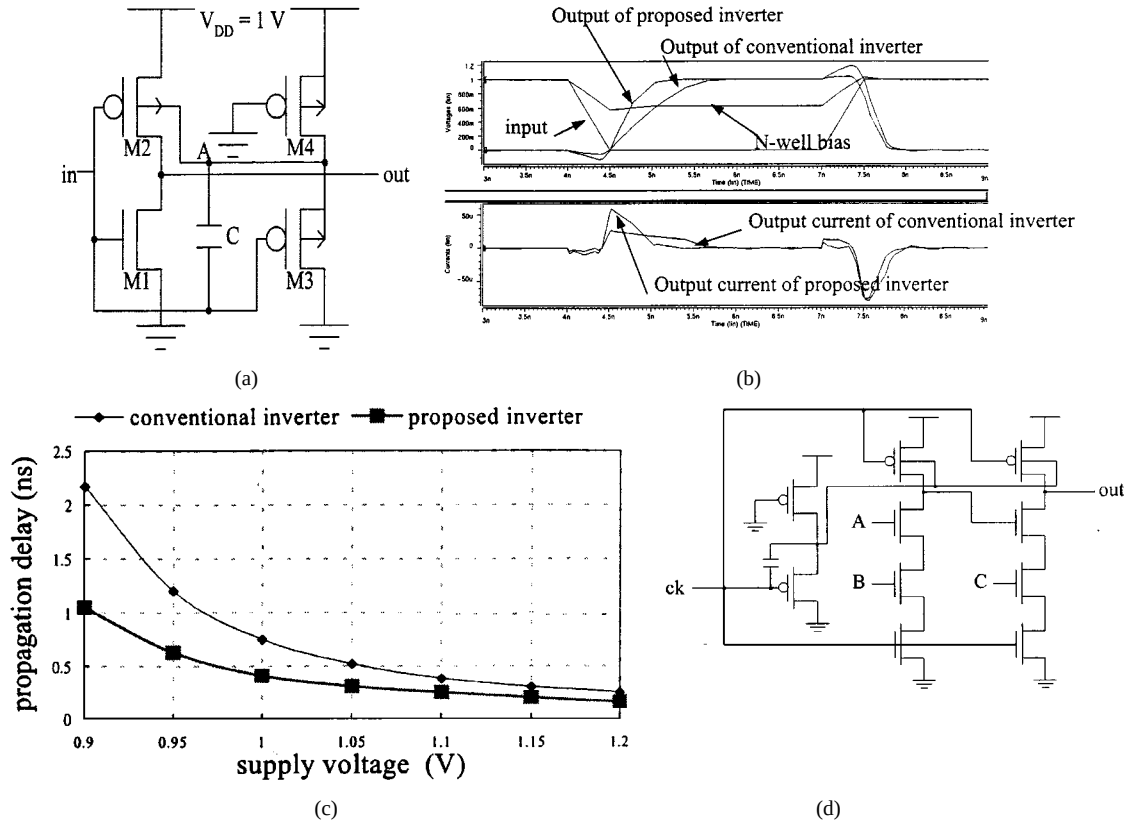


Fig. 1. Improved inverter using the dynamic BGFB method. (a) Schematic. (b) Transient response. (c) Propagation delay. (d) Dynamic logic gate with dynamic BGFB.

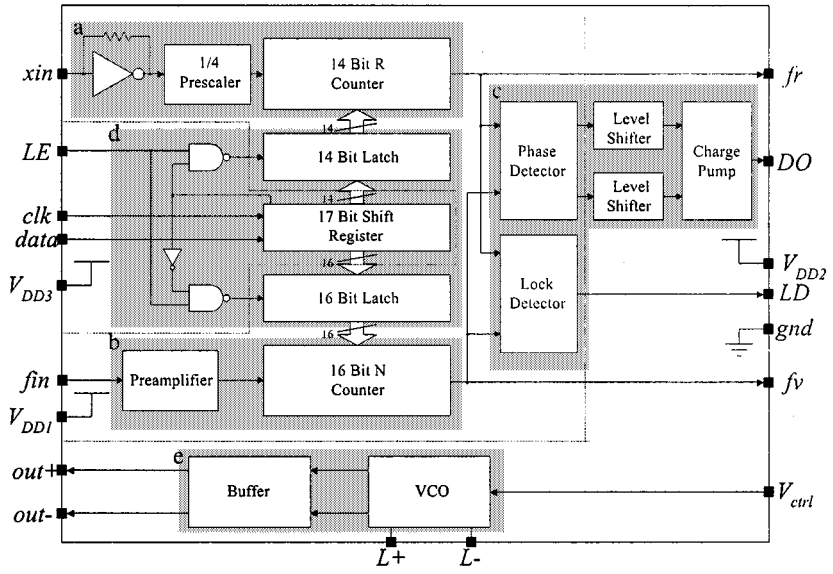


Fig. 2. Functional block diagram of the frequency synthesizer.

than 0.4 V in order to prevent latch-up and other undesired effect [4]–[6].

Since the bottleneck of the operating speed of low-voltage digital circuits depends on the PMOS transistors, whose mobility is only about half of the NMOS ones and threshold voltage is usually larger than the NMOS ones, it is more efficient to apply the BGFB method to PMOS transistors only. Besides, although applying the BGFB method stated above on low-voltage circuit design is capable of increasing the operating frequency, it still consume excess power dissipation because of the resultant larger leakage current when the PMOS transistors are cutoff. Therefore, a more efficient bias scheme, called dynamic BGFB method, which only forward biases the PMOS transistors when they are turn-ON is presented [7].

Fig. 1(a) is the proposed 1-V dynamic BGFB inverter. M1 and M2 form a conventional CMOS inverter, and M3 and M4 form a source follower to dynamically bias the body of M2 (n-well). When the input of the inverter goes low, M3 and M4 turn ON, and

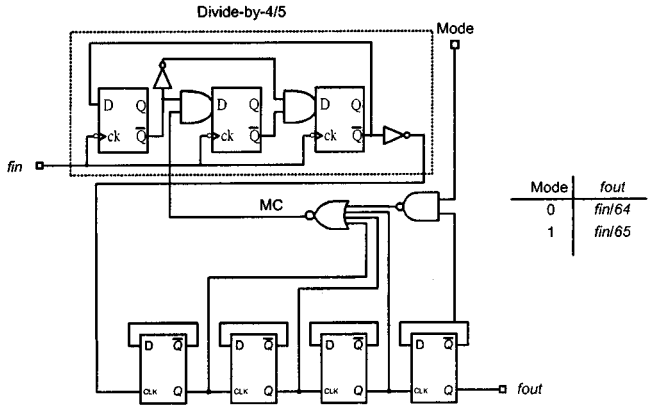


Fig. 3. Functional block diagram of the dual-modulus prescaler.

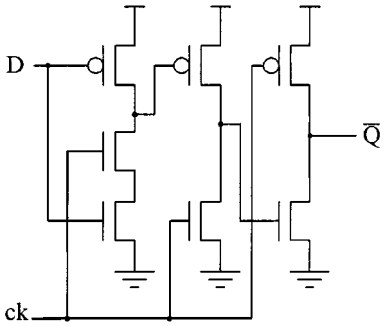


Fig. 4. The 7-transistor DFF proposed in [1].

then the body of M2 will follow the input and become lower. M3 is designed to have a small $V_{\rm SG}$ of 0.6∼0.7 V, thus $V_{\rm SB}$ of M2 is about 0.3∼0.4 V, which can electrically reduce the threshold voltage of M2. In this instance, the PMOS transistor, M2, can deliver a larger drain current to the output capacitor than a conventional inverter does, and reduce the propagation delay of the gate. When the input starts to go high, M3 turns OFF then the body of M2 is pulled back to $V_{\rm DD}$ by M4. The threshold voltage of M2 returns to the normal value again. Therefore, with the dynamic BGFB method, M2 is able to pull up faster and turn OFF normally without excess leakage current. The capacitor C, can be added to improve the switching speed of the body of M2. When input is low, there will be a voltage drop of 0.6 V stored on the capacitor, C. As the input starts to go high again, the voltage of n-well will be pushed higher quickly as the voltage drop across the capacitor will try to remain unchanged. The required value of the capacitor depends on the parasitic capacitance of the n-well. From another point of view, the capacitor, C, and M4 can be regarded as a highpass filter, which directly couples the input signal to the substrate of M2. M4 also helps to keep the substrate bias voltage above 0.6 V, and thus latch-up can be avoided.

The 1-V dynamic BGFB inverter is compared to a conventional CMOS inverter by simulations. Fig. 1(b) gives the simulated transient response of the two inverters. The difference between the propagation delays of the two inverters is also compared in Fig. 1(c).

Moreover, the dynamic BGFB scheme presented here can be also applied to the dynamic logic circuit design. Fig. 1(d) shows a typical dynamic logic circuit with the dynamic BGFB applied. The n-well bias is now dynamically controlled by the clock signal. When "ck" is high, the circuit is in the "evaluation mode," and the n-well is biased at 1 V to make the PMOS subthreshold leakage current as low as possible. When "ck" starts to go low, the circuit enters the "precharge mode," and the output node of each stage has to be charged to $V_{\rm DD}$ via the PMOS transistors. The n-well is now biased at 0.6 V to reduce PMOS transistor's effective threshold voltages. Thus, the precharge time can decrease and the operating frequency of the dynamic circuit can increase. Since all of the PMOS transistors can be laid out in a single well, only one bias circuit is needed.

To conclude, the dynamic BGFB method can be applied to both low-voltage static and dynamic logic circuits to improve operating frequency. A new D flip-flops (DFF) using the method will be discussed in the next section.

III. Low-Voltage Frequency Synthesizer

A low-voltage single-chip frequency synthesizer for ERMES pager application with the proposed dynamic BGFB method is designed. The channel bandwidth of ERMES pager is 25 kHz. The radio band frequency is 169.4125∼169.8125 MHz in Taiwan, and the first IF frequency is 21.4 MHz. Thus, the local oscillator (LO) tuning range must be able to cover 148.0125∼148.4125 MHz. Fig. 2 shows the functional block diagram of the whole synthesizer. There are three sets of supply voltages in the synthesizer chip. V_{DD1} is the supply voltage for the 1-V circuits, including the dividers, preamplifiers, and PFD. V_{DD2} is the supply voltage for charge pump and VCO. In order to achieve better signal to noise ratio and provide a wider tuning range, the VCO is designed to operate at a higher supply voltage of 3 V. V_{DD3} is the supply voltage for shift register. The signal levels of the microcontroller that programs the synthesizer determine V_{DD3}. The components used in the synthesizer are described below.

A. Low-Voltage Back-Gate Forward Bias Dual-Modulus Prescaler

Fig. 3 shows the schematic of the low-voltage dual-modulus prescaler. The dual-modulus divide-by-64/65 prescaler consists of a synchronous divide-by-4/5 counter, an asynchronous divide-by-16 counter and a few static gates. When mode is one (zero), the divide ratio is 65 (64). A new dynamic DFF using the dynamic BGFB method is developed here for low-voltage operation.

1) Low-Voltage Back-Gate Forward Bias DFF: True single-phase clock (TSPC) DFFs have been widely used in many digital circuit designs [9] because of their high operating speed and simple circuits required. Much work has been done to improve the performances of TSPC DFFs [1], [2]. Among them, a 7-transistor ratioed version, as shown in Fig. 4, has been proposed in [1]. It replaces the N-precharge stage and the P-C^{2}MOS [1], [9] stage in a negative-triggered TSPC DFF [9] by two pseudo-nMOS inverters to form a ratioed latch. Instead of the stacked structures in TSPC circuits, no serial transistors are used in the latch, thus the RC time constant can be reduced. Therefore, this DFF with a ratioed latch has the better frequency re-

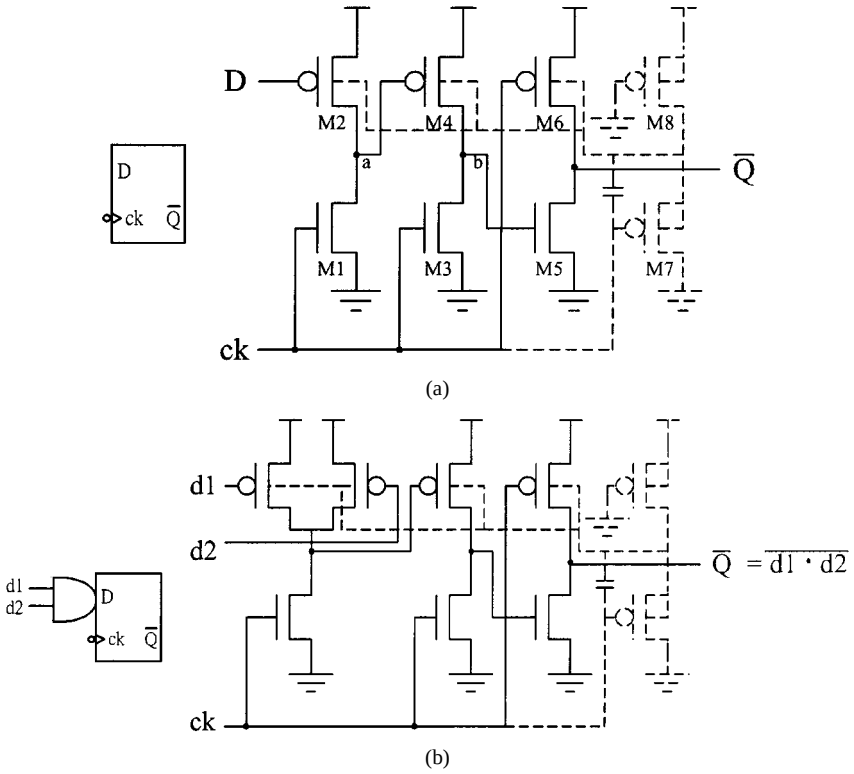


Fig. 5. (a) Circuit schematic of the proposed dynamic BGFB DFF. (b) Circuit schematic of the proposed dynamic BGFB and LFF.

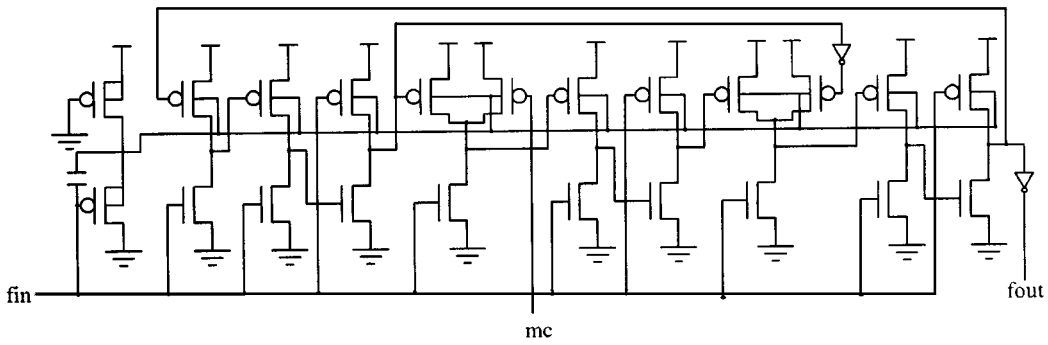


Fig. 6. Low-voltage divide-by-4/5 prescaler using the dynamic BGFB method.

sponse then the conventional TSPC DFFs and it is more suitable for low-voltage operation.

Further, we can replace the N-C^{2}MOS stage in Fig. 4 by another pseudo-nMOS inverter. This becomes a new low-voltage dynamic DFF as shown in Fig. 5(a). The operation principles of this DFF can be briefly described below:

1) When "ck" is high, the circuit is in the "hold" mode. The signal, "ck," will turn OFF M6, and M3 turns ON to discharge node "b" to low (i.e., below V_{tn} of M5) in order to turn OFF M5. Since both M5 and M6 are cutoff now, the data at node $\overline{Q}$ can be held. M1 must be also turned ON to predischarge node "a" to low regardless of the input D.
2) When "ck" goes low, the DFF enters into the "evaluation" mode. If the input D is high (i.e., above $V_{\rm DD} - |V_{tp}|$) in this instant, both of M1 and M2 are turned OFF and node "a" will remain low. Since M3 also turns OFF now, M4 can pull up node "b" to $V_{\rm DD}$ easily and then node "$\overline{Q}$" is discharged to low through M5.
3) If D is low (i.e., below $V_{\rm DD} - |V_{tp}|$) as "ck" goes low, M2 will pull up node "a" quickly to turn OFF M4. Since M3 is also cutoff now, node "b" can remain low to keep M5 OFF. Therefore, node "$\overline{Q}$" can be charged to $V_{\rm DD}$ through M6 now.

However, in order to make the ratioed flip-flop to operate correctly as stated above, careful design must be done to ensure that the NMOS transistors have larger pull-down capability than the pull-up capability of the PMOS transistors. Besides, the high level of "ck" must be larger than $V_{\rm DD} - |V_{tp}|$ and the low level must be smaller then V_{tn}. The DFF presented here has the same functions as conventional TSPC DFFs but it is faster, especially when operating at low supply voltage. That is because only six transistors and no stacked structures are used. Besides, if there are some logic gates required in front of the DFFs in circuit designs, one can also include the gates into the flip-flops to form a logic flip-flop (LFF). Fig. 5(b) is an example of such a LFF, which combines an AND gate and a DFF.

TABLE I
SOME FEATURES OF THE PRESCALER PROPOSED

	transistor count	Clocked transistor count **	power dissipation
TSPC *	41	12	18.1μW @ 100MHz
Proposed	24 and a capacitor	10 and a capacitor	18.7μW @ 100MHz

* The prescaler using TSPC DFFs and static AND gates

** The number of the transistors connected to the clock signal

Finally, the body-biased scheme stated in the last section can also be applied to the DFF as shown by the dashed lines in Fig. 5. Now, the V_{SB} of the PMOS transistors is dynamically controlled by "ck." In the "hold" mode, i.e., "ck" is high, "ck" turns OFF M7 and then the body bias of PMOS transistors, V_{BP}, is pulled up to V_{DD}. This makes the threshold voltages of the PMOS transistors return to the normal value. There are two reasons to do it. 1) If the data stored in $\overline{Q}$ is 0 now, the node "$\overline{Q}$" instead of being at Vss, is pulled up toward V_{DD} due to the large leakage current of M6. Biasing the body of the PMOS transistors at V_{DD} can eliminate the large leakage current, and the minimum operating frequency of the circuit can be decreased. 2) M4 is always turned ON in this mode and M2 may also be turned ON by the node "D" if "D" is low. Increasing their threshold voltages can reduce the drain currents of M2 and M4. Therefore, the pull-down ability of M1 and M2 will not be influenced, and the power dissipation is also reduced.

When the DFF is in its "evaluation" mode, i.e., "ck" is low, both of M7 and M8 turn ON. The body of the PMOS transistors is biased at about 0.6 V in order to reduce the effective threshold voltage of the PMOS transistors. This is because either of M2 and M4 must pull up its drain from low to high rapidly in this instant, and M6 may also have to charge the node "$\overline{Q}$" from low to high if D is low now. Therefore, by decreasing the effective threshold voltage of the PMOS transistors, the time needed for PMOS transistors to pull up their output nodes can be shorten, and the operating frequency of the circuit can increase.

All of the three PMOS transistors in the DFF (M2, M4, and M6) are laid out in the same n-well and only one bias circuit (M7 and M8) is used to control their back-gate forward bias voltage.

2) Synchronous Divide-by-4/5 Counter: A 1-V dual-modulus divide-by-4/5 prescaler using the proposed DFFs and LFFs is shown in Fig. 6. All of the PMOS transistors are in the same n-well and only one bias circuit is used to control the bias voltage of the n-well. The well is biased at 1 V when "ck" is 1 and at 0.6 V when "ck" is 0.

Simulation results show that maximum operating frequency of the prescaler without the dynamic BGFB method is about two times of the conventional one using TSPC DFFs [9] and static AND gates at 1-V supply voltage. If the body-biased scheme is applied to the PMOS transistors, the speed can even be improved three times of the TSPC circuits. The other features of the prescaler are also summarized in Table I, including the required transistor count (area), the number of the transistors connected to the clock signal (clock load), and the simulated power dissipation at 100-MHz frequency.

3) Asynchronous Divide-by-16 Counter: As shown in Fig. 3, the asynchronous counter consists of four toggle flip-flops (TFFs) [1]. Since the maximum operating frequency of it is only one-fourth that of the divide-by-4/5 prescaler, conventional TSPC DFFs [9] are used here.

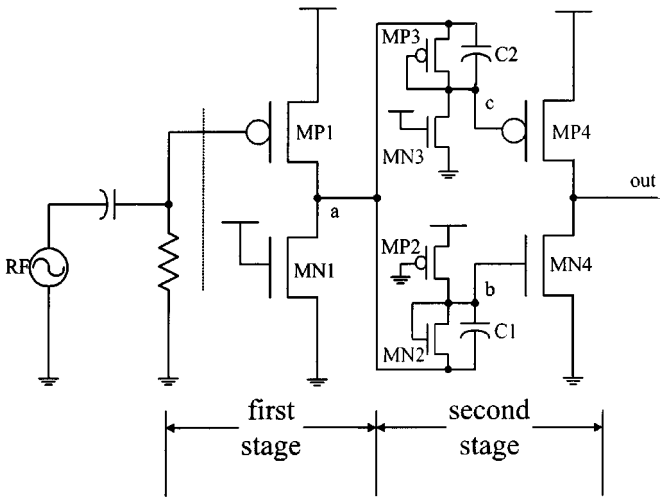


Fig. 7. Proposed low-voltage preamplifier.

B. Preamplifier

TSPC type dynamic digital circuits require an almost full swing clock signal. However, most of the VCOs used in high frequency communication systems can't provide so large an output signal, so a low-voltage preamplifier is used to amplify the smaller VCO output signal, as shown in Fig. 7.

The amplifier is composed of two stages. The first stage is a PMOS common-source amplifier with an NMOS transistor as its load. The dc voltage of the gate of MP1 is biased at ground through an OFF-chip 50-Ω resistor. Then the RF signal is coupled to the amplifier through an OFF-chip capacitance. The second stage is a low-voltage inverter stage. When node "a" is low (high), MP3 (MN2) is cutoff and node "c" ("b") is pulled down (up) to ground (V_{DD}) through MN3 (MP2). Thus, MP4 (MN4) turns ON to pull up (down) the output node to high (low). At this time, node "b" ("c") is biased at only a little above (below) V_{tn} ($V_{DD} - |V_{tp}|$) by MN2 and MP2 (MN3 and MP3). This allows MN4 (MP4) to drive only a small current and prevents it from being completely cutoff. It speeds the switching time because when node "a" starts to go high (low) again, the small boost capacitance, C1 (C2), can push node "b" ("c") from V_{tn} ("$V_{DD} - |V_{tp}|$") to V_{DD} (ground) quickly, instead of from ground (V_{DD}) to V_{DD} (ground) in a conventional inverter. Thus, MN4 (MP4) turns ON to pull down (up) the output node to low (high) more quickly than a conventional inverter.

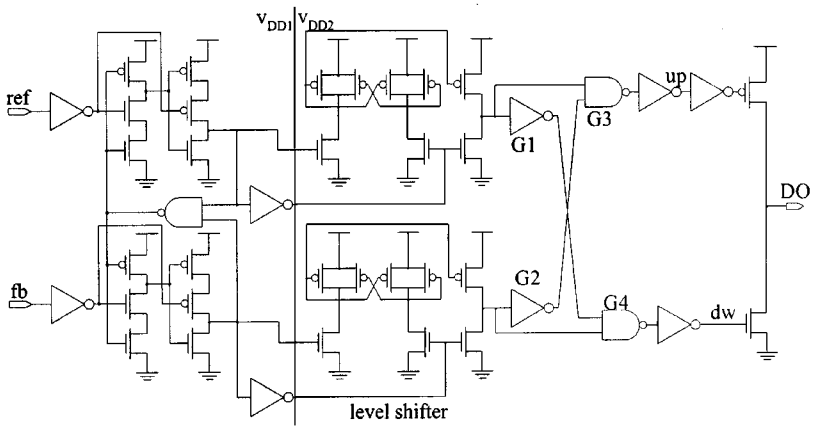


Fig. 8. Schematic of the PFD with level shifter.

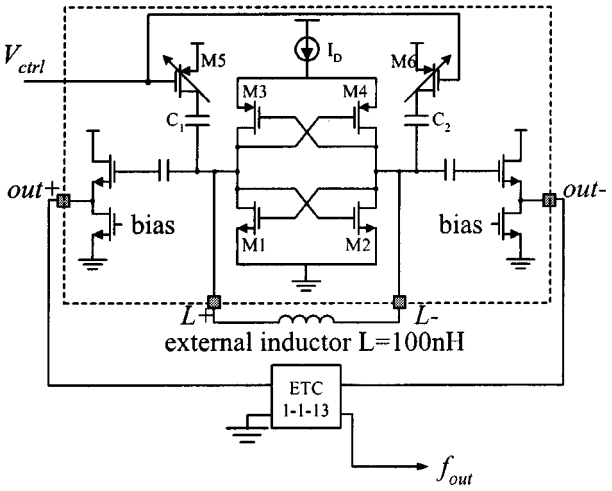


Fig. 9. Schematic of the *LC*-tank based VCO.

C. Frequency Dividers

The input frequency divider is a 16-b programmable dual-modulus frequency divider, which is used to divide the frequency of the VCO output signal. It consists of a preamplifier (Fig. 7), the proposed dynamic BGFB dual-modulus prescaler (Figs. 3 and 6), an 11-b programmable counter and a 5-b programmable counter [10]. The reference frequency divider is a 14-b programmable frequency divider that is used to divide the frequency of the crystal oscillator output signal. It consists of a preamplifier, a divide-by-4 prescaler and a 14-b programmable counter. Both dividers can operate at 1 V.

D. PFD and Lock Detector

Fig. 8 shows the PFD and charge pump used in the synthesizer. A voltage pump circuit consisting of a NMOS and a PMOS is used here. The PFD in Fig. 8 is similar to the one proposed in [11]. It not only uses fewer transistors, but also is faster than the conventional static PFD. However, the circuit in [11] produces short pulses at both output nodes (*up*, *dw*) every reference period even after the PLL is locked. At the instance, a dc path from power supply to ground is present and then dissipates extra power. What is more important is that the mismatch between the voltage pump NMOS and PMOS currents will flow into the filter and modulate the VCO. Therefore, extra gates (G1∼G4) are added in our work to remove the glitches. Since the PFD is designed to operate at 1 V, and the charge pump and VCO are designed to operate at 3 V, it is necessary to amplify the 1-V digital signal (*up* and *dw*) such that they can drive the voltage pump properly. Thus, two level shifters [12] are added in the PFD. It is worth it to note that the level shifters are inserted into the middle of the PFD, instead of in back of the PFD. This is because the level shifters will somewhat increase the pulse width, and make the charge transfer into the filter larger than it should be. Now, if the pulse width increases of the two level shifters are the same, the error can be removed by the logic gates (G1∼G4) in the end of the PFD. The lock detector is formed by OR gating the *up* and *dw* signals. After the PLL is locked, *up* and *dw* will be 0 and *LD* signal keeps on 0.

E. VCO

Most oscillators used in the communications are *LC*-tank based oscillators because of the high Q factor possible. An *LC*-tank based VCO is shown in Fig. 9. The back-connected active devices M1, M2 (M3, M4) produce a negative resistor to cancel the effect of the parasitic resistor. In order to achieve low power operation, the technique of current reuse [13] is used. M1 and M3 (M2 and M4) share the same bias current then produce an effective transconductance $g_{\text{eff}} = g_{M1} + g_{M3}$. Therefore, the bias current I_D can be halved to obtain the same transconductance and therefore the power dissipation can be reduced.

Since the oscillation frequency of such a VCO is proportional to $1/\sqrt{LC_{\text{eff}}}$, a large inductor is need in the low frequency applications, such as the ERMES pager systems. However, since no technique to implement large and high Q inductors in standard CMOS process is available yet, OFF-0chip inductors are used in our work. The oscillation frequency is tuned by the varactor consisting of M5 and C_1 (M6 and C_2). The effective capacitance C_{eff} of the varactor is decided by C_1 (C_2) and the parasitic capacitors C_{gd}, C_{gs}, C_{ds} of M5 (M6). Thus, with different V_{ctrl}, the parasitic capacitor of M5 (M6) and then C_{eff} are changed. The oscillation frequency of the VCO is tuned through this mechanism.

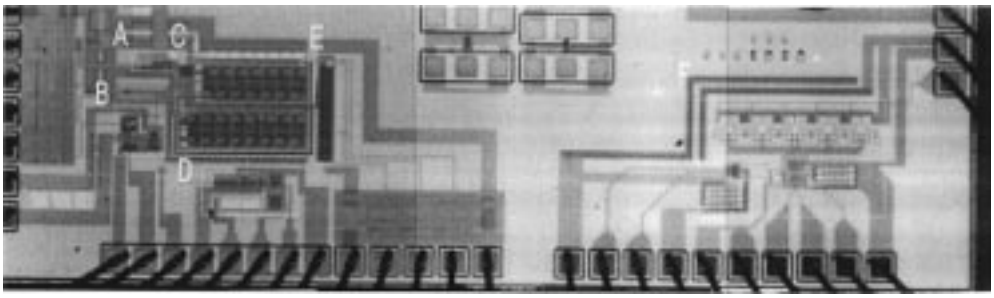


Fig. 10. Microphotograph of the frequency synthesizer.

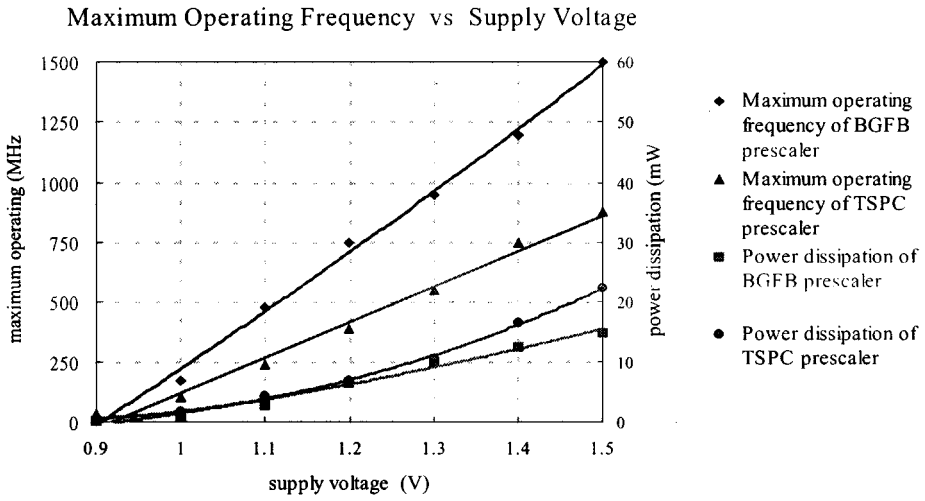


Fig. 11. Measured maximum operating frequency and power dissipation at different supply voltage of the prescalers.

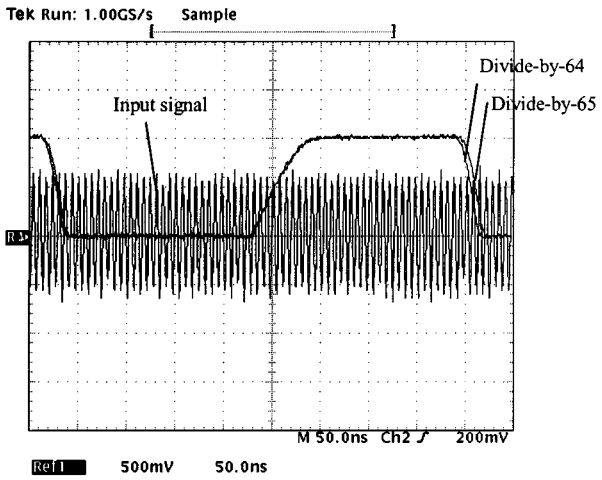


Fig. 12. Measured input and output waveforms of the prescaler.

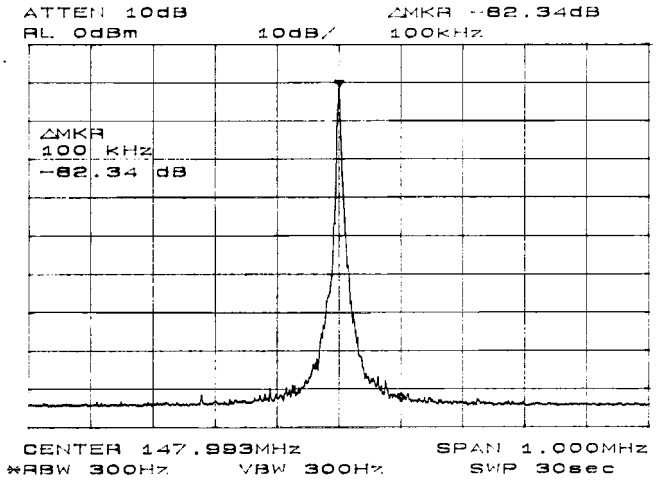


Fig. 13. Measured output frequency spectrum of the synthesizer.

Two source followers buffer the differential output signals. The OFF-chip transformer, ETC1-1-13 [14], is used to transfer the differential signals into a single- ended signal.

IV. Measurement Results

The chip has been fabricated with a 0.35-μm standard CMOS process. Fig. 10 shows the microphotograph of the whole frequency synthesizer. The active area of the VCO, the proposed prescaler and the other components of the synthesizer are 800 μm $\times$ 500 μm, 230 μm $\times$ 70 μm, and 1000 μm $\times$ 750 μm, respectively.

The proposed prescaler has been measured at supply voltage from 0.9 to 1.5 V. Fig. 11 shows the measured maximum operating frequency and power dissipation at different supply voltages. When the supply voltage is 1.5 V, the prescaler can operate at a clock rate of about 1.5 GHz. The maximum operating frequency of 170 MHz and the power dissipation of 0.9 mW (90% of the power is dissipated in the preamplifier, and 10% of it is dissipated in the prescaler) have been measured at 1-V supply voltage. Fig. 12 shows the 170-MHz input waveform and the

TABLE II
ERMES PAGER FREQUENCY SYNTHESIZER

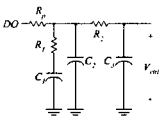
VCO gain	K_{vco}	2.329 MHz/V
Open loop gain bandwidth	K	1 kHz
Zero frequency	ω_z	0.25 kHz
First pole frequency	ω_{p1}	4 kHz
Second pole frequency	ω_{p2}	8.3 kHz
Passive elements: 	R_p	10 kΩ
	R_1	340 kΩ
	C_1	1.8 nF
	C_2	0.12 nF
	R_2	680 kΩ
	C_3	28 pF
Frequency range		148 ~ 148.425 MHz
Channel spacing		25 kHz
Channel number		16
Phase noise @ 148 MHz, 100-kHz offset		-106 dBc/Hz
Power dissipation @ 148 MHz		10.5 mW
Active area		800μmX500μm (VCO) 1000μmX750μm (others)

TABLE III
COMPARISON BETWEEN NPCS CHIP WITH THIS WORK

	NPC's chip [3]	This work
Process	Molybdenum-gate CMOS	0.35um 2P3M process
VCO	No	On-chip VCO with external inductor
Max. operating frequency of the prescaler	100MHz @ 1V	170MHz @ 1V
Input sensitivity of the prescaler	0.5Vpp	<-10dBm (0.2Vpp @ 50ohm)
Power consumption of the PLL	0.85mA @ 95MHz input	1.5mW @ 150MHz, 1V (digital) 9mW @ 150MHz, 3V (VCO)

output waveforms in the two different modes. A divide-by-64 prescaler consisting of six cascaded TSPC TFF's [1] is also implemented for comparison, and the measured results are also shown in Fig. 11. The maximum operating frequency and power dissipation of the TSPC prescaler are 100 MHz and 1.8 mW at 1V, respectively, (including preamplifier). It shows that the proposed prescaler can work at higher speed with less power dissipation than a TSPC one.

The VCO is measured at a supply voltage of 3 V. Fig. 13 shows the frequency spectrum of the VCO output signal locked at the frequency of 148 MHz. Reference frequency is generated by a 4-MHz crystal oscillator. Reference frequency divide-ratio and VCO frequency divide-ratio are 160 and 5920, respectively. Third order loop filter is utilized [15]. The measured phase noise is − 106 dBc/Hz at 100-kHz distance from the carrier. The measured VCO power consumption excluding the output buffers in this condition is 9 mW, and the total frequency synthesizer dissipates 10.5 mW. Table II gives a summary of the final ERMES pager frequency synthesizer. Finally, Table III compares this work with NPCs SM5160 [3], which is implemented with a molybdenum-gate process. The operating frequency and sensitivity of this work are better than NPCs chip. However, the power consumption of the digital parts is slightly larger than NPCs because the chip is operated at a higher frequency. Also, the preamplifier dissipates much power to achieve the sensitivity of − 10 dBm. If the chip is redesigned with VCO directly connected to the preamplifier in the chip. The required sensitivity can be released and the current consumed in the preamplifier can be reduced.

V. CONCLUSION

In this paper, a low-voltage CMOS frequency synthesizer has been implemented with the 0.35-μm standard CMOS process. A 1-V dual-modulus prescaler with the proposed dynamic BGFB method is used in the synthesizer. A maximum operating frequency of 170 MHz with the power consumption of 0.9 mW (including a preamplifier) has been measured at 1-V supply voltage. An *LC*-tank based VCO using an OFF-chip inductor is also implemented. When locked at an oscillation frequency of 148 MHz, measured phase noise of the VCO is −106 dBc/Hz at 100-kHz from the carrier. The power consumption of the frequency synthesizer excluding the output buffers of the VCO is 10.5 mW. It is shown that the low-voltage frequency synthesizer can be implemented by the proposed circuit techniques with a cheap, standard CMOS process without any mask or process modifications.

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