A 6-GHz All-Digital Fractional-N Frequency Synthesizer Using FIR-Embedded Noise Filtering Technique

I-Ting Lee, Hung-Yu Lu, and Shen-Iuan Liu, *Fellow, IEEE*

***Abstract*—A 6-GHz all-digital fractional-N frequency synthesizer using an FIR-embedded noise filtering technique is presented. This noise filtering technique is realized in the digital domain without multiple matched analog components. This fractional-N frequency synthesizer is fabricated in a 90-nm CMOS process, and it occupies 0.18 mm^2. Its power is 28.8 mW with a supply of 1.2 V. The measured out-of-band phase noise at an offset of half the reference frequency is improved by more than 13 dB around 6 GHz considering cancellation variations for different output frequencies.**

***Index Terms*—All-digital, delta–sigma modulator (DSM), digitally controlled oscillator (DCO), frequency synthesizer, quantization noise, time-to-digital converter (TDC).**

I. Introduction

A FRACTIONAL-N frequency synthesizer is realized to achieve a fine frequency resolution by using a delta–sigma modulator (DSM). It is popular for various applications, such as clock generation and frequency synthesis. However, the quantization noise of a DSM is shaped to a high-frequency band. It becomes one of the factors that may limit the bandwidth of a fractional-N frequency synthesizer. Thus, a tradeoff exists between bandwidth and phase noise of a fractional-N frequency synthesizer by using a DSM.

To deal with the above bandwidth tradeoff due to a DSM, several techniques have been proposed. For an analog fractional-N frequency synthesizer, a digital-to-analog converter (DAC) is adopted to compensate the quantization noise caused by a DSM [1], [2]. However, several nonideal factors limit this method, such as the DAC resolution and the gain matching between a DAC and a charge pump (CP). Moreover, to reduce the gain mismatching between a DAC and a CP, a calibration method is also needed [1], [2]. In [3], an all-digital quantization noise cancellation is adopted without the above problems. To reduce the quantization noise, several analog noise filtering techniques are also adopted in [4]–[6]. In [4], a hybrid FIR-embedded filtering technique is presented. Since multiple phase-frequency detectors (PFDs), CPs, and dual-modulus dividers are needed [4], it consumes the chip area and power. In [5], a multiphase voltage-controlled oscillator, a phase interpolator, and a phase blender are used to realize an FIR-embedded filtering technique. It may be limited by the matching accuracy among the analog circuits. In [6], an additional phase-locked loop is added to realize a phase-domain filter. It also needs the large chip area and power.

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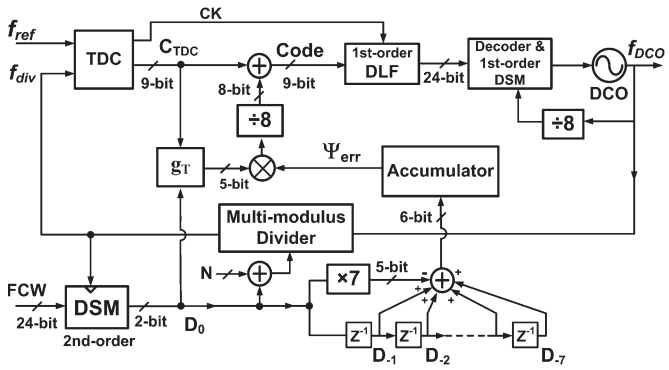


Fig. 1. Proposed all-digital frequency synthesizer.

In this brief, an all-digital FIR-embedded noise filtering technique is presented for a frequency synthesizer. No extra analog circuits are added. It is aimed to reduce the out-of-band phase noise caused by a DSM. This brief is organized as follows: Section II describes the proposed all-digital FIR-embedded noise filtering technique. Section III gives the circuit description. Section IV presents the measurement results. The conclusions are given in Section V.

II. Digital FIR-Embedded Noise Filtering Method

Fig. 1 shows an all-digital fractional-N frequency synthesizer using the FIR-embedded noise filtering technique. It consists of a time-to-digital converter (TDC), a first-order digital loop filter (DLF), a digitally controlled oscillator (DCO), a multimodulus divider (MMD), and a second-order multistage noise-shaping (MASH) 1–1 DSM. The integer part of the MMD is equal to N, which is from 128 to 255. The quantization error Q_{-i} of this DSM at the previous ith state $(i = 0 \sim 7)$ is defined as

$$Q_{-i}(t) = D_{-i}(t) - \text{FCW} \tag{1}$$

where D_{-i} is the DSM's output at the previous ith state, D_0 is the DSM's output at the present state, and the frequency control word (FCW) is the input of the DSM. The difference of quantization errors Q_{-i} and Q_0 is expressed as

$$\Delta Q_{-i}(t) = Q_{-i}(t) - Q_0(t) = D_{-i}(t) - D_0(t). \tag{2}$$

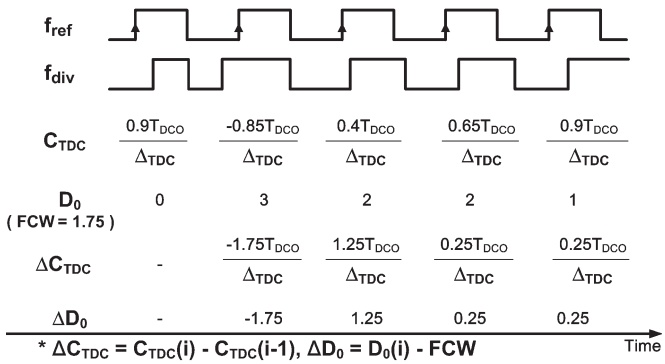


Fig. 2. Simulated transient outputs of a TDC and a second-order DSM in a frequency synthesizer.

Then, these quantization error differences are accumulated by a 6-bit accumulator, and they are given as

$$\Psi_{\rm err}(nT_R) = \Psi_{\rm err}(nT_R - T_R) + \sum_{i=1}^{7} \Delta Q_{-i}(nT_R) \qquad (3)$$

where T_R is the period of the reference clock, and n is an index. To convert parameter $\Psi_{\rm err}$ into a code, a gain factor of g_T $(= T_{\rm DCO}/\Delta_{\rm TDC})$ is required, where $T_{\rm DCO}$ and $\Delta_{\rm TDC}$ represent the clock period of the DCO and the TDC's resolution, respectively. A behavioral simulation of a frequency synthesizer is executed under $\Delta_{\rm TDC} = 8$ ps, a loop bandwidth of 800 kHz, a DCO with the phase noise of -100 dBc/Hz at an offset frequency of 1 MHz, and the frequency $f_{\rm ref}$ of the reference clock equal to 46.875 MHz. The output frequency is equal to 6.082 GHz ($T_{\rm DCO} = 164.42$ ps), and the corresponding divider ratio is 129.75. Fig. 2 shows the simulated transient response for the output $C_{\rm TDC}$ of the TDC and that of a second-order DSM in a frequency synthesizer. According to Fig. 2, the ratio of the difference of the two sequent TDC outputs and $D_0 - {\rm FCW}$ can be used to calculate the gain factor g_T. Considering the finite word-length effect, the gain factor g_T is realized by the following equation as

$$g_T = \frac{\sum_{i=0}^{M} \frac{|C_{\rm TDC}(i) - C_{\rm TDC}(i-1)|}{|D_0(i) - {\rm FCW}|}}{M+1} \qquad (4)$$

where M is an iteration number. However, (4) requires massive digital circuits to realize the division operations. Here, a simplified method is adopted by using the following equality:

$$\frac{x_0}{y_0} = \frac{x_1}{y_1} = \cdots \frac{x_M}{y_M} = \frac{x_0 + x_1 + \cdots + x_M}{y_0 + y_1 + \cdots + y_M}. \qquad (5)$$

By using (5), the gain factor is approximated as

$$g_T \cong \frac{\sum_{i=0}^{M} |C_{\rm TDC}(i) - C_{\rm TDC}(i-1)|}{\sum_{i=0}^{M} |D_0(i) - {\rm FCW}_{\rm est}|} \qquad (6)$$

where the estimated FCW, i.e., ${\rm FCW}_{\rm est}$, is expressed as

$${\rm FCW}_{\rm est} = \frac{\sum_{i=0}^{K} D_{-i}(t)}{K+1} \qquad (7)$$

where K is an integer, and $K \gg M$. Fig. 3 shows a block diagram to calculate the gain factor g_T, where the complicated

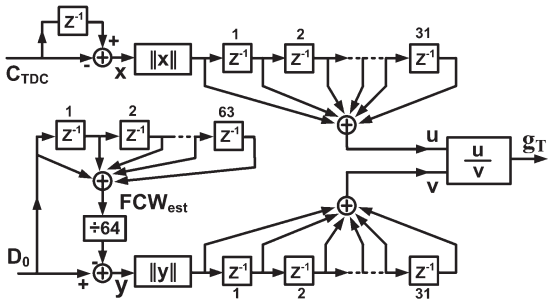


Fig. 3. Block diagram to calculate the gain factor g_T.

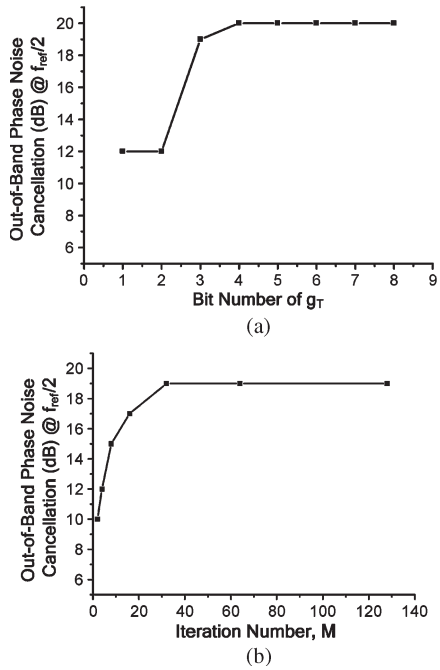


Fig. 4. Behavior simulations for out-of-band phase noise cancellation versus the (a) number of bits of the gain factor g_T and (b) iteration number M.

division operations are significantly reduced. Because of a finite word length in the digital calculations, one may want to know the required bits of this gain factor and the iteration number M in (6). A behavioral simulation is executed with and without the proposed method. The simulation parameters are almost the same with those in Fig. 2, except that the output frequency is equal to 6.081 GHz ($T_{\rm DCO} = 164.45$ ps) and the corresponding divider ratio is 129.728. Fig. 4(a) shows the simulation results for the out-of-band phase noise cancellation at the offset frequency of $f_{\rm ref}/2$ versus the number of bits of g_T, where the iteration number M is large enough. Fig. 4(a) indicates that the number of bits of g_T should be larger than 4 in order to suppress the out-of-band phase noise of 20 dB at $f_{\rm ref}/2$. Fig. 4(b) shows the out-of-band phase noise cancellation at the offset frequency of $f_{\rm ref}/2$ versus the iteration number M when the number of bits of g_T is 5. The required iteration M must be larger than 31 to suppress the out-of-band phase noise of 19 dB at $f_{\rm ref}/2$. In this brief, the number of bits of g_T is 5, the iteration number M is 31, and K is 63. By using (6), there is a loss of 1 dB for the out-of-band phase noise. Finally, the input code for the DLF is calculated as

$${\rm Code} = C_{\rm TDC} + \frac{g_T \cdot \Psi_{\rm err}}{8}. \qquad (8)$$

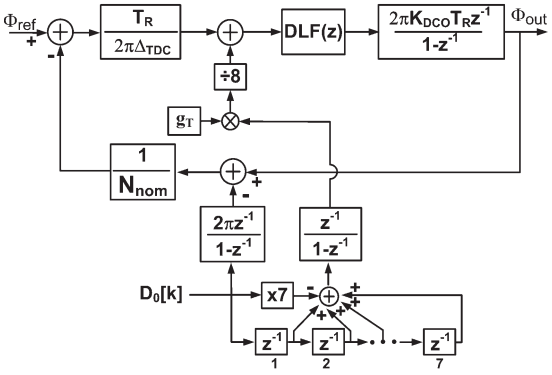


Fig. 5. z-Domain model of the proposed frequency synthesizer.

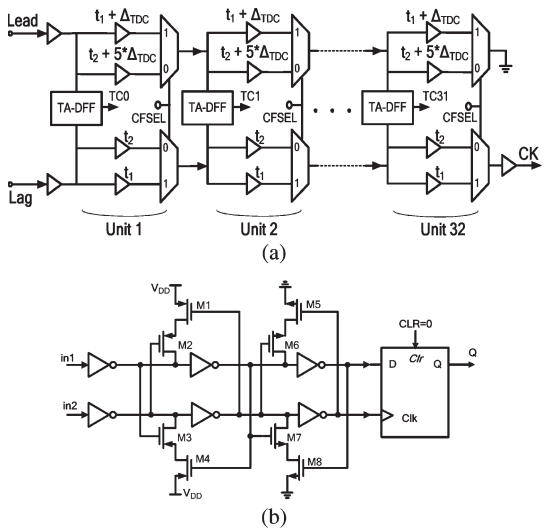


Fig. 6. (a) Vernier delay chain. (b) TA-DFF.

The z-domain model [4], [7] of the proposed all-digital frequency synthesizer is shown in Fig. 5, where $g_T = T_{\rm DCO}/\Delta_{\rm TDC} = T_R/\Delta_{\rm TDC}N_{\rm nom}$, and $N_{\rm nom}$ is the nominal division ratio. The output phase noise due to the quantization noise of the second-order DSM is expressed as

$$\Phi_{\rm out} = \frac{H(z)}{1+H(z)} \cdot D_0[k] \cdot \frac{2\pi z^{-1}}{1-z^{-1}} \cdot \frac{1}{8} \times (1+z^{-1}+z^{-2}+z^{-3}+z^{-4}+z^{-5}+z^{-6}+z^{-7}) \quad (9)$$

where $H(z) = ({\rm DLF}(z)K_{\rm DCO}T_R^2/N_{\rm nom}\Delta_{\rm TDC})(z^{-1}/(1-z^{-1}))$, and ${\rm DLF}(z)$ is the transfer function of the DLF. Thus, the output phase noise is improved since the quantization noise of the second-order DSM is multiplied with the transfer function of an FIR filter.

III. Circuit Description

A. TDC

Fig. 6(a) shows a Vernier delay chain [8], where 32 units are adopted. Every unit is composed of four delay elements cells, two multiplexers, and two time amplifiers with D flip-flops (TA-DFFs). When the phase error between two pulses, i.e., Lead and Lag, is larger than $31 * (t_1 + \Delta_{\rm TDC})$, the coarse–fine selection signal (CFSEL) selects the coarse delay lines by multiplexers. Then, the timing resolution of this TDC is increased to $5\Delta_{\rm TDC}$. When the phase error between Lead and Lag is less than $31 * (t_1 + \Delta_{\rm TDC})$, the fine delay lines are selected, and the timing resolution of this TDC is equal to $\Delta_{\rm TDC}$. Since $\Delta_{\rm TDC}$ is small, in order not to violate the setup and hold times of a conventional DFF, a time amplifier [9] is added, as shown in Fig. 6(b). Although the total output digits for coarse and fine delay lines are 12, the scaling factor of 5 exists between these two delay lines. It results in the equivalent bits of this TDC being 9 instead of 12 by using a decoder. The areas of a TA-DFF and a DFF in our 90-nm process are 250 and 160 μm^2, respectively. By the proposed Vernier delay chain, 32 DFFs for coarse delay lines are saved. The output signal CK of this Vernier delay chain is used to load the digital codes into the DLF.

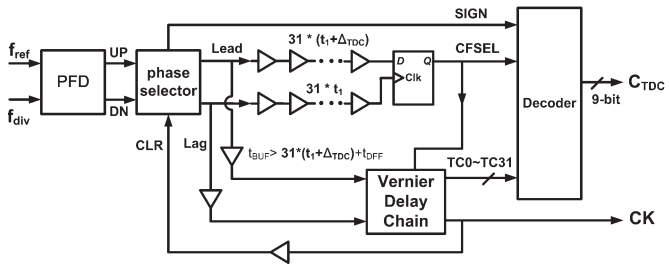


Fig. 7. Nine-bit coarse/fine Vernier TDC.

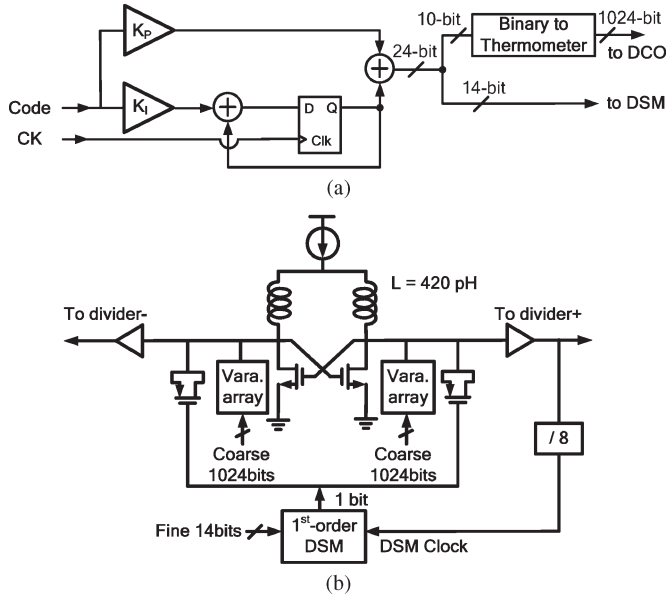


Fig. 8. (a) First-order DLF. (b) DCO.

Fig. 7 shows the 9-bit TDC, which is composed of a PFD, a phase selector [10], a Vernier delay chain, a decoder, and delay lines. Two input clocks trigger a PFD to generate two pulses UP and DN. The phase selector decides which pulse leading or lagging and the sign. It saves a half-delay line in the Vernier delay chain. In this brief, the fine timing resolution is $\Delta_{\rm TDC} = 8$ ps, the fine delay lines cover the range of ± 256 ps, whereas the coarse ones cover the range of ± 1.28 ns.

B. DLF, DCO, and MMD

Fig. 8(a) shows the first-order DLF with 24-bit outputs, where the proportional and integral gains are K_p and K_I. For better linearity, a binary-to-thermometer decoder converts the first 10 bits of the DLF into 1024 thermometer bits to control

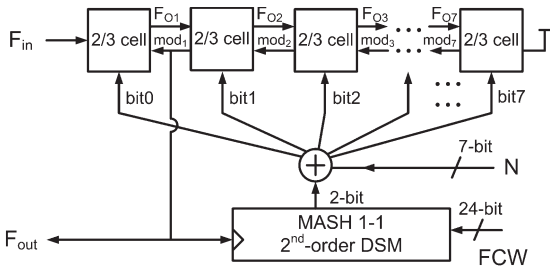


Fig. 9. MMD.

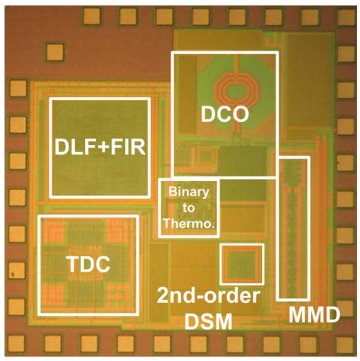


Fig. 10. Die photo.

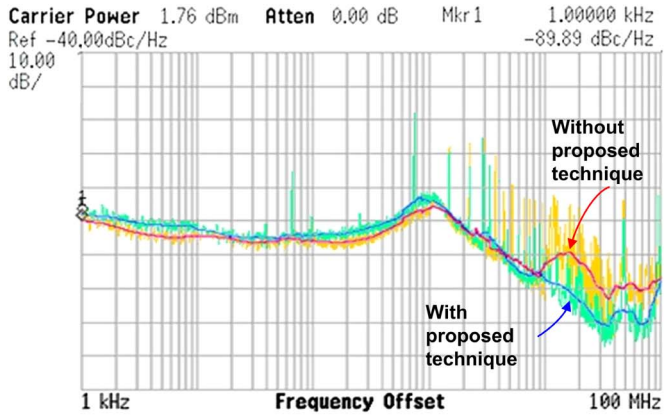
the frequency of the DCO. The DCO is shown in Fig. 8(b). It is composed of an LC-tank oscillator, the coarse and fine pMOS varactor arrays, a first-order DSM, and output buffers. The 1024 thermometer bits control the coarse pMOS varactor arrays, which achieve a tuning gain of 1 MHz/code. The fine 14 bits of the DLF are applied to a first-order DSM to achieve a fine frequency resolution of 245 Hz/code. A first-order DSM is realized by an accumulator, and the output of the DCO is divided by eight to serve as the clock of this DSM. This DCO covers from 5.4 to 6.5 GHz, and its simulated phase noise is -100 dBc/Hz at 1-MHz offset. The power consumption is 9.6 mW with a supply of 1.2 V.

The MMD [11] is realized by a series of divide-by-2/3 dividers, as shown in Fig. 9. The integer part of the division ratio of this MMD is N, which is from 128 to 255. The fractional part of the divider ratio is realized by a 24-bit second-order MASH 1–1 DSM. Note that a second-order MASH 1–1 DSM has a better noise-shaping performance compared with a first-order one. In addition, the gain factor g_T is estimated by using the outputs of a TDC and a second-order DSM in a frequency synthesizer.

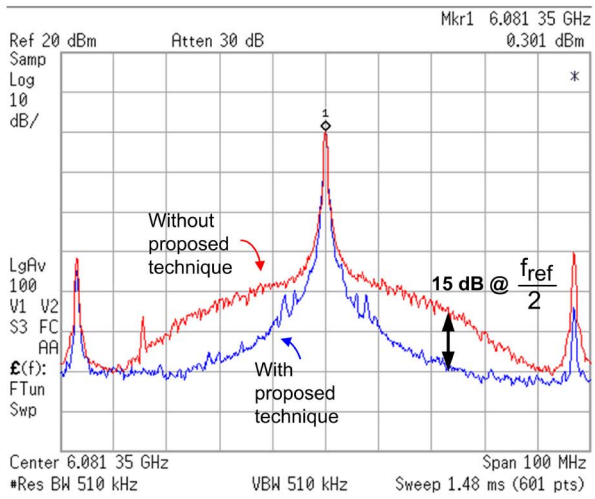
IV. Experimental Results

This 6-GHz fractional-N synthesizer using the proposed all-digital FIR-embedded noise filtering technique is fabricated in a 90-nm CMOS process. The die photo is shown in Fig. 10. The active core area is 0.18 mm^2. The total power consumption is 28.8 mW for a supply of 1.2 V.

When this frequency synthesizer works at 6.08135 GHz and the division ratio of 129.735, Fig. 11(a) shows the averaged in-band phase noise of -95 dBc/Hz at the offset frequency of 50 kHz with the proposed method. Fig. 11(b) shows the measured output spectra at 6.08135 GHz and the division ratio of



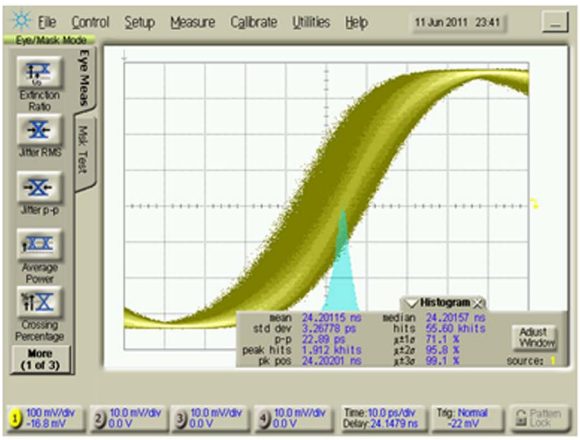
(a)



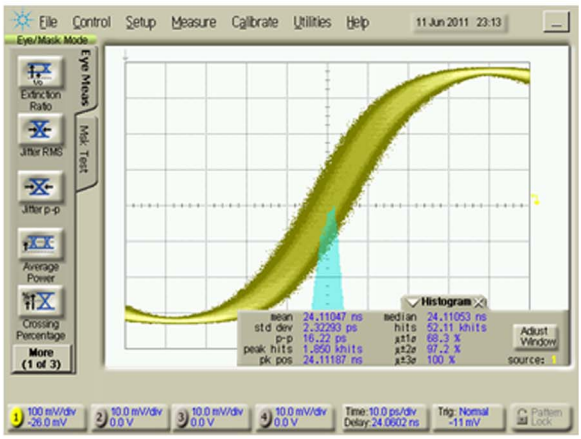
(b)

Fig. 11. (a) Measured phase noise plots. (b) Spectra with and without the proposed technique.

129.735 with and without the proposed method, respectively. With the proposed method, the out-of-band phase noise at the offset frequency of $f_{\rm ref}/2$ is suppressed by 15 dB. In Fig. 11(b), the reference spur is slightly improved by this FIR filter. Fig. 12(a) and (b) shows the measured jitter histograms without and with the proposed technique, respectively. In Fig. 12(a), the RMS jitter is 3.27 ps, and the peak-to-peak jitter is 22.89 ps. In Fig. 12(b), the RMS jitter is 2.32 ps, and the peak-to-peak jitter is 16.22 ps. Fig. 13 shows the summary for the measurement and simulation results of the out-of-band phase noises at the offset frequency of $f_{\rm ref}/2$. The bit number of g_T and the iteration number M are selected according to the behavioral simulation results in Fig. 4(a) and (b), respectively. The behavioral simulation is executed under $\Delta_{\rm TDC} = 8$ ps and without the DCO's phase noise. However, the degradation of the DCO's phase noise and the resolution of a TDC may cause the deviation between the measurement and simulation results. The measured reference spur is -43 dBc, and the worst-case in-band fractional spur is -27 dBc. The performance summary of this work is given in Table I. Compared with other works, the reference spur of this work is worse. The reference spur suffers from the digital noises coupling to the DCO and the DCO's gain. To suppress the reference spur, these digital coupling noises and the gain of this DCO should be reduced.



(a)



(b)

Fig. 12. Measured jitter histograms (a) without and (b) with the proposed technique.

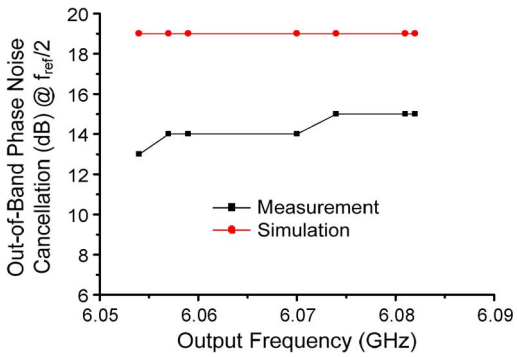


Fig. 13. Measurement and simulation results for out-of-band phase noise cancellation at $f_{\rm ref}/2$.

V. Conclusion

A 6-GHz all-digital fractional-N frequency synthesizer using the proposed FIR-embedded noise filtering technique is realized in a 90-nm CMOS process. By using this embedded FIR filtering technique, the out-of-band phase noise due to DSM quantization noise is suppressed. Compared with the analog FIR technique [4], the matched analog components, such as PFDs, CPs, and dual-modulus prescalers, are not required in this work. Due to the nature of digital circuits, the gain mismatching between the main and compensation paths are relaxed.

TABLE I
Performance Summary and Comparison

	Our	[3]	[4]	[5]	[6]	[13]
Output Freq. (GHz)	5.4~6.5	3.67	1	1	5	3.6
In-band Phase Noise	-95 dBc/Hz	-108 dBc/Hz	-85 dBc/Hz	-106 dBc/Hz	-86 dBc/Hz	-104 dBc/Hz
Method	FIR	Digital	FIR	FIR+PI	NF	PI
Out-of-band Phase Noise Cancellation	15dB @ 23.4MHz	15dB @ 10MHz	15dB @ 6MHz	12dB @ 6MHz	13dB @ 10MHz	N.A.
Reference Spur (dBc)	-43	-65	N.A.	-66	-61	-65
Phase Noise (dB)	-108@ 10MHz	-120@ 1MHz	N.A.	-105@ 3MHz	-102@ 1MHz	-105@ 3MHz
Power (mW)	28.8	46.7	6.1	16.8	30	80
Area (mm2)	0.18	0.95	0.5	0.31	0. 56	0.4
CMOS (nm)	90	130	180	130	90	65
VCO	LC	LC	Ring	Ring	LC	LC

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