Voltage-mode MOSFET-C filters using operational transresistance amplifiers (OTRAs) with reduced parasitic capacitance effect

J.-J.Chen, H.-W.Tsao and S.-I.Liu

Abstract: The MOSFET-C integrator with reduced parasitic capacitance effect using operational transresistance amplifiers is proposed and experimental results are demonstrated. The bandwidths of these circuits are independent of their gains. The required capacitors are smaller than those described in previous work. Two new configurations of universal biquad filters based on these circuits are presented. A second-order bandpass filter, constructed using universal biquad filters, and a third-order Chebyshev lowpass filter, with 1dB passband ripple, are breadboarded. Measured results are presented.

1 Introduction

In certain mixed analogue–digital applications, it has been demonstrated that continuous-time filters offer several advantages over the discrete-time of integrated filters, e.g. switched-capacitor filters and digital filters [1]. Continuous-time filter techniques have therefore received considerable attention in MOS VLSI technology, because these filters can be stabilised against fabrication tolerances and temperature variations [1]. Unfortunately, the bandwidth of conventional active building blocks is dependent on the closed-loop voltage gain, and the effect of parasitic capacitance will also degrade the performance of whole analogue signal processing circuits.

In this paper, the MOSFET-C integrator constructed with operational transresistance amplifiers (OTRAs) is proposed. Using current feedback techniques, OTRAs have a bandwidth almost independent of the closed-loop voltage gain. In addition, because the impedances at the input and output terminals of an OTRA are low, most parasitic capacitances will have little effect on these circuits. The effect of the other parasitic capacitances can be compensated without adding any extra elements. To verify the basic function of the proposed circuits, we have employed discrete components to breadboard these circuits. We present the experimental results, simulation results and analysis of total harmonic distortions.

Two configurations of universal biquad filters derived from these circuits are proposed. Experimental results of the MOSFET-C integrator are presented to demonstrate the constant bandwidth performance. A bandpass filter and a third-order lowpass filter, with 1dB passband ripple based on this integrator, are also tested. To investigate the effects of parasitic capacitances, the integrator with externally added capacitors to simulate 'parasitic capacitances' is described and tested. The total harmonic distortions of the integrator and differentiator are also analysed and tested.

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2 Circuit description

The characteristics of an OTRA (Fig. 1*a*) can be described by

$$\begin{bmatrix} V^+ \\ V^- \\ V_o \\ I_d \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ R_m & -R_m & 0 & 0 \\ 1 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_o \\ V_d \end{bmatrix} \quad (1)$$

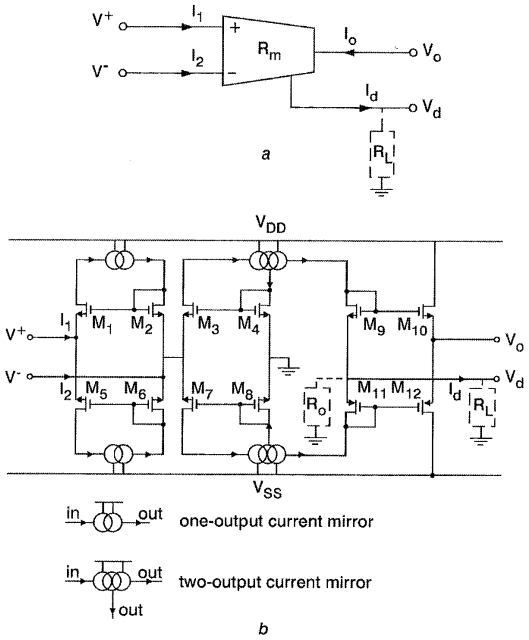

Fig. 1 *Symbol and actual circuit of an OTRA*
a Symbol
b Actual circuit

Obviously, both input terminals are virtually grounded. The output voltage is the difference of two input currents multiplied by transresistance R_m ($R_m = R_o//R_L$, where R_o is the total effective output impedance of the two-output current mirrors, and R_L is the external load impedance). Now we can construct this building block using the circuit shown in Fig. 1*b*. R_m usually has a large value, and can be considered as infinite in most applications.

For an NMOS transistor biased in the triode region, the channel current is given in terms of various basic device parameters as

$$i_D = F(v_D, V_G) - F(v_S - V_G) \tag{2}$$

with $F(v_X, V_G) = 2K(V_G - V_B - V_{FB} - \phi_B)\, v_X - K(v_X - V_B)^2 - 4/3K\gamma(v_X - V_B + \phi_B)^{3/2}$

$$K = \frac{W}{2L}\mu C_{ox},\ \gamma = \frac{\sqrt{2qN_A\varepsilon_S}}{C_{ox}},\ v_X = v_D \text{ or } v_S$$

where i_D is the drain current in the triode region; W and L are the channel width and length, respectively; μ is the effective channel mobility; V_{FB} is the flat band voltage; N_A is the substrate doping concentration; C_{OX} is the gate oxide capacitance per unit area; ϕ_B is the approximate surface potential at strong inversion; and V_G and V_B are the gate and substrate voltage, respectively.

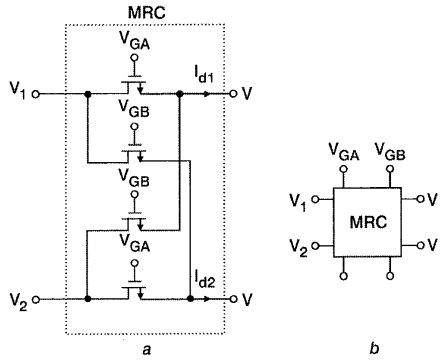

Fig. 2 *MOSFET resistive circuit and symbol of MRC*
a MOSFET resistive circuit
b Symbol of MRC

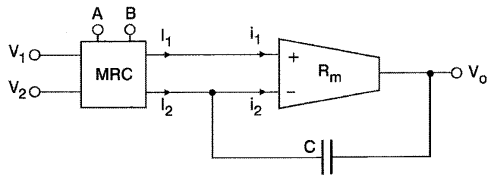

Fig. 3 *MOSFET-C integrator based on single OTRA*
A = V_{GA}; B = V_{GB}

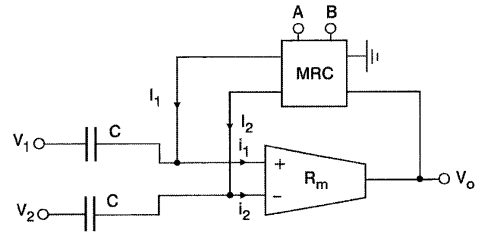

Fig. 4 *MOSFET-C differentiator based on single OTRA*
A = V_{GA}; B = V_{GB}

The circuit illustrated in Fig. 2*a* is a MOSFET resistor circuit (MRC), whose symbol is shown as Fig. 2*b*. If all NMOS transistors of the circuit shown in Fig. 2*a* operate in the triode region, straightforward circuit analysis will yield [2]

$$\begin{aligned} i_{d1} - i_{d2} &= F(v_1, V_{GA}) - F(v_1, V_{GB}) \\ &\quad - F(v_2, V_{GA}) + F(v_2, V_{GB}) \\ &= 2K(V_{GA} - V_{GB})(v_1 - v_2) \end{aligned} \tag{3}$$

An MRC and OTRA can be used to realise integrators and differentiators. Figs. 3 and 4 show the circuit diagrams of the MOSFET-C integrator and differentiator. For the integrator shown in Fig. 3, the relationship between v_o, v_1 and v_2 is

$$2K(V_{GA}-V_{GB})(v_1-v_2) = I_1 - I_2 = i_1 - \left(i_2 - C\frac{dv_o}{d\tau}\right) \tag{4}$$

Since $i_1 - i_2 = v_o/R_m$, the output voltage of this integrator can be expressed as

$$\begin{aligned} v_o &= \frac{1}{C}\int \left(2K(V_{GA} - V_{GB})(v_1 - v_2) \right. \\ &\quad \left. - \frac{1}{R_m}(i_1 - i_2)\right) d\tau \end{aligned} \tag{5a}$$

$$\cong \frac{1}{RC}\int (v_1 - v_2)\, d\tau \tag{5b}$$

$$R = \frac{1}{2K(V_{GA} - V_{GB})}$$

If we take Laplace transforms of eqn. 4 and replace $i_1(s) - i_2(s)$ with $V_o(s)/Z_m(s)$, eqn. 6 can be obtained:

$$2K(V_{GA} - V_{GB})(V_1(s) - V_2(s)) = \frac{V_o(s)}{Z_m(s)} + sCV_o(s) \tag{6}$$

and the transfer function can be expressed as

$$\frac{V_o(s)}{V_1(s) - V_2(s)} = \frac{2K(V_{GA} - V_{GB})}{sC + \dfrac{1}{Z_m(s)}} \tag{7}$$

If $Z_m(s)$ takes the form of $N(s)/D(s)$, the transfer function of $V_o(s)$ can be rewritten as

$$\frac{V_o(s)}{V_1(s) - V_2(s)} = \frac{2K(V_{GA} - V_{GB})N(s)}{sCN(s) + D(s)} \tag{8}$$

If $Z_m(s)$ can be modelled with a single dominant pole p as

$$Z_m(s) = \frac{R_i}{1 + \dfrac{s}{p}} \tag{9}$$

The transfer function of $V_o(s)$ can be expressed as

$$\frac{V_o(s)}{V_1(s) - V_2(s)} = \frac{2K(V_{GA} - V_{GB})R(i)}{1 + \dfrac{s}{(R_iC + p^{-1})^{-1}}} \tag{10}$$

If the capacitance C does not change, the poles and zeros of this transfer function will always remain the same. Thus, the bandwidth of this circuit is nearly constant and independent of the closed-loop voltage gain. For the MOSFET transistors in the MRC to operate in the triode region, the dynamic range of input voltage must be restricted such that

$$\max(v_1 - v_2) \le \min\big((V_{GA} - V_B),\ (V_{GB} - V_T)\big) \tag{11}$$

Furthermore, the circuit shown in Fig. 4 is a differentiator. We have proposed this circuit previously [3]. The transfer function is

$$\frac{V_o(s)}{V_1(s) - V_2(s)} = \frac{sC}{2K(V_{GA} - V_{GB}) + \dfrac{1}{Z_m(s)}} \tag{12}$$

With $Z_m(s) = N(s)/D(s)$, eqn. 12 can be expressed as

$$\frac{V_o(s)}{V_1(s) - V_2(s)} = \frac{sCN(s)}{2K(V_{GA} - V_{GB})N(s) + D(s)} \tag{13}$$

If $Z_m(s)$ can be modelled with a single dominant pole p, as shown in eqn. 9,

$$\frac{V_o(s)}{V_1(s) - V_2(s)} = \frac{\dfrac{sCR(i)}{(1 + 2K(V_{GA} - V_{GB})R(i)}}{1 + \dfrac{s}{(1 + 2K(V_{GA} - V_{GB})R(i)p}} \tag{14}$$

If $(V_{GA} - V_{GB})$ does not change, the poles and zeros of this transfer function are always the same. Thus, the bandwidth of this circuit is also nearly a constant and independent of the closed-loop voltage gain. Since the MOSFET transistors must operate in the triode region, if $(v_1 - v_2)$ is a sine wave, the dynamic range of input voltage must be restricted in the following range:

$$\max(v_1 - v_2) \leq \frac{2K(V_{GA} - V_{GB})}{\omega C} \times \min\big((V_{GA} - V_T),\ (V_{GB} - V_T)\big) \tag{15}$$

where ω is the angular frequency of $(v_1 - v_2)$.

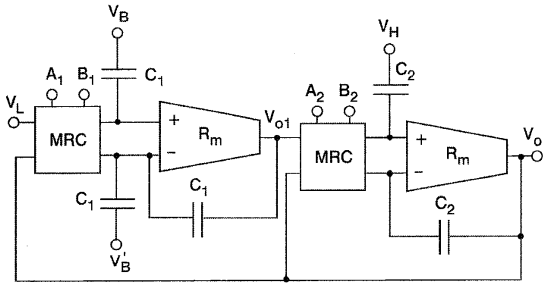

Fig. 5 *Universal biquad filter using MOSFET-C integrators shown in Fig. 3*
$A_1 = V_{GA1}$; $A_2 = V_{GA2}$; $A_3 = V_{GA3}$; $B_1 = V_{GB1}$; $B_2 = V_{GB2}$; $B_3 = V_{GB3}$

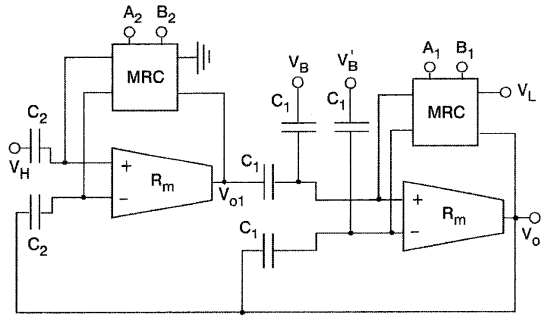

Fig. 6 *Universal biquad filter using MOSFET-C differentiators shown in Fig. 4*
$A_1 = V_{GA1}$; $A_2 = V_{GA2}$; $B_1 = V_{GB1}$; $B_2 = V_{GB2}$

We can then use the integrator and differentiator to realise two configurations of universal biquad filters, shown in Figs. 5 and 6. In Fig. 5, if $V_{GA2} = V_{GA1}$, $V_{GB2} = V_{GB1}$ and all the transistor sizes in the MRCs are equal, the output voltage $V_o(s)$ can be obtained by direct analysis. With infinite transresistances of the two amplifiers, the output voltage $V_o(s)$ is

$$V_o(s) = \frac{V_H(s)s^2C_1C_2R_1R_2 + (V_B(s) - V_{B'}(s))sC_1R_1 + V_L(s)}{s^2C_1C_2R_1R_2 + sC_1R_1 + 1} \tag{16}$$

where

$$R_1 = \frac{1}{2K(V_{GA1} - V_{GB1})} \text{ and } R_2 = \frac{1}{2K(V_{GA2} - V_{GB2})}$$

Let us take $V_H(s) = V_B(s) = V_{B'}(s) = 0$ (i.e., connecting nodes V_H, V_B and $V_{B'}$ to ground) and $V_L(s) = V_{in}(s)$ (connecting V_L to input signal V_{in}). A lowpass filter (LP) with unity gain can then be established at node V_0, with natural angular frequency ω_0 and quality factor Q given by the following equations:

$$\omega_o = \sqrt{\frac{1}{R_1R_2C_1C_2}} \tag{17}$$

$$Q = \sqrt{\frac{R_2C_2}{R_1C_1}} \tag{18}$$

The various passive sensitivities can be calculated as

$$S^{\omega_o}_{R_1} = S^{\omega_o}_{R_2} = S^{\omega_o}_{C_1} = S^{\omega_o}_{C_2} = -\frac{1}{2}$$
$$S^{Q}_{R_1} = S^{Q}_{C_1} = \frac{1}{2}$$
$$S^{Q}_{R_2} = S^{Q}_{C_2} = -\frac{1}{2} \tag{19}$$

Table 1 summarises other possible combinations, which also yield useful second-order filtering networks. Their natural angular frequency ω_0 and quality factor Q are the same as in eqns. 17 and 18, respectively.

For the circuit of Fig. 6, the output voltage $V_o(s)$ can also be expressed by eqn. 16. This network can synthesise various filtering functions as listed in Table 1.

Using these integrators and differentiators, we can also construct high-order ladder filters. The circuit of Fig. 7 is a third-order Chebyshev lowpass filter, which can be implemented using the integrator shown in Fig. 3. The experimental results are presented in Section 6.

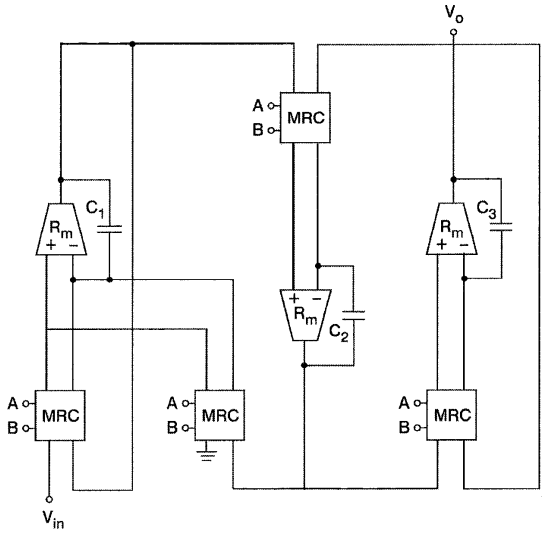

Fig. 7 *Third-order Chebyshev lowpass filter*
$A = V_{GA}$; $B = V_{GB}$

3 Stability analysis

The function $Z_m(s)$ which characterises the transresistance of an OTRA, can be modelled with a single dominant pole as

$$Z_m(s) = \frac{R_i}{1 + \frac{s}{p}} \tag{20}$$

Table 1: Second-order filters derived from Figs. 5 and 6

	V_H	V_B	$V_{B'}$	V_L	Transfer function V_0/V_{in}	Function
1	V_{in}	F	F	G	$s^2C_1C_2R_1R_2/(s^2C_1C_2R_1R_2 + sC_1R_1 + 1)$	HP
2	F	V_{in}	F	G	$sC_1R_1/(s^2C_1C_2R_1R_2 + sC_1R_1 + 1)$	BP
3	F	F	V_{in}	G	$-sC_1R_1/(s^2C_1C_2R_1R_2 + sC_1R_1 + 1)$	BP
4	F	F	F	V_{in}	$1/(s^2C_1C_2R_1R_2 + sC_1R_1 + 1)$	LP
5	V_{in}	F	F	V_{in}	$(s^2C_1C_2R_1R_2 + 1)/(s^2C_1C_2R_1R_2 + sC_1R_1 + 1)$	NF
6	V_{in}	F	V_{in}	V_{in}	$(s^2C_1C_2R_1R_2 - sC_1R_1 + 1)/(s^2C_1C_2R_1R_2 + sC_1R_1 + 1)$	AP

G: connected to ground; F: left floating; V_{in}: connected to input signal; HP: highpass; BP: bandpass; LP: lowpass; NF: notch; AP: allpass

where p is positive, and $(-p)$ is the dominant pole of the OTRA, R_i is the DC transresistance. The transfer function of the integrator in Fig. 3 can be rewritten as

$$\frac{V_o(s)}{V_1(s) - V_2(s)} = \frac{2K(V_{GA} - V_{GB})R_i}{1 + \frac{s}{p_i}} \tag{21}$$

where $p_i = (R_iC + p^{-1})^{-1}$.

For this integrator to be stable, p_i, must remain in the left half of the s-plane. As p_i is positive, it is not necessary to restrict the sign of $(V_{GA} - V_{GB})$ i.e. this integrator is always stable. We can also investigate the stability of the differentiator shown as Fig. 4 by straightforward analysis,

$$\frac{V_o(s)}{V_1(s) - V_2(s)} = \frac{sC}{2K(V_{GA} - V_{GB}) + 1/R_i} \frac{1}{1 + s/p_d} \tag{22}$$

where $p_d = p[2KR_i(V_{GA} - V_{GB}) + 1]$.

For this differentiator to be stable, the pole p_d must remain in the left half of the s-plane, i.e. the voltage difference $(V_{GA} - V_{GB})$ should satisfy the following condition:

$$(V_{GA} - V_{GB}) > -\frac{1}{2KR_i} \tag{23}$$

4 Effect of parasitic capacitances

To investigate the effects of parasitic capacitance on the integrator, we can redraw this integrator with parasitic capacitances shown explicitly as in Fig. 8. Owing to the vitually grounded inputs and the low-impedance output characteristics of an OTRA, capacitances C_{p15}, C_{p16} and C_{p17} have no effect. In addition, since V_{GA} and V_{GB} are DC sources, the effects of C_{p3}, C_{p4}, C_{p5}, C_{p6}, C_{p7}, C_{p8}, C_{p9}, and C_{p10}, also disappear. Then the voltage V_o can be written as

$$V_o(s) = \frac{2K(V_{GA} - V_{GB}) + s(C_{p11} - C_{p13})V_1(s) + s(C_{p12} - C_{p14})V_2(s)}{s(C + C_{p2} - C_{p1}) + 1/Z_m(s)} \tag{24}$$

The capacitances C_{p11}, C_{p12}, C_{p13}, and C_{p14}, are drain-to-source capacitances of NMOS transistors in the MRC. As the aspect ratios and drain-to-source voltages of NMOS transistors are identical, capacitances C_{p11}, and C_{p13}, will be approximately equal, and C_{p2}, will be nearly equal to C_{p14}. With $Z_m(s)$ approaching infinity, the transfer function is

$$\frac{V_o(s)}{V_1(s) - V_2(s)} = \frac{2K(V_{GA} - V_{GB})}{s(C + C_{p2} - C_{p1})} \tag{25}$$

The gain tolerance of this integrator, caused by the capacitances C_{p15}, and C_{p15}, can be compensated through adjusting the voltages V_{GA} and V_{GB} or the use of some precompensation technique without adding any extra components.

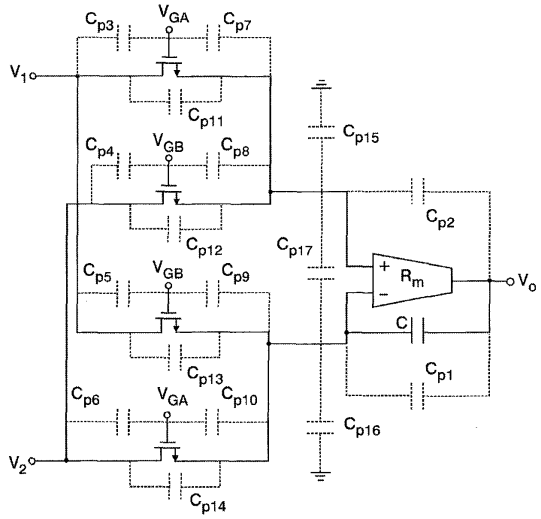

Fig. 8 *MOSFET-C integrator with added parasitic capacitance*

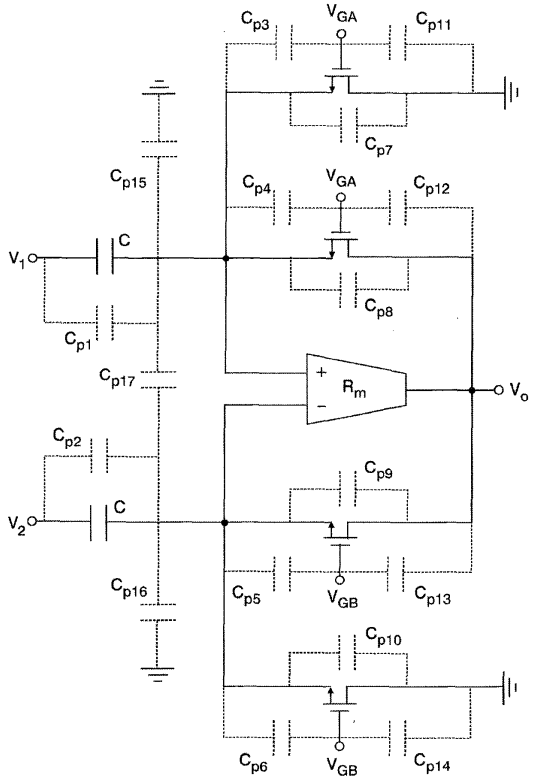

Fig. 9 *MOSFET-C differentiator with added parasitic capacitance*

The differentiator with parasitic capacitances is shown in Fig. 9. For similar reasons, the capacitances C_{p3}, C_{p4}, C_{p5}, C_{p6}, C_{p7}, C_{p8}, C_{p9}, C_{p10}, C_{p11}, C_{p12}, C_{p13}, C_{p14}, C_{p15}, C_{p16}, and C_{p17}, will have no effect, and the resultant output voltage V_o is

$$V_o(s) = \frac{s(C + C_{p1})V_1(s) - s(C + C_{p2})V_2(s)}{2K(V_{GA} - V_{GB})} \quad (26)$$

The gain tolerance depends on capacitances C_{p1}, and C_{p2}, which should be considered as a part of both capacitors C, it can also be corrected through the use of a pre-compensation technique without adding any additional components. If the pre-distortion technique is employed to make $C + C_{p1} = C + C_{p2} = C_T$, the transfer function can be rewritten as

$$\frac{V_o(s)}{V_1(s) - V_2(s)} = \frac{sC_T}{2K(V_{GA} - V_{GB})} \quad (27)$$

Thus the effect of parasitic capacitances of the differentiator has been nullified.

5 Harmonic distortion analysis

Using the level-3 MOSFET model of SPICE, the dependence of the mobility on V_{GA} and the threshold voltage on v_{DS} can be expressed as [4, 5]

$$\mu_s = \frac{\mu}{1 + \theta(V_G - V_{TH})} \quad (28)$$

$$V_{TH} = V_{FB} + 2\phi_p - \sigma v_{DS} + \gamma F_s\sqrt{2\phi_p - V_{BS}} + F_n(2\phi_p - V_{BS}) \quad (29)$$

For single-ended input ($v_1 = V_{pp}\cos\omega t$ and $v_2 = 0$), analysis results show that second-order harmonics will be present and the total harmonic distortions can be shown (see the Appendix) to be

$$THD \approx HD_2 = \frac{\frac{\theta}{2}\left(\frac{1+F_B}{2} - 2\sigma\right)V_{pp}}{1 + 2\theta\left(V_{FB} + 2\phi_p + \gamma F_s\sqrt{2\phi_p - V_{BS}} + F_n(2\phi_p - V_{BS}) - \frac{V_{GA} - V_{GB}}{2}\right)} \quad (30)$$

For fully differential input ($v_1 = -v_2 = 0.5V_{pp}\cos\omega t$), there will be almost no harmonic distortions in this integrator.

The analysis of the harmonic distortions of the differentiator can be carried out using the same method.

6 Experimental and simulation results

We use commercial IC CD4007UBE to construct an OTRA, as shown in Fig. 1*b*. To verify the constant bandwidth performance, the integrator shown in Fig. 3 is breadboarded. The measured results of this integrator with a negative gain ($V_{GA} < V_{GB}$) are shown in Figs. 10*a* and *b*. The voltage V_{GA} is equal to 5.4V, and the voltages V_{GB} for curves X7 and X8 are 7.6V and 6.4V, respectively. As indicated in these results, the poles and zeros of these curves are the same as the others. Thus, the bandwidths are nearly independent of the voltage gains.

External capacitors C_{p3}, C_{p7}, C_{p17} and C_{p15}, which are used to simulate parasitic capacitances and are equal to 10nF, are then individually connected in our integrator, as shown in Fig. 11, to demonstrate the immunity of parasitic capacitances. Curves X3, X4, X5, X6, and X7 (as shown in Figs. 12*a* and *b*) are the experimental results of the integrator shown in Fig. 11 including C_{p3}, C_{p3}, C_{p3} and C_{p15} (only once at a time) or no parasitic capacitor with V_{GA} = 5.4V and V_{GB} = 7.6V, respectively. All of the gains and phase results are nearly identical, and the parasitic-capacitance-immune performance is obvious.

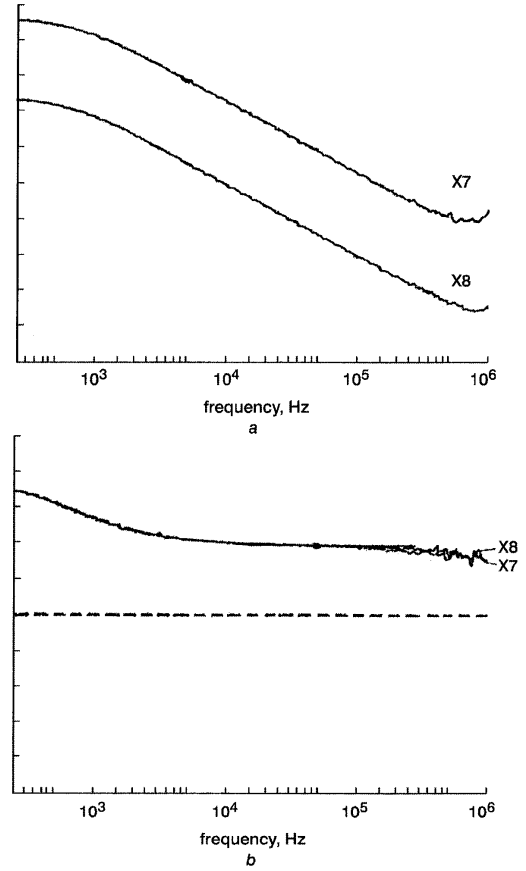

Fig. 10 *Experimental results for integrator shown in Fig. 3*
a Gain amplitude
Vertical scale: 10dB/div; X7: 18.776dB; X8: −4.460dB
b Phase amplitude
Vertical scale: 45°/div; X7: 89.663°; X8: 88.686°

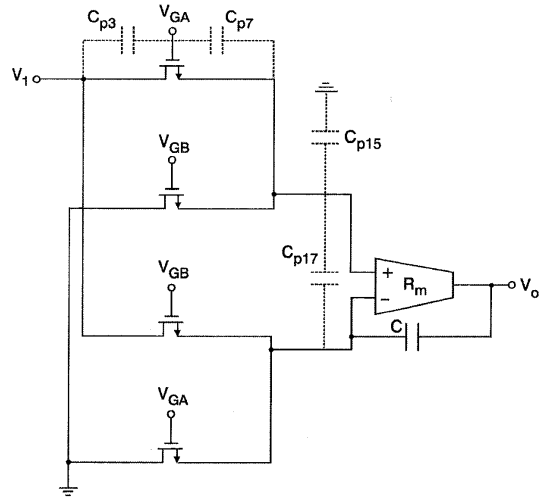

Fig. 11 *MOSFET-C integrator with added enlarged parasitic capacitors*

The second-order bandpass filter, derived from Fig. 5 and Table 1, is implemented. The measured gain amplitude and phase responses of the bandpass filter are presented in Fig. 13. In this filter, we have set $V_{GA1} = V_{GA2}$ = 7.6V,

$V_{GB1} = V_{GB2} = 5.4$V, and all capacitors are equal to 2nF. The third-order Chebyshev lowpass filter with 1dB passband ripple (as shown in Fig. 7) is breadboarded. The capacitors are selected as $C_1 = 2$nF, $C_2 = 1$nF and $C_3 = 2$nF, the measured results are shown in Fig. 14. To verify the theoretical results of harmonic distortions, the harmonic components of the integrator are measured. We select $v_1 = 1\cos(2\pi*60*10t)V$ and $v_2 = 0$, the harmonic components are then measured and shown in Fig. 15. Obviously, as the theoretical analysis has predicted, only the second-order harmonic component is observable and is 34dB lower than the fundamental signal.

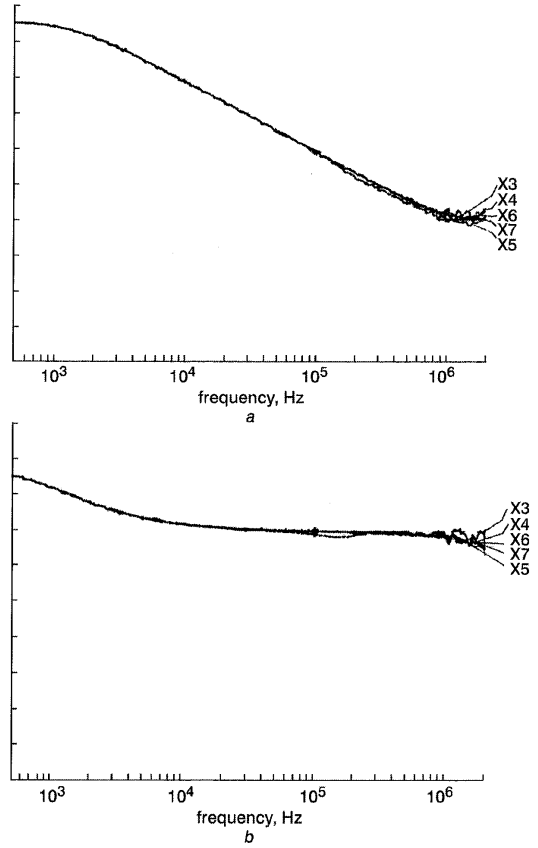

Fig. 12 *Experimental results for integrator shown in Fig. 11*
a Gain amplitude
Vertical scale: 10dB/div
b Phase amplitude
Vertical scale: 45°/div

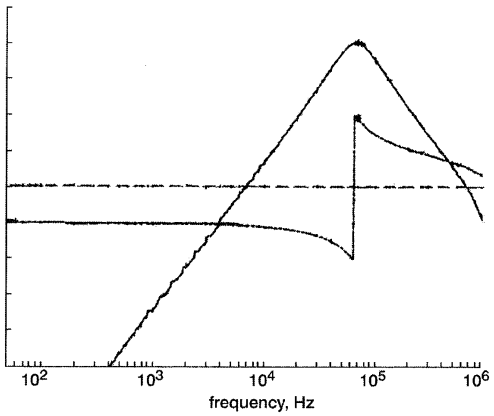

Fig. 13 *Gain amplitude and phase experimental results for bandpass filter derived from Fig. 5 and Table 1*
Vertical scales: 5.000dB/div and 90.000°/div

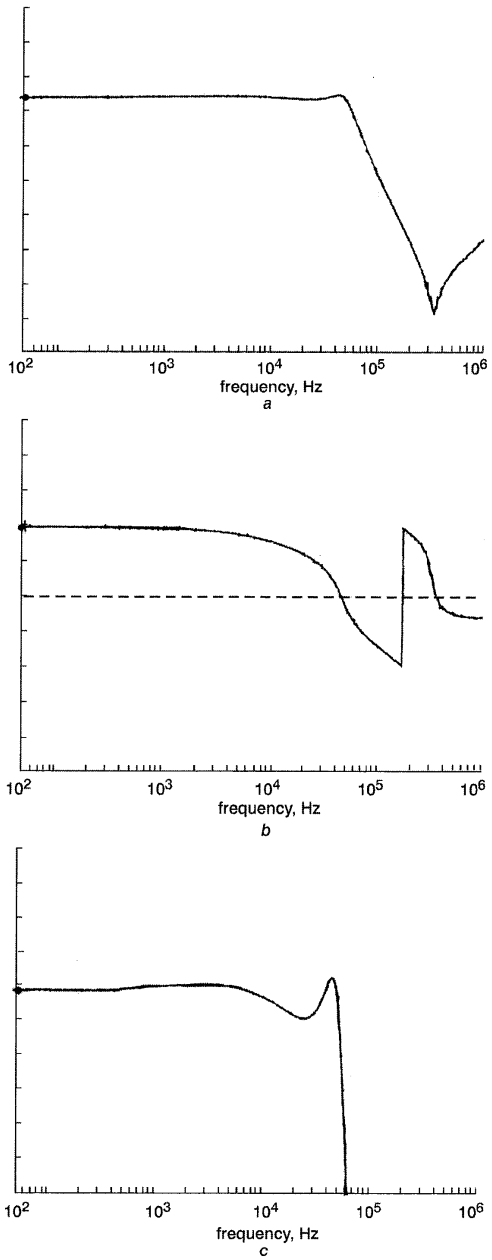

Fig. 14 *Experimental results for third-order Chebyshev lowpass filter derived from Fig. 7*
a Gain amplitude
Vertical scale: 10dB/div; marker 50.000Hz
b Phase
Vertical scale: 90°/div; marker 50.000Hz
c Passband ripple
Vertical scale: 1.000dB/div; marker 50.000Hz

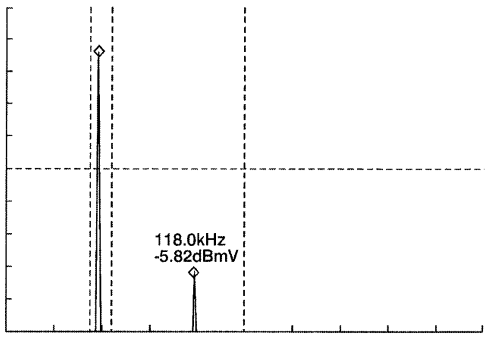

Fig. 15 *Harmonic components spectrum of MOSFET-C integrator*

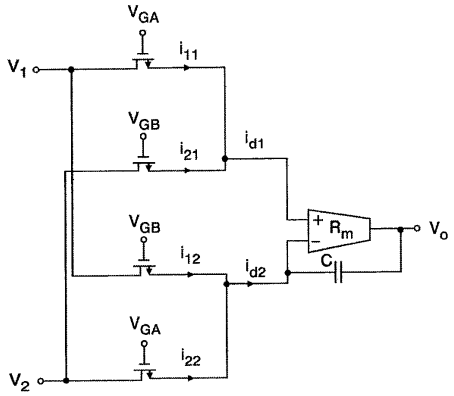

Fig. 16 *Currents i_{11}, i_{12}, i_{21} and i_{22}*

7 Conclusions

We have proposed MOSFET-C filters with reduced parasitic capacitance effect using operational transresistance amplifiers. Signal processing circuits implemented employing OTRAs have almost constant bandwidths because of the use of current-feedback configurations. The proposed circuits are easy to cascade because of the low output impedance of an OTRA. Comparing the proposed circuits with those described previously [6], the voltage-current convertor is not necessary in the proposed circuits; they can directly process voltage signals, and their output can be connected to more circuits without any buffers or current copiers. They can also be tuned by changing the gate voltages of MOS transistors in MRCs and are therefore suitable for many filtering applications.

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9 Appendix

The dependence of channel mobility on the gate voltage can be described as [7, 8]

$$\mu_s = \frac{\mu}{1+\theta(V_G - V_{TH})} \approx \mu\big(1-\theta(V_G - V_{TH})\big) \text{ with } \theta(V_{GS}-V_{TH}) \ll 1 \quad (31)$$

The drain current of an NMOS transistor is

$$i_{DS} = \frac{\frac{W}{2L}\mu C_{ox}}{1+\theta(V_G - V_{TH})} \times \left(V_{GS} - V_{TH} - \frac{1+F_B}{2}v_{DS}\right) v_{DS} \quad (32)$$

where

$$F_B = \frac{\gamma F_s}{2\sqrt{2\phi_p - V_{BS}}} + F_n$$

$$V_{TH} = V_{FB} + 2\phi_p - \sigma v_{DS} + \gamma F_s\sqrt{2\phi_p - V_{BS}} + F_n(2\phi_p - V_{BS})$$

In Fig. 16, the currents i_{11}, i_{12}, i_{21} and i_{22} can be obtained as

$$i_{11} \approx \frac{W}{2L}\mu C_{ox}\big(1-\theta(V_{GA}-V_{TH})\big) \times \left(V_{GA} - V_{TH} - \frac{1+F_B}{2}v_1\right) v_1 \quad (33)$$

$$i_{12} \approx \frac{W}{2L}\mu C_{ox}\big(1-\theta(V_{GB}-V_{TH})\big) \times \left(V_{GA} - V_{TH} - \frac{1+F_B}{2}v_1\right) v_1 \quad (34)$$

$$i_{21} \approx \frac{W}{2L}\mu C_{ox}\big(1-\theta(V_{GA}-V_{TH})\big) \times \left(V_{GA} - V_{TH} - \frac{1+F_B}{2}v_2\right) v_2 \quad (35)$$

$$i_{22} \approx \frac{W}{2L}\mu C_{ox}\big(1-\theta(V_{GB}-V_{TH})\big) \times \left(V_{GB} - V_{TH} - \frac{1+F_B}{2}v_2\right) v_2 \quad (36)$$

Then

$$i_{d1} - i_{d2} = (i_{11}+i_{22}) - (i_{12}+i_{21}) = \frac{W}{2L}\mu C_{ox}(V_{GA}-V_{GB})\Bigg(\Big(1+2\theta\Big(V_{FB}+2\phi_p + \gamma F_s\sqrt{2\phi_p - V_{BS}} + F_n(2\phi_p - V_{BS}) - \frac{V_{GA}-V_{GB}}{2}\Big)\Big) \times (v_1 - v_2) + \theta\left(\left(\frac{1+F_B}{2} - 2\sigma\right)(v_1^2 - v_2^2)\right)\Bigg) \quad (37)$$

and

$$i_{d1} - i_{d2}(s) = \frac{W}{2L}(V_{GA}-V_{GB})\Bigg(\Big(1+2\theta\Big(V_{FB}+2\phi_p + \gamma F_s\sqrt{2\phi_p - V_{BS}} + F_n(2\phi_p - V_{BS}) - \frac{V_{GA}-V_{GB}}{2}\Big)\Big) \times \big(V_1(s) - V_2(s)\big) + \theta\left(\frac{1+F_B}{2} - 2\sigma\right) \times \big((V_1(s) * V_1(s)) - (V_2(s) * V_2(s))\big)\Bigg) \quad (38)$$

where $V_1(s) = \mathrm{L}\{v_1(t)\}$ and $V_2(s) = \mathrm{L}\{v_2(t)\}$, $(V1(s)*V_1(s)) = \int_s^\infty V_1(s)V_1(s-w)dw$, $(V_2(s)*V_2(s)) = \int_s^\infty V_2(s)V_2(s-w)dw$
The output voltage V_o can be represented as

$$V_o(s) = \frac{W}{2L}\mu C_{ox}(V_{GA} - V_{GB})\left(\left(1+2\theta\left(V_{FB} + 2\phi_p + \gamma F_s\sqrt{2\phi_p - V_{BS}} + F_n(2\phi_p - V_{BS}) - \frac{V_{GA}-V_{GB}}{2}\right)\right) \times \left(V_1(s) - V_2(s)\right) + \theta\left(\frac{1+F_B}{2} - 2\sigma\right)\left(V_1(s) * V_1(s)\right) - \left(V_2(s) * V_2(s)\right)\right) \times \frac{1}{sC + 1/Z_m(s)} \tag{39}$$

where $V_o(s) = \mathrm{L}\{v_o(t)\}$.

If we select $v_1 = -v_2 = 0.5\ V_{pp}\cos\omega t$ and assume that $|Z_m(s)|$ is very large, the inverse Laplace transformation of $V_o(s)$, $v_o(t)$ will be given by

$$v_o(s) = \frac{W}{2L}\mu C_{ox}(V_{GA} - V_{GB})\left(\left(1 + 2\theta\left(V_{FB} + 2\phi_p + \gamma F_s\sqrt{2\phi_p - V_{BS}} + F_n(2\phi_p - V_{BS}) - \frac{V_{GA}-V_{GB}}{2}\right)\right)\right) \times \left(\frac{V_{pp}\sin(\omega t)}{C}\right) \tag{40}$$

Thus, the fundamental component exists and the total harmonic distortion is nearly zero. If we set $v_2 = 0$ and $v_1 = V_{pp}\cos\omega t$, the following equation can be obtained:

$$v_o(t) = \frac{W}{2L}\mu C_{ox}(V_{GA} - V_{GB})\left(\theta\left(\frac{1+F_B}{2} - 2\sigma\right)\frac{\theta V_{pp}^2}{2C} + \left(1 + 2\theta\left(V_{FB} + 2\phi_p + \gamma F_s\sqrt{2\phi_p - V_{BS}} + F_n(2\phi_p - V_{BS}) - \frac{V_{GA}-V_{GB}}{2}\right)\right) \times \frac{V_{pp}\sin(\omega t)}{C} - \theta\left(\frac{1+F_B}{2} - 2\sigma\right)\frac{V_{pp}^2\sin(2\omega t)}{4C}\right) \tag{41}$$

Obviously, only the second-order harmonic component exists and the total harmonic distortion can be derived as

$$THD = HD_2 = \frac{\frac{\theta}{4}\left(\frac{1+F_B}{2} - 2\sigma\right)V_{pp}}{1 + 2\theta\left(V_{FB} + 2\phi_p + \gamma F_s\sqrt{2\phi_p - V_{BS}} + F_n(2\phi_p - V_{BS}) - \frac{V_{GA}-V_{GB}}{2}\right)} \tag{42}$$