CMOS Oversampling $\Delta\Sigma$ Magnetic-to-Digital Converters

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***Abstract*—In this paper, two CMOS oversampling delta-sigma ($\Delta\Sigma$) magnetic-to-digital converters (MDCs) are proposed. The first MDC consists of the magnetic operational amplifier (MOP) and a first-order switched-capacitor (SC) $\Delta\Sigma$ modulator. The second one directly uses the MOP to realize a first-order SC $\Delta\Sigma$ modulator. They can convert the external magnetic field into digital form. Both circuits were fabricated in a 0.5-μm CMOS double-poly double-metal (DPDM) process and operated at a 5-V supply voltage and the nominal sampling rate of 2.5 MHz. The dynamic ranges of these converters are at least $\pm$100 mT. The gain errors within $\pm$100 mT are less than 3% and the minimum detectable magnetic field can reach as small as 1 mT. The resolutions are 100 μT for both of the two MDCs. The measured sensitivities are 1.327 mv/mT and 0.45 mv/mT for the first and the second MDC, respectively.**

***Index Terms*—CMOS, delta–sigma modulator, magnetic sensor.**

I. Introduction

MANY physical quantities in life, such as the magnetic field, voice, light, pressure, and temperature, are converted to electrical signals with maximum possible accuracy and reliability [1]. Magnetic sensors can be found in many applications [2]–[5], such as brushless motor controls, computer storage devices, security detectors, automotive applications, etc. Hall devices are by far the most widely used magnetic sensors today. Characteristics of some recently published and commercially available integrated Hall magnetic field sensors are listed in Table I.

Integrated microsensors with on-chip interface circuits are currently replacing discrete sensors in view of their inherent advantages, namely, low cost, high reliability and on-chip processing. To achieve small, robust, and inexpensive microsystems, it is desirable to integrate the magnetic sensor with digital signal processing circuits. Magnetic MOSFET (MAGFET), though not outstanding in sensitivity, is sufficient to fulfill the requirement of some applications, such as monitoring the exposure to magnetic fields [6] and current sensing.

In this paper, two $\Delta\Sigma$ magnetic-to-digital converters (MDCs) with digital outputs being proportional to the external magnetic field are proposed. The first architecture uses two operational amplifiers (op-amps) to implement the magnetic operational amplifier (MOP) and the $\Delta\Sigma$ modulator; the second one uses the MOP to replace the op-amp of the integrator in the $\Delta\Sigma$ modulator for further reducing power consumption and chip area.

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TABLE I
SOME PUBLISHED INTEGRATED MAGNETIC SENSOR SYSTEMS AND COMMERCIALLY AVAILABLE HALL MAGNETIC FIELD SENSORS

Work	Proposed	Ref. [17]	Ref. [6]	Ref. [18]
Technology	CMOS 0.5um	CMOS 0.7um	CMOS 0.8um	BiCMOS
Sensing Device	MAGFET	MAGFET	SSIMT and CCHD	Hall Plate
Range	±100mT	0~800mT	±200mT	±80mT
Sensitivity (mv/mT)	1.327 and 0.45	0.03	Not mentioned	25
System Offset	<0.5mT	0.2%(1.6mT)	Not mentioned	Not mentioned
Resolution	>10bits (100uT)	6 bits	11 bits (100uT)	1mT

II. Magnetic Sensor and Readout Circuit

The operation of MAGFET is similar to that of the Hall sensor [7], [8], except that the resulting output signal is different: the former is current, and the latter is voltage. Both of them output signals proportional to the corresponding excitations. The concave MAGFET device can be utilized, whose physical structure has two split drains [9]–[11]. Under the condition of no external magnetic field imposed, it behaves as two MOSFET devices paralleled with the same drain currents. When the MAGFET device is excited by the external magnetic field, current deviation occurs, and one can convert this current to voltage by means of the readout circuit in [12]. The sensitivity can be obtained from

$$S = \frac{\Delta V_{\text{out}}}{B_{\perp}} = \frac{R \cdot \Delta i}{B_{\perp}} \quad (VT^{-1}) \tag{1}$$

where

- $B_{\perp}$ external magnetic field perpendicular to the surface of MAGFET;
- Δi current deviation in split drains;
- R resistor used for converting current deviation to voltage, ΔV_{out}.

Taking the layout mismatch problem and optimal sensitivity into account simultaneously, the aspect ratio of each MAGFET device in the following sections is chosen to be $W/L = 80\ \mu\text{m}/40\ \mu\text{m}$ and $d = 2\ \mu\text{m}$, according to [13].

III. Magnetic-to-Digital Converters (MDCs)

Two architectures for MDCs are presented. The first one consists of a magnetic field readout circuit realized by the MOP and a first-order $\Delta\Sigma$ modulator. For the second one, the former readout circuit is omitted, and the op-amp in the switched-capacitor (SC) integrator is replaced with a MOP. All the circuits of the MDCs will be described in the following subsections.

A. Magnetic Operational Amplifier (MOP)

The concept of the MOP is similar to that of a conventional op-amp [14]. The difference is that a magnetic-field-induced

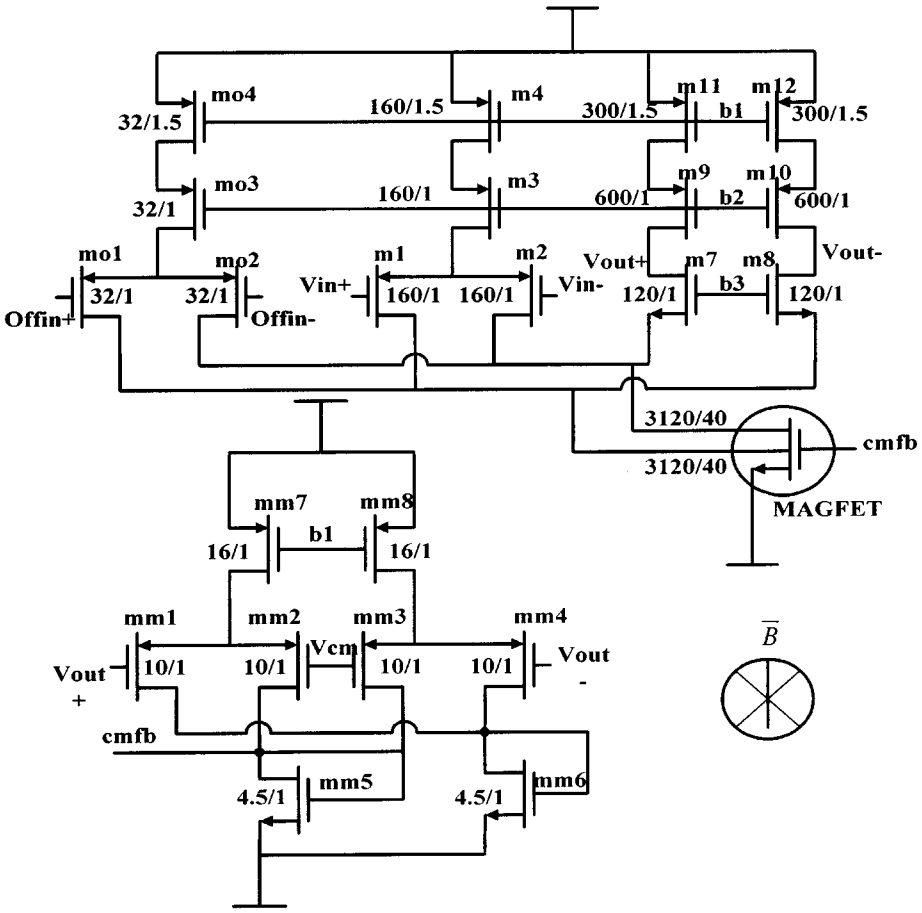

Fig. 1. Fully differential folded-cascode MOP.

voltage V_m is added to the input of the MOP. So the output voltage of the MOP can be expressed as

$$V_{\text{out}} = A \cdot (V_{\text{in}+} - V_{\text{in}-} + V_m). \tag{2}$$

Here, A is the finite dc gain of this op-amp and V_m is the magnetically induced voltage, which is proportional to the applied magnetic field $B_\perp$, and it can be expressed as

$$V_m = S_m \cdot B_\perp \tag{3}$$

where S_m denotes the conversion gain from the magnetic field to the induced voltage. By connecting the MOP in a negative feedback configuration, the linearity can be improved and one can control the gain and sensitivity via resistor ratio.

A fully differential folded-cascode op-amp with common-mode feedback (CMFB) is chosen as the MOP, which is shown in Fig. 1. When no magnetic field is applied, the output drain currents of MAGFET are equal, which means that the voltage difference between the two differential outputs of the MOP is zero. With such condition, the MOP works just like a general op-amp. When a magnetic field is applied, there will be a current imbalance between these two drains. The voltage difference between the differential outputs, $V_{\text{out}+}$ and $V_{\text{out}-}$, will be generated. In order to compensate the small offset inherently in a folded cascode op-amp due to process variation, additional auxiliary input stage, mo1 and mo2, is introduced. The auxiliary differential pair inputs are pulled outside the chip so that they can be trimmed by properly setting the bias voltage through variable resistor network.

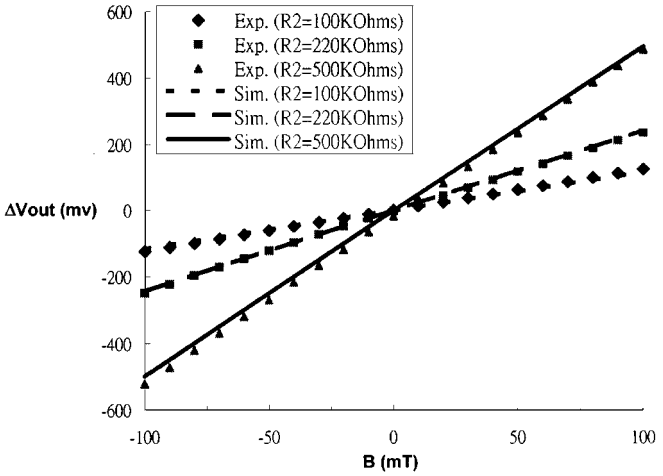

Fig. 2. Simulated and experimental results of the inverting amplifier composed of a MOP and two resistors, $R_1 = 1\ \text{k}\Omega$ and $R_2 = 100\ \text{k}\Omega$, $220\ \text{k}\Omega$, and $500\ \text{k}\Omega$, respectively.

The simulated and measured results of the MOP as an inverting amplifier are shown in Fig. 2. The simulation results are obtained using the macro models of MAGFET in [15]. The lines and the dotted points represent the simulation results and the experimental results, respectively. From Fig. 2, one can observe

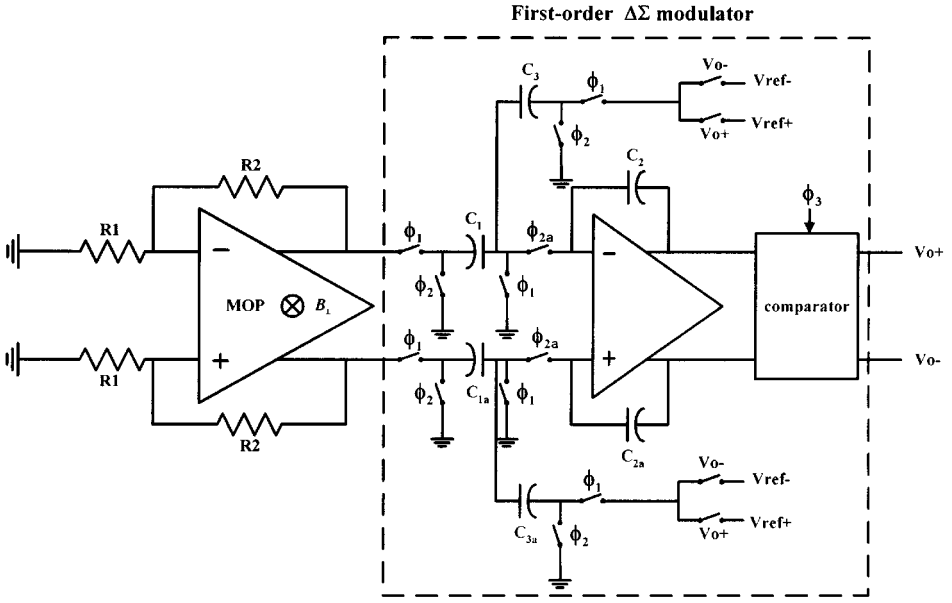

Fig. 3. Implementation of the first MDC architecture.

that the measured results almost match with the simulated ones. The sensitivity is about 1.251 mV/mT when the feedback resistor $R_2 = 100\,\text{k}\Omega$, and the grounded $R_1 = 1\,\text{k}\Omega$. When R_2 is increased up to 500 kΩ, the sensitivity will reach 5.05 mV/mT. The MOP has the higher conversion gains than those of the MAGFET devices only.

B. The First MDC Architecture

The circuits of the first MDC are shown in Fig. 3. The transfer function can be derived as

$$Y = V_m \cdot \left(1 + \frac{R_2}{R_1}\right) \cdot \frac{C_1}{C_2} \cdot \frac{Z^{-1}}{1 + \left(\frac{C_3}{C_2} - 1\right) Z^{-1}} + E \cdot \frac{(1 - Z^{-1})}{1 + \left(\frac{C_3}{C_2} - 1\right) Z^{-1}} \quad (4)$$

where

Y	average digital output of the quantizer;
V_m	magnetically induced voltage on the input of the MOP;
$\left(1 + \frac{R_2}{R_1}\right)$	gain of the readout circuit realized by a MOP;
E	quantization noise.

When choosing $C_3 = C_2$, (4) can be simplified as

$$Y = Vm \cdot \left(1 + \frac{R_2}{R_1}\right) \cdot \left(\frac{C_1}{C_2}\right) Z^{-1} + E\left(1 - Z^{-1}\right). \quad (5)$$

The signal is amplified by two stages, thus one can relax the amplification ratio requirement of each stage. Furthermore, from (5), one can find that the quantization noise is first-order shaped as expected.

To reduce the charge injection and clock feedthrough, the linear resistance transmission gate [16] is used in these circuits.

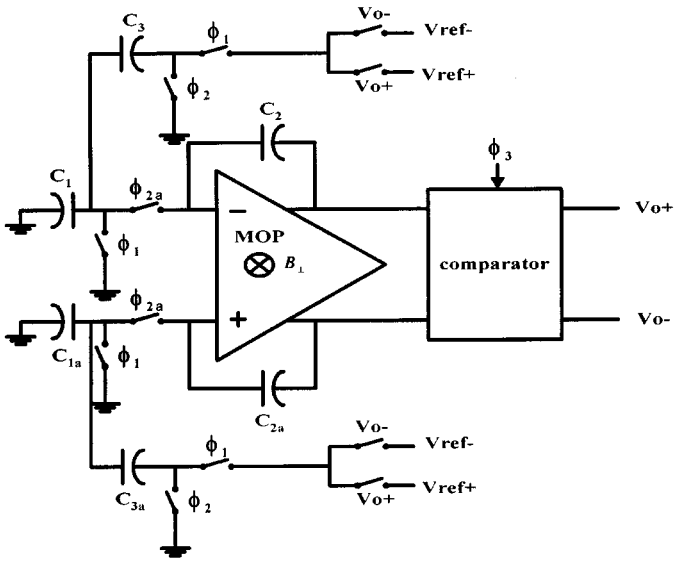

Fig. 4. Implementation of the second MDC architecture.

C. The Second MDC Architecture

The circuits of the second MDC are shown in Fig. 4. The magnetically induced voltage V_m can be regarded as the voltage difference between two input nodes of the MOP in the SC integrator. The quantized output Y will be

$$Y = \frac{(C_1 + C_3)V_m}{C_2 + (C_3 - C_2)Z^{-1}} + \frac{C_2\left(1 - Z^{-1}\right)}{C_2 + (C_3 - C_2)Z^{-1}} E. \quad (6)$$

Let $C_3 = C_2$, and the following expression will be obtained.

$$Y = \left(1 + \frac{C_1}{C_2}\right) \cdot V_m + E\left(1 - Z^{-1}\right). \quad (7)$$

Note that the output Y is proportional to V_m and the quantization error E will be first-order shaped to high frequency, also. The conversion gain is determined by capacitor ratio irrespective of resistors compared to the first architecture. Although the

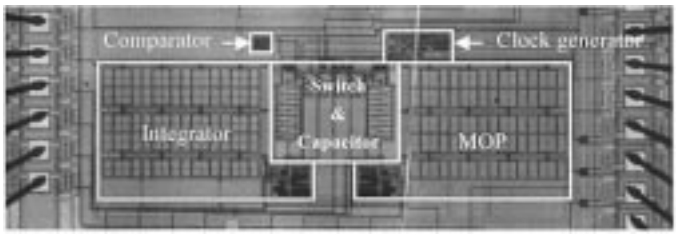

Fig. 5. Photograph of the first MDC.

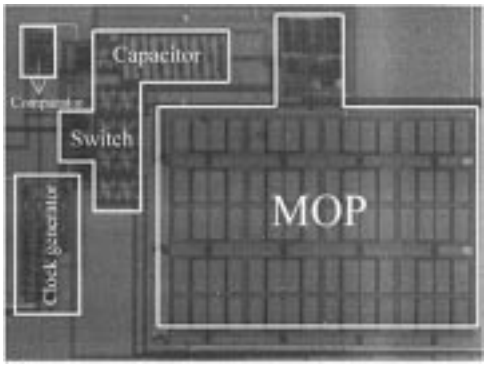

Fig. 6. Photograph of the second MDC.

gain factor is less flexible than the previous architecture, it is worth it to trade this for reduction of power consumption and chip area.

IV. Experimental Results

Two MDCs have been implemented in a standard 0.5-μm double-poly double-metal (DPDM) CMOS process. These chips have been encapsulated in a standard IC package and have been exposed to magnetic field in the range of ± 100 mT. This chip has been characterized by applying a dc magnetic field. The number of samples is 65 536 points, which is large enough for average accuracy while still maintaining a tolerable measurement time. Through an off-chip up–down counter, the digital average value of the comparator is obtained after shifting the bits of the output code depending on the sampled numbers. The average value is then fed into a digital-to-analog converter (D/A) to return to an analog voltage, which is used as our measurement result.

In the first MDC architecture, off-chip resistors R_1 and R_2 are 1 kΩ and 220 kΩ, respectively. In the $\Delta\Sigma$ modulator, the capacitor values are $C_1 = C_{1a} = 3$ pF and $C_2 = C_{2a} = 1$ pF. A layout photograph of the first MDC scheme is shown in Fig. 5. The circuit (without pad) occupies an area of 2.2 mm $\times$ 0.85 mm.

In the second MDC architecture, the capacitor values in the $\Delta\Sigma$ modulator are $C_1 = C_{1a} = 220$ pF (off-chip) and $C_2 = C_{2a} = 1$ pF. A layout photograph of the second MDC is shown in Fig. 6. The circuit (without pad) occupies an area of 0.84 mm $\times$ 1.11 mm. Measurement results are shown in Figs. 7–9. The solid line indicates the approximated line of the measured data for the MDCs. The dynamic ranges of these converters are at least ± 100 mT. The measured sensitivities are 1.327 mv/mT and 0.45 mv/mT for the first and the second MDC, respectively. The error between the measured points and

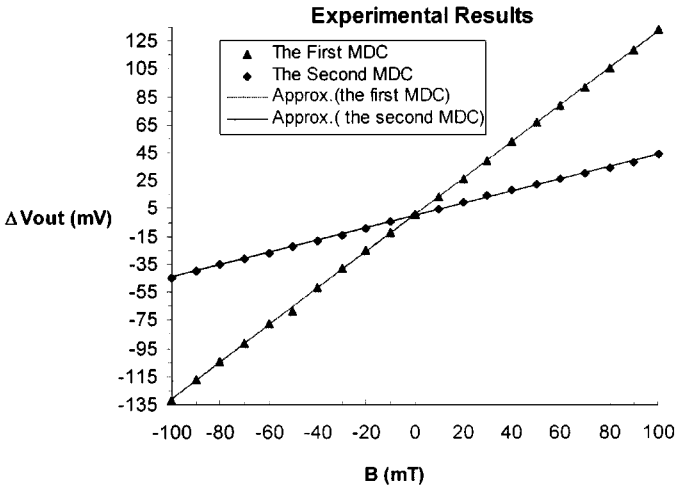

Fig. 7. The average value of the comparator output from measurement (-100 mT $\leq B \leq 100$ mT).

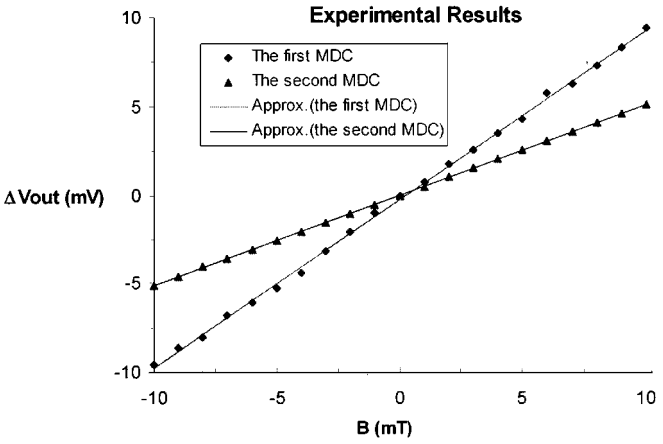

Fig. 8. The average value of the comparator output from measurement (-10 mT $\leq B \leq 10$ mT).

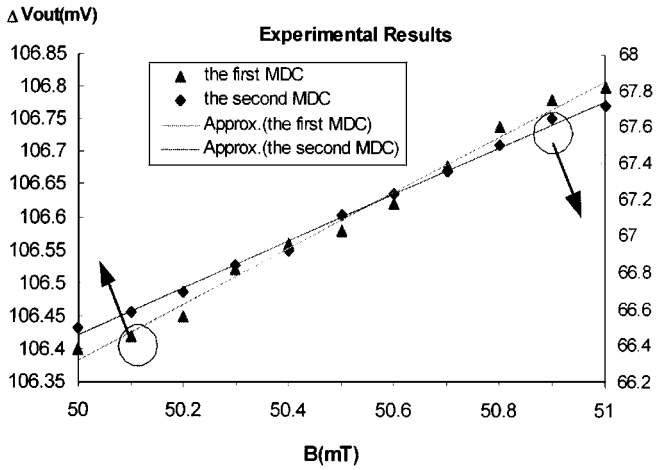

Fig. 9. The average value of the comparator output from measurement (50 mT $\leq B \leq 51$ mT).

the approximated line is under 3%, and the minimum detectable magnetic field can reach as small as 1 mT. Further measurement is also performed as shown in Fig. 8, where a smaller magnetic range is imposed on this system, and the linearity of the transfer

TABLE II
PERFORMANCE SUMMARIES

Parameter	The first MDC	The second MDC
Supply voltage	5v	5v
Power consumption	49.3mw	32.4mw
Gain errors	3%	3%
Sensitivity	1.327mV/mT	0.45mV/mT
Resolution	100uT	100uT
Min detectable Magnetic field	1mT	1mT
Dynamic range	±100mT	±100mT
Sampling frequency	2.5MHz	2.5MHz

curve is still maintained. The resolutions can reach as small as 100 μT for both of the two MDCs seen from Fig. 9. The resolution of the MDC under dc excitation is limited by offset (mainly by $1/f$ noise), and not by thermal noise. The power consumption of the first MDC and the second one are 49.3 and 32.4 mW, respectively.

Note that the sensitivities of the MDCs are much smaller than those of the MOP. This is because the sizes of MAGFET in the MDCs are reduced for chip area consideration. Take the capacitor and resistor values into (5) and (7); the sensitivity of the first MDC should be three times as large as that of the second MDC, which is close to our measurement results $(1.327/0.45 = 2.948)$. The discrepancy is probably due to process variation. For the range between $\leqq 0.5$ mT, the slope is almost zero and forms a dead zone. Thus, a conclusion is made conservatively that the minimum detectable magnetic field is 1 mT, which is not equal to the resolution of 100 μT. This is because the weak signal is overwhelmed by offset and noise. In summary, these results are similar to the outcome in the previous section and indicate that the average digital output of the MDC is proportional to the applied magnetic field.

V. CONCLUSION

In this paper, two MDCs are presented. The magnetic field is a low-frequency signal, therefore, a $\Delta\Sigma$ modulator is used to transfer the magnetic signal into digital form with its noise-shaping characteristic. The performance of these MDCs are summarized in Table II. Comparisons with other recently published integrated magnetic to digital systems are listed in Table I, which proves that the proposed MDCs are acceptable in some practical applications. In the future, more elaborate offset cancellation techniques and higher order $\Delta\Sigma$ modulation can be included to enhance the resolution of the MDC.

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