exhibit a significant mainlobe reduction, to approximately 25% of conventional BPSK scheme with bidirectional, linear phasor rotation for the same sidelobe level of about -25 dB. They are not symmetrical around the carrier frequency f_c, but their central frequencies appear shifted above and below f_c for clockwise and anticlockwise phasor rotation, respectively. In this respect, the spectra resemble those of an SSB modulation scheme, where the direction of the phasor rotation will determine which part of the frequency spectrum (upper or lower sideband) will be occupied by the modulated signal.

Conclusions: The current work shows that the mainlobe width of a constant envelope PSK modulation scheme can be significantly reduced by 25% (for the same sidelobe level), by employing smooth, monotonically increasing (or decreasing) sinusoidal phase variations. Computer simulation of constant envelope BPSK schemes was used to calculate the spectra for conventional and monotonic phase variations. Comparison showed the mainlobe width of the proposed technique to be reduced by approximately 25% of that for conventional BPSK schemes for the same sidelobe levels. It also showed it to be shifted with respect to the carrier frequency to an upper or lower band depending on the direction of phasor rotation on the unit circle. In this respect, the spectrum of the transmitted signal resembles that of a classical SSB modulation scheme.

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EULER DIFFERENTIATOR WITH REDUCED CHANNEL LENGTH MODULATION

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Indexing terms: Signal processing, Switched-current circuits, Circuit design

A new design method for the Euler differentiator using the MOSFET switched-current (SI) technique with reduced channel length modulation effect is proposed. The realisation of these circuits requires only current mirrors, voltage-to-current convertors [1], and analogue switches. Because the input terminal of this differentiator is a virtual ground, signal processing circuits which have cascade structures can be easily implemented. In the Letter, a 4th-order lowpass filter is designed to demonstrate the performance of this differentiator. Simulation results which agree well with the theoretical analysis have been obtained.

Introduction: With the rapid development of MOS VLSI technology, discrete-time signal processing (DSP) circuits have been receiving much attention. Recently, current-mode analogue signal processing techniques have become important. The properties of these current-mode circuits enable them to outperform their voltage-mode counterparts in applications where the performance of the voltage-mode circuits is limited. Among these current-mode circuits, switched current (SI) is a new sampled-data technique. It needs only a standard CMOS process without any special procedure for realising linear floating capacitors which are required in switched-capacitor (SC) circuits. That is why the future of CMOS SI circuits is particularly promising.

In this Letter, we use voltage-to-current convertors to reduce the effect of channel length modulation in SI differentiators by fixing the voltage between drain and source of MOS transistors (V_{DS}). Simulation results which agree well with the theoretical analysis are presented in the following Section.

Circuit description: In the saturation region, the drain current I_D of MOS transistors can be described by the following equation [2]:

$$I_D = K(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \tag{1}$$

where

$$K = \frac{W}{2L}\mu C_{ox}$$

$$V_T = V_{T_o} + \gamma[(2|\varphi_p| + V_{SB})^{1/2} - (2|\varphi_P|)^{1/2}]$$

λ is the channel length modulation parameter, and φ_P is strong inversion surface potential.

For AC analysis, the small signal part of drain current I_D, dI_D, can be expressed as

$$dI_D = \frac{\partial I_D}{\partial V_{GS}} dV_{GS} + \frac{\partial I_D}{\partial V_{DS}} dV_{DS} \tag{2}$$

The second term of eqn. 2 results from the channel length modulation in MOS transistors. If we can reduce the change of $V_{DS}(dV_{DS})$ by fixing the value of V_{DS} (that is $dV_{DS} \simeq 0$), the AC signal dI_D will be only the function of V_{GS} and the effect of channel length modulation will be eliminated. We may, therefore, use voltage-to-current convertors implemented by CMOS differential input comparators [3] to provide virtual ground terminals which fix the voltage V_{DS} of the MOS transistors in the current mirror structure and obtain an SI differentiator with better performance. The SI differentiator is shown in Fig. 1, where two nonoverlapping clocks ϕ_1 and ϕ_2 are employed to control switches. The circuit operates as follows. The total source current in M19 and M20 after sampling by ϕ_1 and ϕ_2 is equal to I_{in} except for a pure time delay.

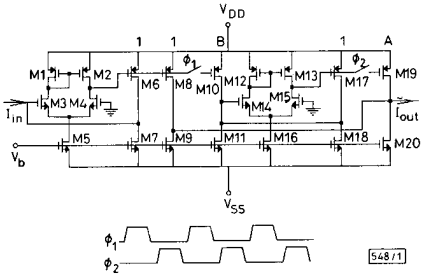

Fig. 1 *Euler differentiator with reduced channel length modulation*

The output signal I_{out} is established in the output weighted transistors (weight A for M19 and M20, B for M8 and M9) as soon as clock ϕ_2 is on. Thus we have

$$I_{out}(n) = AI_{in}(n-1) - BI_{in}(n) \tag{3}$$

Expressed in the z domain with $A = B$

$$I_{out}(n) = AI_{in}(z)[z^{-1} - 1] \tag{4}$$

Therefore

$$H(z) = \frac{I_{out}(z)}{I_{in}(z)} = A[z^{-1} - 1] \tag{5}$$

This corresponds to the backward Euler mapping $[s \rightarrow (1 - z^{-1})/T]$ of a differentiator.

Secondly, the current scaler shown in Fig. 2 is used to scale current up or down by changing the aspect ratios of the MOSFET devices. Because the input terminal of this circuit is a virtual ground, the effect of channel length modulation will not occur. Output currents I_{n_i} and I_{p_i} can be derived as

$$I_{n_i} = -a_i \times I_{in} \tag{6}$$

$$I_{p_i} = b_i \times I_{in} \tag{7}$$

where a_i and b_i are the weights of aspect ratios.

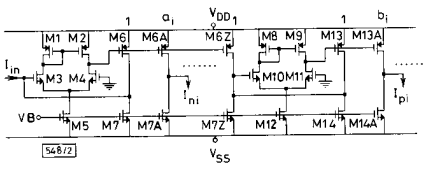

Fig. 2 *Current scaler circuit*

Using current scalers and Euler differentiators, FIR filters can be implemented with $z^{-1} - 1$ as the basic blocks. Their transfer function can be described as

$$H(z) = \frac{Y(z)}{X(z)} = \sum_{k=0}^{N} b_k (z^{-1} - 1)^k \tag{8}$$

According to eqn. 6, a linear-phase 4th-order lowpass FIR filter [4] is constructed as shown in Fig. 3. Its transfer function can be described as

$$H(z) = (z^{-1} - 1)^4 + 5(z^{-1} - 1)^3 + 10(z^{-1} - 1)^2 + 10(z^{-1} - 1) + 5 \tag{9}$$

The sensitivities of the SI differentiator based FIR filter with respect to variations of the multiplier coefficients are given by

$$D_{b_i}^{H}(z) = \frac{\partial H(z)}{\partial b_i} = (z^{-1} - 1)^k \tag{10}$$

The sensitivities of the differentiator-based FIR filters can be shown to be superior to those of delay-element based FIR filters [5].

Table 1 ASPECT RATIOS OF MOSFET DEVICES IN FIG. 1 AND FIG. 2

Fig. 1		Fig. 2	
Devices	*W/L*	Devices	*W/L*
M1 M2 M12 M13	15/5	M1 M2 M8 M9	15/5
M3 M4 M14 M15	40/5	M3 M4 M10 M11	40/5
M5 M16	5/5	M5 M12	5/5
M6 M8 M10 M17 M19	30/5	M6 M6Z M13	30/5
M7 M9 M11 M18 M20	10/5	M7 M7Z M14	10/5
		M13A	$b_i \times 30/5$
		M14A	$b_i \times 10/5$

b_i: coefficient of eqn. 8; W and L in μm

Simulation results: A linear-phase 4th-order lowpass FIR shown in Fig. 3 is simulated by PSPICE using 3·5 μm CMOS process parameters to demonstrate the high frequency performance of this differentiator. The corresponding transistor aspect ratios are given in Table 1. The simulated frequency responses of this FIR filter for 10 MHz sampling rate which agree well with the theoretical analysis are shown in Fig. 4.

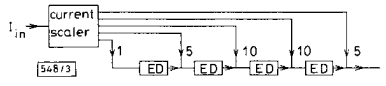

Fig. 3 *Block diagram of 4th-order SI linear-phase FIR lowpass filter*

Conclusion: A new design method for the Euler differentiator with reduced channel length modulation has been successfully developed by using the SI technique. Because the input terminal of this differentiator is a virtual ground, it is convenient

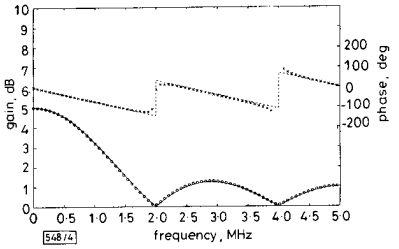

Fig. 4 *Frequency responses of circuit shown in Fig. 3 with 10 MHz sampling rate*

for implement signal processing circuits that have cascade structures. Meanwhile, the proposed SI differentiator-based FIR filters will have lower component sensitivities than the delay-element-based ones. Simulation results of a linear phase, 4th-order lowpass filter which agree well with the theoretical analysis are presented to demonstrate the feasibility of this differentiator.

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AMPLITUDE SCALE METHOD: NEW AND EFFICIENT APPROACH TO MEASURE FRACTAL DIMENSION OF SPEECH WAVEFORMS

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Indexing terms: Speech processing, Signal processing, Algorithms

A new algorithm to measure the fractal dimension of speech waveforms is presented. Limitations of the box counting method in determining the fractal dimension of speech waveforms are also explained.

Introduction: In fractal-based signal processing, which the authors call FSP, fractal dimension (FD) is an often used measurement. A very popular approach to obtain the fractal dimension of the underlying signal is the box counting method [1]. However, recent work in speech processing has