Nonlinear circuit applications with current conveyors

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Abstract: Integrable nonlinear building blocks such as multipliers, dividers, and piecewise linear approximation circuits using current conveyors are presented. Several practical circuits including an amplitude modulator, a squarer, a square rooter, and nonlinear resistors also have been demonstrated experimentally. The results presented in the paper will facilitate realisations of nonlinear circuits using CCIIs.

1 Introduction

Current conveyors (CCs) are useful in many analogue signal processing circuits [1, 2]. Since the gain–bandwidth product of an operational amplifier (OA) is finite, the higher the gain it realises, the less bandwidth it possesses. Based on this, several constant-bandwidth amplifiers have been presented using various current-mode active elements [3, 4]. It has been demonstrated that the major advantage of CCs over conventional OAs, is that they are able to provide wider bandwidth and better accuracy [5]. Several implementations have emerged such as active filters, oscillators, and amplifiers using CCs. However, few implementations with CCs are realised to synthesise various analogue nonlinear signal processing circuits.

Recently, the application of continuous-time techniques (i.e. MOSFET-C, OTA-C techniques etc.) in the analogue MOS integrated circuits has received much attention because such implementations can tolerate the variations in the fabrication processes and environment conditions, provided some automatic tuning scheme is employed [6, 7]. Among them, the OTA-C technique uses operational transconductance amplifiers and capacitors to synthesise various linear and nonlinear function circuits [8, 9] which are attractive for integration. The MOSFET-C technique uses MOS transistors biased in the nonsaturation region as voltage-controlled resistors. Both of them have performance limitations owing to real active elements. The OTA-C technique is subject to the limited input voltage swing, frequency dependent transconductance, driving capability etc, whereas the MOSFET-C technique uses OAs as active elements and its limitations includes nonideal OAs, nonresistive characteristics of MOS transistors etc. It is difficult to decide whether the MOSFET-C technique is better than the OTA-C technique. However, it can provide more efficient utilisation of the finite bandwidth circuits for CCIIs than OAs in the MOSFET-C technique [10].

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2 Circuit description

Basically a CCII, as shown in Fig. 1, is a three-terminal network whose characteristics can be described as

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm A_i & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \quad (1)$$

where the plus and minus signs of the current transfer ratio A_i denote CCII+ and CCII−, respectively. In the

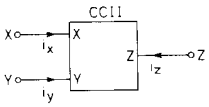


Fig. 1 *Circuit symbol of a CCII*

following analysis, the current transfer ratio A_i is assumed to be equal to one if not specifically mentioned, CCII-based nonlinear building blocks including multipliers, dividers, and piecewise-linear approximation circuits are presented in the following Sections.

2.1 Multiplier

The drain current of a MOS transistor biased in the nonsaturation region can be expressed by the following equations when the drain-to-source voltage is zero [11]

$$I_D = F(V_D, V_G) - F(V_S, V_G) \quad (2)$$

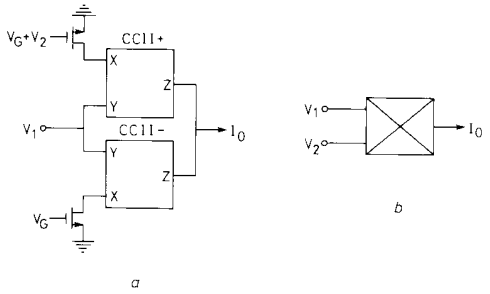
with

$$F(V_X, V_G) = 2K(V_G - V_B - V_{FB} - \phi_B)V_X - K(V_X - V_B)^2 - \tfrac{4}{3}K\gamma(V_X - V_B + \phi_B)^{3/2}$$

$$K = \frac{W}{2L}\mu C_{0x}$$

$$\gamma = \frac{1}{C_{0x}}(2qN_A\varepsilon_s)^{1/2}$$

where I_D is the drain current in the nonsaturation region, W and L are channel width and length, respectively, μ is the effective mobility, V_{FB} is the flat-band voltage, N_A is the substrate doping concentration, C_{0x} is the gate oxide capacitance per unit area, ϕ_B is the approximate surface potential in strong inversion, V_G, V_B are the gate and substrate voltage, respectively, and V_x is either the drain voltage V_D or the source voltage V_S of the MOS transistor. A four-quadrant multiplier with current output can be constructed as shown in Fig. 2*a*. The corresponding block diagram is represented in Fig. 2*b*. Assuming the



a

Fig. 2
a circuit of proposed multiplier
b symbol of multiplier, shown in Fig. 2*a*

aspect ratios of these two MOS transistors, shown in Fig. 2*a*, to be equal, the transfer function of the multiplier can be obtained as

$$I_0 = K_M V_1 V_2 \tag{3}$$

where $K_M(=2K)$ is the multiplier constant. The operation constraint of this multiplier is

$$V_1 \leqslant \min [V_G + V_2 - V_T, V_G - V_T] \tag{4}$$

where V_T is the threshold voltage of the two MOS transistors shown in Fig. 2*a*. It should be noted that the nonlinearities of the MOS transistors, including even and odd harmonics can be cancelled simultaneously. If we exchange the gate voltages of these two MOS transistors, a similar multiplier can be obtained with

$$I_o = -K_M V_1 V_2 \tag{5}$$

Therefore, the sign of K_M can be either positive or negative.

2.2 Divider

We can also synthesise a divider circuit using the proposed multiplier. Before building a divider, a linear voltage-to-current (V–I) converter is required. A linear V–I converter can be easily implemented using a CCII and a resistor. Hence, a simple divider can be constructed as shown in Fig. 3. Routine circuit analysis yields

$$V_o = -\frac{GV_1}{K_M V_2} = K_D \frac{V_1}{V_2} \tag{6}$$

where G is the conductance of the resistor, shown in Fig. 3, and $K_D\ (= -G/K_M)$ is the divider constant which can be positive or negative depending upon the sign of K_M. Although the circuit shown in Fig. 3 can perform the division function, we propose a new integrable linear V-I converter which is composed of a CCII and four MOS transistors biased in the nonsaturation region, shown in Fig. 4*a*. Applying eqns. 1 and 2, we can express the transfer characteristics of this linear V–I converter as

$$I_o = 2K(V_{GA} - V_{GB})(V_{in1} - V_{in2}) \tag{7}$$

Therefore, a divider, which similar to the divider circuit of Fig. 2, can be constructed in Fig. 4*b*. Its block repre-

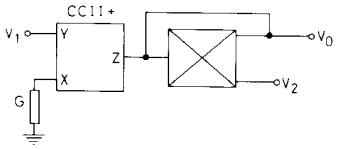
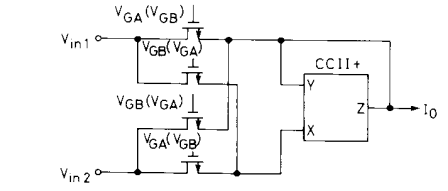


Fig. 3 *Circuit of proposed divider*



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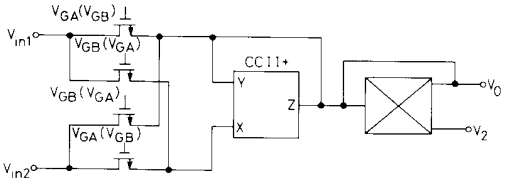

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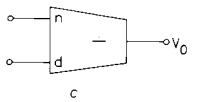


c

Fig. 4
a Proposed voltage-to-current converter
b Circuit of integrable divider
c Symbol of divider circuit

sentation is shown in Fig. 4*c*. The transfer function is given as

$$V_o = K_D \frac{V_{in1} - V_{in2}}{V_2} \tag{8}$$

where

$$K_D = \frac{\left(\frac{W}{L}\right)_C}{\left(\frac{W}{L}\right)_M} (V_{GA} - V_{GB})$$

$(W/L)_C$ and $(W/L)_M$ are the aspect ratios of the transistors of the V–I converter and the multiplier, respectively.

2.3 Piecewise-linear approximation circuits

Recently, in the area of precision rectification, current conveyors have been utilised and have shown very promising results [12, 13]. Here we use diodes, resistors, and CCIIs to implement the piecewise-linear functions. The basic building blocks for the piecewise-linear functions

can be classified into voltage-mode and current-mode limiters according to the types of input signals, as shown in Figs. 5 and 6, respectively. First, we consider the circuit shown in Fig. 5*a*. V_{in} is an input voltage and V_B is

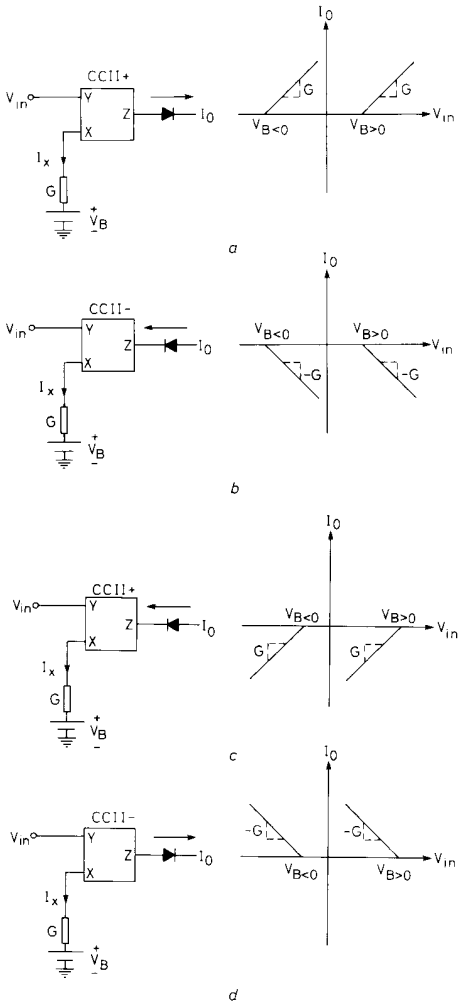


Fig. 5 *Voltage-mode piecewise linear function building blocks*

a breakpoint voltage. If $i_x > 0$ (i.e. $[(V_{in} - V_B)/R] > 0$), the current i_x will flow through the diode. But if $i_x < 0$, no current flows through the diode. Therefore, the transfer characteristic of the voltage limiter (VL) can be written as

$$I_0 = \begin{cases} 0 & \text{for } V_{in} \leqslant V_B \\ G(V_{in} - V_B) & \text{for } V_{in} > V_B \end{cases} \quad (9)$$

where G is the conductance of the resistor shown in Fig. 5*a*. Similar results can also be obtained for the remaining circuits in Figs. 5*b–d*. Let us now consider the circuit of a current limiter (CL), as shown in Fig. 6*a*, its transfer characteristics can be expressed as

$$I_0 = \begin{cases} -(I_B + I_{in}) & \text{for } I_{in} \leqslant -I_B \\ 0 & \text{for } I_{in} > -I_B \end{cases} \quad (10)$$

where I_B is the breakpoint DC current. The remaining CLs shown in Figs. 6*b–d*, have similar transfer characteristics to eqn. 10 depending on the type of CCIIs and the diode.

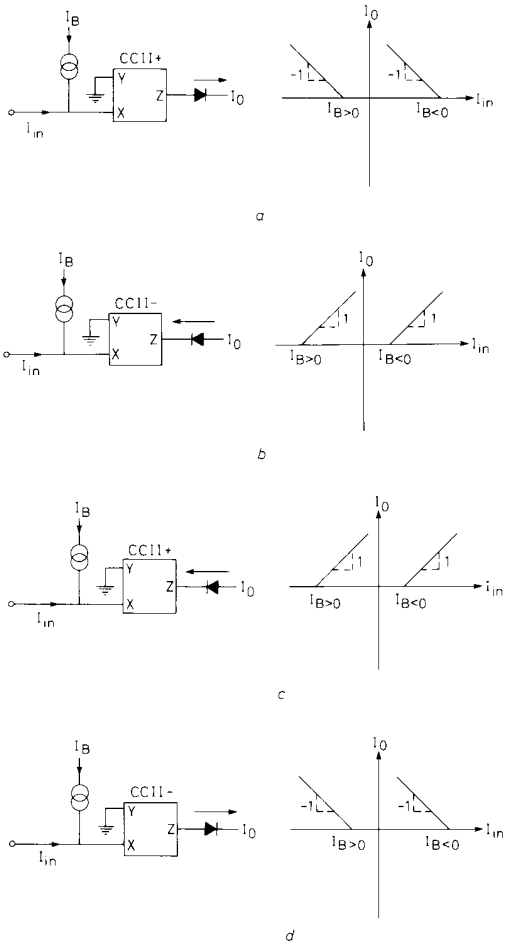


Fig. 6 *Current-mode piecewise linear function building blocks*

3 Performance analysis

A practical CCII+, shown in Fig. 7, can be constructed using a commercial OA (LF356) together with current mirrors composed of transistors arrays (CA3096AE) [14]. Fig. 8 shows a simplified macromodel for the OA. The resistance R_i, typically 1 MΩ or so, is the open-loop differential input impedance and R_0, typically about 100 Ω, is the open-loop output impedance. The dependent voltage source, Av_i represents the open-loop differential voltage gain of the OA, where A can be expressed as

$$A = \frac{A_o \omega_1}{s + \omega_1} \quad (11)$$

Factor A_o is the DC open-loop voltage gain, and ω_1 is the 3 dB corner frequency of the OA. Assume that the bandwidth of the current mirrors to be higher than that of the OA. Then we substitute the simplified model into

the proposed multiplier, shown in Fig. 2. The nonideal transfer function of this multiplier can be approximately expressed as

$$I_o = K_M V_1 V_2 \frac{1}{1 + (s/B)[1 + (R_o/R_{eq})]} \quad (12)$$

where $B\ (= A_\phi \omega_1)$ is the gain-bandwidth product of the OA and R_{eq} is the equivalent resistance of the MOSFETs biased in the nonsaturation region, as shown in Fig. 2*a*.

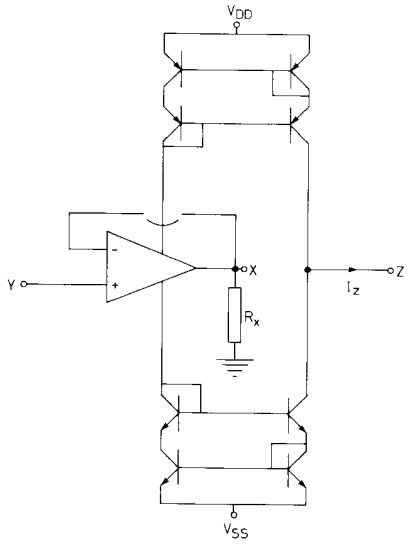


Fig. 7 *Practical realisation of a CCII+ proposed in Reference 13*

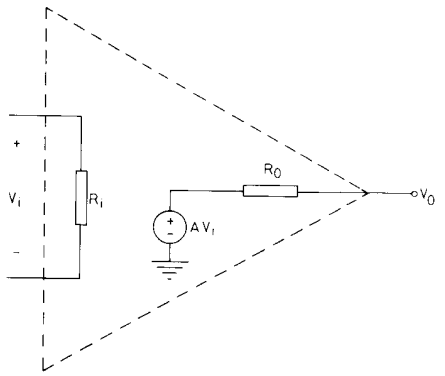


Fig. 8 *Simplified macromodel of an operational amplifier*

The bandwidth of this multiplier is dependent on the ratio of the equivalent resistance of the MOS transistors and the effective output resistance R_o of the OA. We can therefore utilise the finite bandwidth of the OA efficiently by appropriately designing the values of R_{eq} and R_o.

For the divider, shown in Figs. 3 and 4*b*, it is necessary to discuss the stability of the circuits. If we assume that there is a parasitic capacitor C_p at the output node of the divider circuit, then eqn. 6 can be rewritten as

$$V_o = \frac{-GV_1}{K_M V_2 - sC_p} \quad (13)$$

To be stable, the pole of transfer function of this divider must be in the left-half plane (LHP), which dictates that

$$K_M V_2 < 0 \quad (14)$$

A similar stable condition can also be derived for the divider shown in Fig. 4*b*.

4 Experimental results

To verify the theoretical analysis, the proposed nonlinear circuits are experimentally demonstrated. The NMOS transistors in the MOS transistor arrays (CA3600E) are used to implement the circuit of Fig. 2*a*. The measurement results of these building blocks and their applications are summarised below.

4.1 Multiplier, modulator, and squarer

The multiplier, shown in Fig. 2*a*, is breadboarded, its DC transfer curves are shown in Fig. 9, where V_1 is a 1 kHz

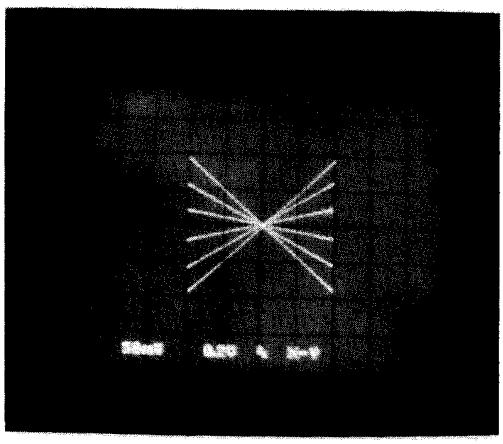


Fig. 9 *DC transfer curves of multiplier, shown in Fig. 2a*

triangular waveform of 0.1 V_{pp} in amplitude and V_2 are DC signals varied between ± 0.5 V in 0.2 V steps with $V_G = 2.6$ V. It is well known that a four-quadrant multiplier can be used as a modulator and a squarer. The first application of the proposed multiplier is an amplitude modulator. Two 0.1 V_{pp} sinusoidal signals with different frequencies (3 kHz and 100 kHz) are applied to the multiplier shown in Fig. 2*a*. The experimental data are measured with a 12 kΩ output resistor (see Fig. 10). The second circuit application is a continuous-time squarer. A 0.1 V_{pp} sinusoidal signal at frequency 10 kHz is applied to both the inputs of the multiplier. The results are shown in Fig. 11.

4.2 Divider and square rooter

The divider, shown in Fig. 3, is also implemented and its DC transfer curves are shown in Fig. 12, where V_1 is switched between two symmetrical constant values (± 0.1 V) and V_2 is a negative ramp waveform between 0 V and -0.5 V at a frequency of 1 kHz with $V_G = 2.6$ V. Its time-domain response is shown in Fig. 13. The circuit of a square rooter is shown in Fig. 14. As an example, a 0.1 V_{pp} sinusoidal waveform with frequency 10 kHz is applied to the input of the square rooter, the experimental results are shown in Fig. 15.

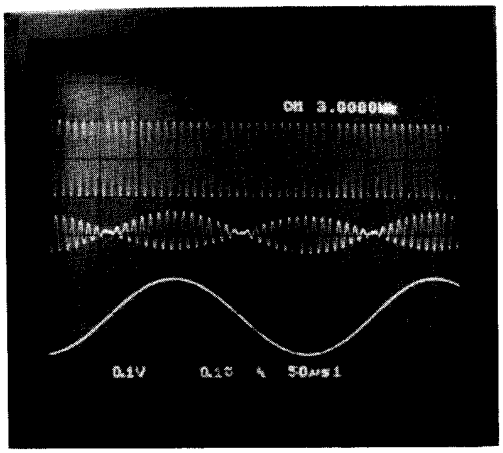


Fig. 10 *Modulation application of multiplier.*
Upper trace, 100 kHz (0.1 V/div)
Lower trace, 3 kHz (0.1 V/div)
Middle trace, modulated output (0.1 V/div)
Horizontal scale is 50 μs/div

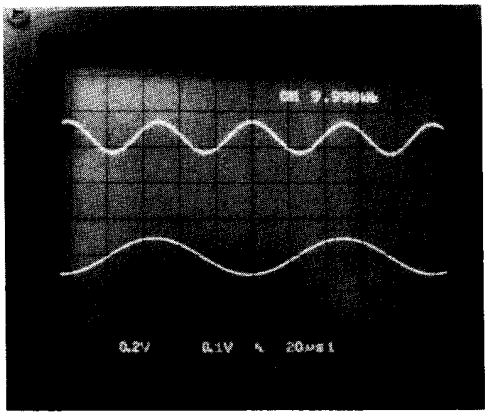


Fig. 11 *Experimental result of a squarer*
Upper trace, output of square (0.2 V/div)
Lower trace is input of squarer (0.1 V/div). The horizonal scale is 20 μs/div

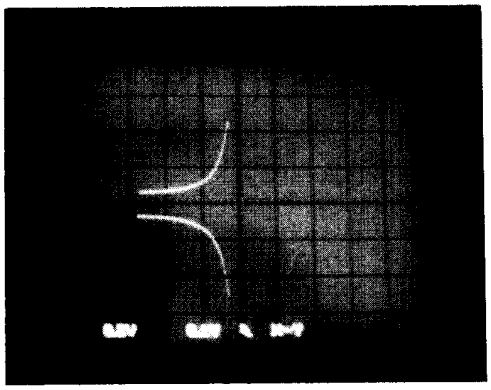


Fig. 12 *DC transfer curves of divider, shown in Fig. 3*
$R = 12\ K\Omega$
Horizontal and vertical scales are 0.2 V/div

4.3 *Piecewise-linear approximation circuits*

The applications of the VLs and CLs for the realisation of nonlinear functions can also be implemented. A desired nonlinear function is shown in Fig. 16*a*, Fig. 16*b* shows its corresponding hardware implementation and the experimental result is given in Fig. 16*c*.

5 Conclusions

Several integrable nonlinear building blocks using CCIIs such as a multiplier, a divider, and CLs, have been presented. Several applications including multiplication,

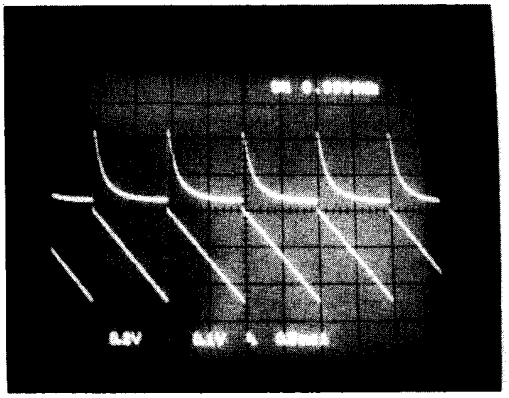


Fig. 13
Upper trace (0.1 V/div), output of a divider, shown in Fig. 3
Lower trace (0.2 V/div), input of Fig. 3 which is a negative ramp between 0 V and −0.5 V
Horizontal scale is 0.5 ms/div

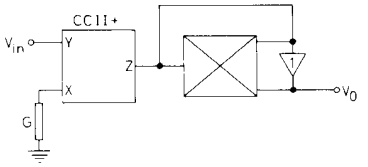


Fig. 14 *Circuit of a root squarer*

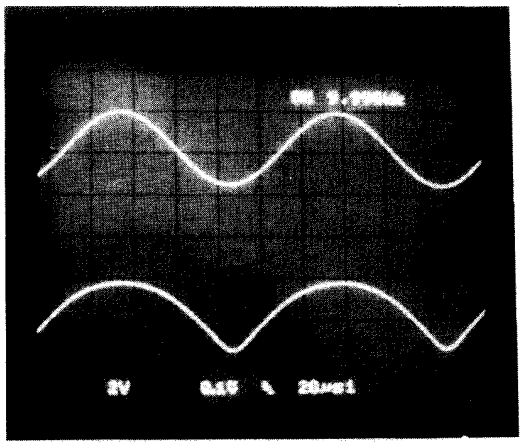
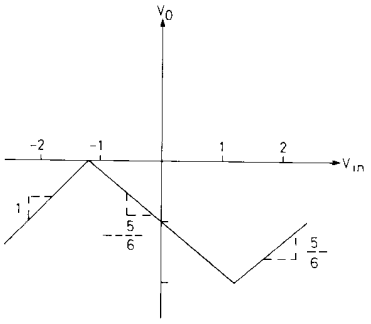
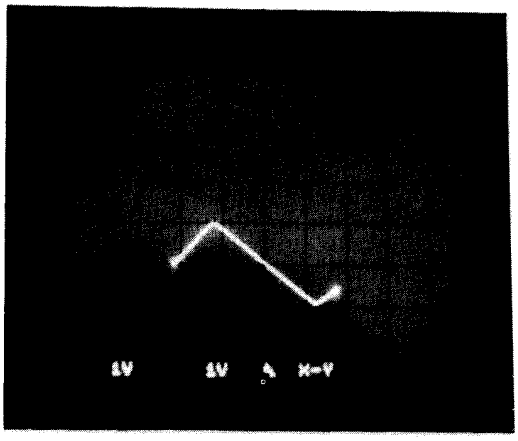


Fig. 15 *Experimental result of Fig. 14*
Upper trace (0.1 V/div) is input of root squarer
Lower trace (2 V/div) is output of root squarer
Horizontal scale 20 μs/div



a



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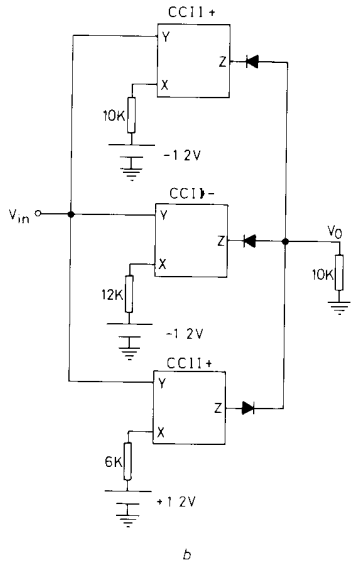

b

Fig. 16

a Example of piecewise-linear approximation function
b Circuit realisation using proposed voltage-mode limiters
c Experimental results of Fig. 16*b*
Horizontal and vertical scale are 1 V/div

division, amplitude modulation, squaring, etc. have also been demonstrated experimentally. To verify the feasibility, CCIIs implemented by bipolar transistors are used in experiments. It is to use the CMOS CCIIs [11] in MOS technology. A systematic study of the nonlinear signal processing circuits using CCIIs has been established. The results will facilitate the realisation of nonlinear circuits using CCIIs.

6 References

1 KUMAR, U.: 'Current conveyors: a review of the state of the art', *IEEE Circuits and Systems Mag.*, 1981, **3,** (1), pp. 10–13
2 WILSON, B.: 'Recent developments in current conveyors and current-mode circuits', *IEE Proc. G*, **137,** 1990, pp. 63–77
3 ALLEN, P.E., and TERRY, M.B.: 'The use of current amplifiers for high performance voltage applications', *IEEE J. Solid-State Circuits*, 1980, **SC-17,** pp. 155–162
4 WILSON, B.: 'Constant bandwidth voltage amplification using current conveyors', *Int. J. Electron.*, 1988, **65,** pp. 983–988
5 TOUMAZOU, C., LIDGEY, F.J., and CHEUNG, P.Y.K.: 'Current-mode analogue signal processing circuits — a review of recent developments'. Proc. IEEE ISCAS'89, pp. 1572–1575, 1989
6 BANU, M., and TSIVIDIS, Y.: 'An elliptic continuous-time CMOS filter with on-chip automatic tuning', *IEEE J. Solid-state Circuits*, 1985, **SC-20,** pp. 1114–1121
7 PARK, C.S., and SCHAUMANN, R.: 'Design of an eighth-order fully integrated CMOS 4 MHz continuous-time bandpass filter with digital/analog control of frequency and quality factor'. IEEE Proc. ISCAS'87, 1987, pp. 754–757
8 GEIGER, R.L., and SÁNCHENZ-SEINENCIO, E.: 'Active filter design using operational transconductance amplifiers: a tutorial', *IEEE Circuits and Systems Mag.*, 1985, **1,** pp. 20–32
9 SÁNCHENZ-SEINENCIO, E., RÁMIREZ-ANGULO, J., LINARES-BARRANCO, B., and RODRÍGUEZ-VÁZQUEZ, A.: 'Operational transconductance amplifier-based nonlinear function syntheses', *IEEE J. Solid-State Circuits*, 1989, **SC-24,** pp. 1576–1586
10 SHEN-IUAN LIU, HEN-WAI TSAO, and JINGSHOWN WU.: 'CCII-based continuous-time filters with reduced gain-bandwidh sensitivity', *Proc. IEE. G*, 1991, **138,** (2), pp. 210–216
11 BANU, M., and TSIVIDIS, Y.: 'Detailed analysis of nonlinearities in MOS fully integrated active RC filters based on balanced networks', *IEE Proc. G*, 1984, **131,** pp. 190–196
12 TOUMAZOU, C., and LIDGEY, F.J.: 'Wide-band precision rectification', *IEE. Proc. G*, 1987, **134,** p. 7–15
13 WADSWORTH, D.C.: *in* TOUMAZOU, C., LIDGEY, F.J., and HAIGH, D.G. (Eds.): 'Analogue IC design: the current mode approach' (Peter Peregrinus Ltd., London), Chap. 5, p. 535
14 WILSON, B.: 'High performance current conveyor implementation', *Electron. Lett.*, 1984, **20,** pp. 990–991