Magnetic-to-Digital Converters Using Single-Amplifier-Based Second-Order Delta-Sigma Modulators

Chien-Hung Kuo, Shr-Lung Chen, and Shen-Iuan Liu, Senior Member, IEEE

Abstract—In this paper, two magnetic-to-digital converters (MDCs) using single-amplifier-based second-order delta-sigma modulators (DSMs) are presented to detect the dc magnetic field. The proposed second-order DSM required only a single-operational amplifier to achieve the second-order noise shaping. Both the proposed circuits have been fabricated in a 0.5- μ m CMOS DPDM process, and the resolution of 11 bits can be achieved. The measured sensitivities are 1.486 and 0.459 mV/mT, and the minimum detectable magnetic fields are 0.6 mT and 0.4 mT for the MDC with and without the pre-amplifier, respectively. Both the measured nonlinearities are smaller than 1.3% within the range of \pm 100 mT.

Index Terms—CMOS, delta-sigma modulator (DSM), magnetic sensor.

I. INTRODUCTION

THERE IS A trend to convert magnetic fields into their corresponding electrical information to be helpful to human knowledge by using different kinds of magnetic sensors, such as Hall sensors, spinning current Hall sensors, and magnetic MOS-FETs (MAGFETs) [1]–[8]. The MAGFETs with two split drains can sense the perpendicular magnetic field to produce the corresponding current. Hence, it can be readily connected to the readout circuit to attain the electrical signal [3]. It is desired to integrate the sensor and signal processing circuits in a system to save power consumption and cost. The delta–sigma modulator (DSM) is an attractive candidate for the sensing applications due to its robust capability to process variations and high-resolution performance.

In order to have the minimum number of analog components for sensor applications, the first-order DSM is a good choice. Unfortunately, the first-order DSM will be sensitive to pattern noises and, therefore, it degrades the signal-to-noise ratio of the system. The second-order DSM can be insensitive to pattern noises. However, the required number of the amplifiers should be doubled. Obviously, there is a tradeoff between performance and circuit complexity.

Manuscript received January 28, 2003; revised September 11, 2003. The associate editor coordinating the review of this paper and approving it for publication was Dr. Andre Bossche.

- C.-H. Kuo is with the Department of Electrical Engineering, Tamkang University, Taipei, Taiwan 10617, R.O.C. (e-mail: chk@mail.tku.edu.tw).
- S.-L. Chen is with the University of California, Los Angeles, CA 90024 USA. S.-I. Liu is with the Department of Electrical Engineering, National Taiwan
- S.-I. Liu is with the Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan 10617, R.O.C., and also with the Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan 10617, R.O.C. (e-mail: lsi@cc.ee.ntu.edu.tw).

Digital Object Identifier 10.1109/JSEN.2004.823685

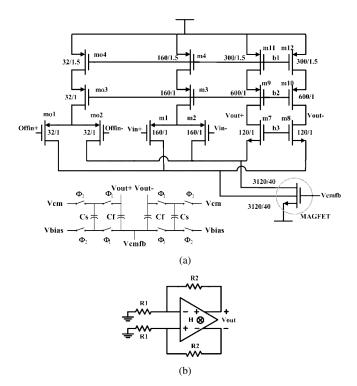


Fig. 1. (a) Proposed CMOS magnetooperational amplifier. (b) Magnetic preamplifier.

In this paper, a second-order DSM using single amplifier is proposed. Based on the proposed DSM, two magnetic-to-digital converters (MDCs) are also presented. This paper is organized as follows. In Section II, the proposed circuits are described. In Section III, experimental results are given. Finally, the conclusion is given in Section IV.

II. CIRCUIT DESCRIPTION

One of the proposed MDCs consists of a preamplifier using MAGFETs [3] and a second-order DSM using a single-operational amplifier. The circuit description will be given as follows.

A. Preamplifier Using a Magnetic Operational Amplifier (MOP)

The magnetic operational amplifier (MOP) [4], [5] is used a sensor to detect the dc magnetic field. Fig. 1(a) shows a MOP which can be realized by a folded-cascode operational amplifier except the NMOS current source pairs being replaced by MAGFETs [3]. The concept of the MOP is similar to that of a

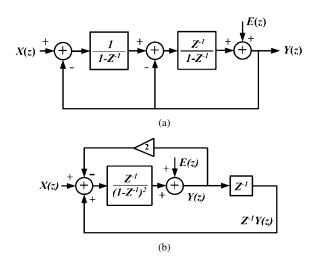


Fig. 2. (a) Linear model of a second-order DSM. (b) Linear model of a second-order DSM using a single-operational amp.

conventional operational amplifier. When no magnetic field is applied, the output currents on both drains of the MAGFET are equal. It means that the voltage difference between the differential outputs of the MOP is zero. When a perpendicular magnetic field H is applied, there will be the current imbalance between these two drains and the voltage difference between the differential outputs $V_{\mathrm{out+}}$ and $V_{\mathrm{out-}}$. Thus, a magnetic field induced voltage $v_m (= S_m \cdot H)$ could be added to the input of the MOP, where S_m denotes the conversion gain from the magnetic field to the induced voltage. So, the output voltage of the MOP can be expressed as follows:

$$V_{\text{out+}} - V_{\text{out-}} = A \cdot (V_{\text{in+}} - V_{\text{in-}} + v_m)$$
 (1)

where A is the finite dc gain of the operational amplifier. To improve the linearity and sensitivity the MOP is connected in an inverting amplifier with resistors R_1 and R_2 , as shown in Fig. 1(b). The output voltage can be expressed as

$$V_{\text{out}} = \left(1 + \frac{R_2}{R_1}\right) \cdot v_m. \tag{2}$$

B. Single-Amplifier-Based Second-Order DSM

Fig. 2(a) shows the linear model of a traditional second-order DSM, and its transfer function can be expressed as follows:

$$Y(z) = X(z) \cdot z^{-1} + E(z) \cdot (1 - z^{-1})^2 \tag{3}$$

where X(z) is the input signal, Y(z) is the modulator output, and E(z) is the quantization noise. By routine analysis, (3) can be modified as

$$Y(z) = X(z) \cdot \frac{z^{-1}}{(1 - z^{-1})^2} + \frac{z^{-1}}{(1 - z^{-1})^2} \cdot (-2 + z^{-1}) \cdot Y(z) + E(z).$$
 (4)

From (4), the linear system model can be redrawn as shown in Fig. 2(b). It can be found that this second-order DSM can be realized by single-operational amplifier using pseudo-2 path techniques [9] with proper clocking. Fig. 3 shows the implementation of the proposed second-order DSM using a single amplifier,

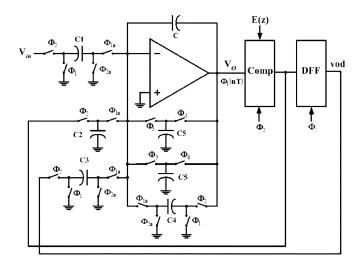


Fig. 3. Proposed second-order DSM with a single-operational amp.

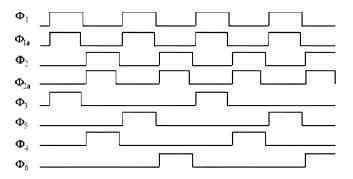


Fig. 4. Clock timing diagram.

where only the singled-end structure is given. It consists of a pseudo-2 path switched-capacitor integrator, a comparator, and a D-flip flop. The clock timing diagrams of the clocks are shown in Fig. 4. Φ_1 and Φ_2 are two major nonoverlapping clocks. With regard to the clock Φ_i (i = 1, 2), Φ_{ia} with the advanced falling edge is provided to avoid the signal dependent charge injection for switches. The remaining clocks $\Phi_3 \sim \Phi_6$ are generated to achieve the pseudo-2 path functions. Hence, the transfer function of Fig. 3 can be derived as follows:

$$V_{o}(z) = \frac{C_{1} \cdot z^{-1} \cdot V_{\text{in}}}{C - (C + C_{4}) \cdot z^{-1} + C_{5} \cdot z^{-2}} + \frac{z^{-1} \cdot (-C_{2} + C_{3} \cdot z^{-1}) \cdot V_{o}}{C - (C + C_{4}) \cdot z^{-1} + C_{5} \cdot z^{-2}} + E(z).$$
(5)

By taking that $C_1 = C_2/2 = C_3 = C_4 = C_5 = C$, (5) can realize a second-order DSM using single amplifier.

C. Proposed MDCs

The first MDC with the magnetic preamplifier is shown in Fig. 5. The clocks of the MDC are the same as those shown in Fig. 4. Assume that $C_2/2 = C_3 = C_4 = C_5 = C$. According to (1) and (5), the transfer function can be derived as

$$V_o(z) = v_m \cdot \left(1 + \frac{R_2}{R_1}\right) \cdot \left(\frac{C_1}{C}\right) \cdot z^{-1} + E(z) \cdot (1 - z^{-1})^2.$$
 (6)

Note that the quantization noise E(z) is second-orderly differentiated.

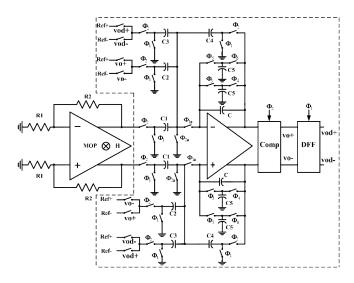


Fig. 5. Proposed MDC with the magnetic preamplifier.

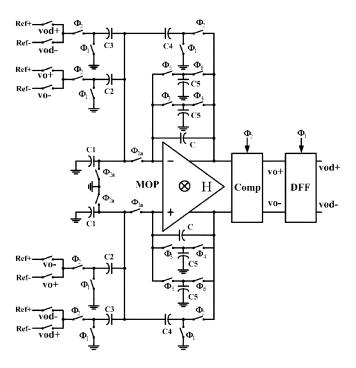


Fig. 6. Proposed MDC without the magnetic preamplifier.

The second MDC without the magnetic preamplifier with the same clocks as former one is shown in Fig. 6. Assume that $C_2/2 = C_3 = C_4 = C_5 = C$; the output transfer function can be

$$V_o(z) = v_m \cdot \left(\frac{C_1}{C} + 5\right) + E(z) \cdot (1 - z^{-1})^2. \tag{7}$$

D. Comparator

Since the performance of the DSM is unsusceptible to the nonlinearity of the comparator, the high-resolution comparator is unnecessary. The general regenerative latch comparator is employed as the qunatizer in the DSM.

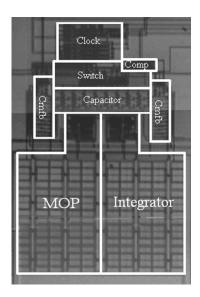


Fig. 7. Die photo of the proposed MDC with preamplifier.

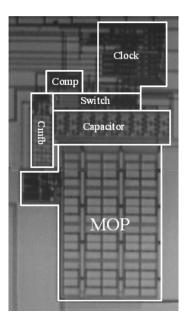


Fig. 8. Die photo of the proposed MDC without preamplifier.

III. EXPERIMENTAL RESULTS

Two MDCs based on the proposed second-order DSM have been fabricated in a standard 0.5 μ m DPDM CMOS process, and have been encapsulated in the same package. For the proposed MDC in Fig. 5, the off-chip resistors R_1 and R_2 are 1 k Ω and 220 k Ω , respectively, and the capacitor values are $C_1=3$ pF, $C_2=2$ pF, and $C_3=C_4=C_5=C=1$ pF. The die photograph of the MDC with the preamplifier is shown in Fig. 7. The circuit (without pads) occupies an area of 1.17 \times 1.65 mm. For the proposed MDC without the preamplifier, the capacitor values are the same as the former one except $C_1=220$ pF (off-chip). Fig. 8 shows the die photograph of the MDC without the preamplifier. The area of the circuit (without pad) is 0.84 \times 1.38 mm.

The magnitude and polarity of the magnetic field is controlled by using a GW regulated dc power supply (Model GPR-22H10H) to regulate proper current into an electromagnet

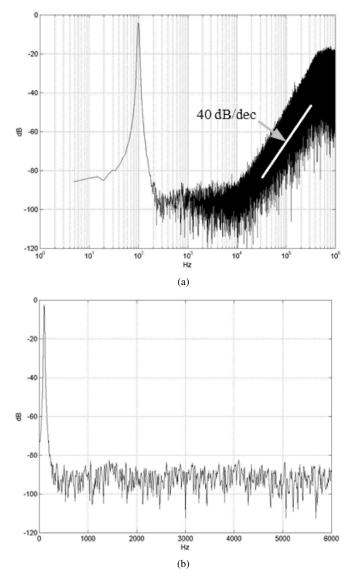


Fig. 9. (a) Measured output spectrum. (b) Expanded view of (a).

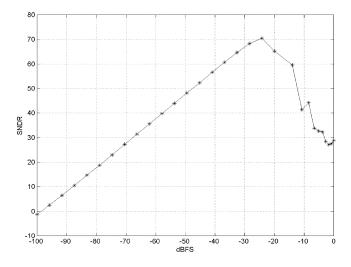
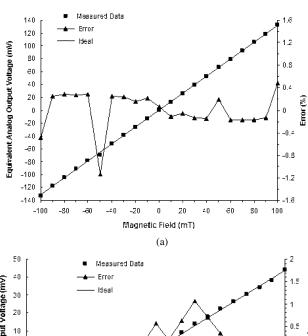


Fig. 10. SNDR versus input power.

core. The magnitude of the generated magnetic field is detected by the Gauss/Tesla meter (F.W. BELL model 5080) with a Hall



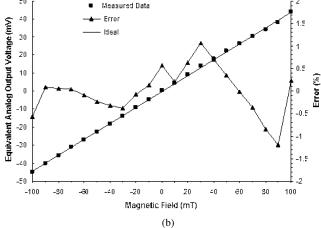


Fig. 11. (a) Equivalent analog output voltages and their corresponding errors versus magnetic fields for the MDC with preamplifier. (b) Equivalent analog output voltages and their corresponding errors versus magnetic fields for the MDC without preamplifier.

probe close to the test chip. To prevent the measurement results from interfering, these equipments and devices are caged into an iron shell. In addition, to attenuate the offset induced by the Earth, the Hall probe is shielded in the zero flux chamber of Gauss/Tesla meter before our measurement stage.

A 100-Hz sinusoidal input signal, which corresponds to the amplitude generated by a 50-mT magnetic field, is applied to the modulator. The positive and negative reference voltages are 5 and 0 V, respectively, and the digital output of 262 144 points under the sampling frequency of 2.5 MHz is recorded. By means of the numerical analysis, the output spectrum is plotted in Fig. 9(a). Fig. 9(b) is the expanded plot of Fig. 9(a). The noise floor near dc is roughly 90 dB after normalizing the peak signal power to 0 dB, and there is no evident tone in the signal band. From this figure, the second order noise-shaping is apparently valid because the slope of noise-shaping in higher band is 40 dB/dec. The measured SNDR versus input signal power for a sinusoid of 100 Hz is shown in Fig. 10. The modulator achieves a dynamic range of 75 dB and a peak SNDR of 70 dB within noise bandwidth of 1 kHz.

The proposed circuits have been characterized by applying a set of dc magnetic fields in the range of \pm 100 mT. The output digital codes are converted by a DAC into an analog output

| Work | Fig. 5 in this paper | Fig. 6 in this paper | Ref. [5] | Ref. [5] | Ref. [6] | Ref. [7] | Ref. [8] |
|-------------------|------------------------|------------------------|----------------------|----------------------|------------|-------------|---------------------------------|
| Technology | CMOS 0.5um | CMOS 0.5um | CMOS 0.5um | CMOS 0.5um | BiCMOS | CMOS 0.7um | CMOS 0.8um |
| Sensing Device | MAGFET | MAGFET | MAGFET | MAGFET | Hall Plate | MAGFET | Spinning Current Hall Device |
| Range | ±100mT | ±100mT | ±100mT | ±100mT | ±80mT | 0~800mT | ±200mT |
| Sensitivity | 1.486 mv/mT | 0.459 mv/mT | 1.327 mv/mT | 0.45 mv/mT | 25 mv/mT | 0.03 mv/mT | _ |
| System Offset | 0.6 mT | 0.4mT | 1 mT | 1 mT | _ | 0.2%(1.6mT) | _ |
| Resolution | 11 bits (50uT) | 11 bits (50uT) | 0.1mT | 0.1mT | 1mT | 6 bits | 12 bits (100uT) |
| Area | 1.9305 mm ² | 1.1592 mm ² | 1.87 mm ² | 0.888 mm^2 | _ | _ | _ |
| Power | 28.58 mW | 20.73 mW | 32.4 mW | 32.4 mW | _ | _ | _ |
| nonlinearity | <1.12 % | <1.3% | <3% | <3% | _ | _ | _ |

TABLE I
SOME RECENTLY PUBLISHED INTEGRATED MAGNETIC SENSOR SYSTEMS AND COMMERCIALLY AVAILABLE HALL MAGNETIC FIELD SENSORS

voltage. The reference voltage can be calculated From Fig. 10, which the peak SNDR is located at - 24.5 dBFS and it corresponds to an input of 297.2 mV. Fig. 11(a) and (b) show the equivalent analog output voltages for the MDC with and without the preamplifier, respectively. In these figures, each data point is obtained by averaging five measurement results, and, in each measurement, 65 536 points are sampled for analysis. For the MDC with the preamplifier, the sensitivity of 1.486 mV/mT is measured, and the resolution of 50 μ T can be achieved. The nonlinearity error is below 1.12% within the range of \pm 100 mT. The minimum detectable magnetic field is 0.6 mT, and the power consumption of the system is 28.58 mW at a 5-V supply voltage. For the MDC without the preamplifier, the measured sensitivity is 0.459 mV/mT, and the resolution of 50 μ T is achieved. The nonlinearity error is smaller than 1.3% within the range of \pm 100 mT. The minimum detectable magnetic field is 0.4 mT, and the power consumption of the system is 20.73 mW under a 5-V supply.

Taking into account the capacitor and resistor values in (6) and (7), the sensitivity of the MDC with the preamplifier should be 2.946 times as large as that of the MDC without the preamplifier. Our measurement result is 3.237. The discrepancy is caused by the parasitic capacitances shunted to ground when off-chip capacitor C_1 is added in the MDC without the preamplifier.

Comparisons with some published works are listed in Table I. The proposed MDCs using second-order DSMs can achieve better sensitivities, better linearity and smaller minimum detectable field compared to those in [5]. Obviously, the reduced area and power consumption of the MDC without preamplifier comes at the price of a smaller sensitivity. The degradation of the sensitivity is due to the absence of the gain stage in the architecture.

IV. CONCLUSION

In this paper, two MDCs using the proposed single-amplifier-based second-order DSM are presented. The proposed DSM is realized by using the pseudo-2 path technique to accomplish the second order noise-shaping. The measured sensitivities are $1.486~\rm mV/mT$ and $0.459~\rm mV/mT$ within the range of $\pm~100~\rm mT$ and the power consumptions are $28.58~\rm and~20.73~\rm mW$ for the MDC with and without the preamplifier, respectively.

ACKNOWLEDGMENT

The authors would like to thank the reviewers for their comments to improve this paper. They would also like to thank the National Science Council and Chip Implementation Center (CIC), Taiwan, for fabricating the chips.

REFERENCES

- [1] P. Ripka, "Magnetic sensors for industrial and field applications," *Sens. Actuators A*, vol. 41–42, pp. 394–397, 1994.
- [2] C. S. Roumenin, Solid State Magnetic Sensors. Amsterdam, The Netherlands: Elsevier, 1994.
- [3] H. P. Baltes and R. S. Popovic, "Integrated semiconductor magnetic field sensors," *Proc. IEEE*, vol. 74, pp. 1107–1132, Aug. 1986.
- [4] K. Maenaka, H. Okada, and T. Nakamura, "Universal magneto-operational amplifier (MOP)," Sens. Actuators A, vol. 21–23, pp. 807–811, 1990.
- [5] C. H. Kuo, S. L. Chen, L. A. Ho, and S. I. Liu, "CMOS oversampling $\Delta\Sigma$ magnetic to digital converters," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1582–1586, Oct. 2001.
- [6] Datasheet of A3516: "Ratiometric Linear Hall-Effect Sensor for High-Temperature Operation" [Online]. Available: http://www.alle-gromicro.com/
- [7] C. Rubio, S. Bota, J. G. Macias, and J. Samitier, "Monolithic integrated magnetic sensor in a digital CMOS technology using a switched current interface system," in *Proc. 17th IEEE Instrumentation Measurement Technology Conf.*, vol. 1, 2000, pp. 69–73.
- [8] P. Malcovati and F. Maloberti, "An integrated microsystem for 3-D magnetic field measurements," *IEEE Trans. Instrum. Meas.*, vol. 49, pp. 341–345, Apr. 2000.
- [9] T. H. Hsu and G. C. Temes, "An improved circuit for pseudo-N-path switched-capacitor filters," *IEEE Trans. Circuits Syst.*, vol. CAS-32, pp. 1071–1073, Oct. 1985.



Chien-Hung Kuo was born in Taipei, Taiwan, R.O.C., on April 1, 1965, He received the B.S. degree in electrical engineering from Feng Chia University, Taiwan, in 1987 and the M.S. and Ph.D. degrees in electrical engineering from the National Taiwan University, Taipei, in 1992 and 2003, respectively.

From 1993 to 2003, he was a Lecturer at Kuang Wu Institute of Technology, Taiwan. He has been an Assistant Professor with the Department of Electronic Engineering, Tamkang University, Taipei, since Au-

gust 2003. His research is directed toward the design of the analog-to-digital converter.

^{*} Note: "-" indicates not mentioned



Shr-Lung Chen was born in Taipei, Taiwan, R.O.C., on November 8, 1976. He received the B.S. and M.S. degrees in electrical engineering from the National Taiwan University, Taipei, in 1999 and 2001, respectively. He is currently pursuing the Ph.D. degree at the University of California, Los Angeles.

His previous research focus was on magnetic sensor-actuator systems and delta- sigma ADCs. His current research interests are in high-speed ADC-DAC and RF interconnect.



Shen-Iuan Liu (S'88–M'93–SM'03) was born in Keelung, Taiwan, R.O.C., on April 4, 1965. He received the B.S. and Ph.D. degrees in electrical engineering from the National Taiwan University (NTU), Taipei, in 1987 and 1991, respectively.

From 1991 to 1993, he served as a Second Lieutenant in the Chinese Air Force. From 1991 to 1994, he was an Associate Professor with the Department of Electronic Engineering, National Taiwan Institute of Technology. He joined in the Department of Electrical Engineering, NTU, in 1994, and he has been a

Professor since 1998. His research interests are in analog and digital integrated circuits and systems.