National Taiwan University
Department of Electrical Engineering
Introduction to Electronic Design Automation, Spring 2006

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Handout #4
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Homework #2 (due April 25, 2006 in-class)

1. (13 pts) Given the following Polish expression, $E = 12H3V4HV5$.

   (a) (2 pts) Dose the above expression satisfy the balloting property? Justify your answer.

   (b) (2 pts) Is E a normalized Polish expression? If not, exchange an operator and its adjacent operand to transform E into a normalized Polish expression E'.

   (c) (3 pts) Give the slicing tree corresponding to the expression E, or explain why no such a slicing tree exists. Also, give the slicing tree corresponding to the "resulting" normalized Polish expression E', if E is not a normalized Polish expression.

   (d) (6 pts) Assume the modules 1, 2, ..., 5 have the sizes and shapes indicated in Table 1. If all modules are hard and have free orientations, what will be the size of the smallest bounding rectangle corresponding to E if it is a normalized Polish expression or E' otherwise? **Show all steps that lead to your answer.**

Module No.	Width	Height
1	3	1
2	2	2
3	4	3
4	3	1
5	5	5

Figure 1: Table 1.

2. (8 pts) Derive the B*-tree for the the packing of the five modules, $a, b, c, d,$ and e shown in Figure 2. Show all steps for computing the coordinates of the modules from the resulting B*-tree?
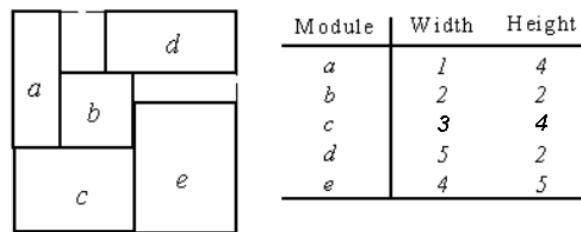

Module	Width	Height
a	1	4
b	2	2
c	3	4
d	5	2
e	4	5

Figure 2: A packing for the five modules $a, b, c, d,$ and e.

3. (8 pts) For the floorplanning problem discussed in class (and programming assignment #1), we were asked to minimize the area of the final bounding rectangle for the given set of hard blocks. Suppose we need to pack a set of hard blocks into a die with a **fixed** bounding rectangle (i.e., fixed-outline floorplanning). Discuss how you can modify the cost function of floorplanning to address the fixed-outline floorplanning.

4. (10 pts) Let the three tuple (u, v, w) denotes an edge (u, v) with weight w. Given a circuit C of 6 vertices, $n_1, n_2, \ldots, n_6$, and 5 edges, $C = \{(n_1, n_4, 4), (n_4, n_2, 2), (n_2, n_3, 3), (n_2, n_5, 5), (n_3, n_6, 6)\}$, apply the Kernighan-Lin heuristic to find the balanced min-cut for C with the initial partitions $\{n_1, n_2, n_3\}$ and $\{n_4, n_5, n_6\}$. **Show all steps that lead to your answer.**

5. (10 pts) Refer to the circuit shown in Figure 3(a). The I/O structure of a single EXOR gate is shown Figure 3(b) (and (c)); here, A and B are inputs and C is the output.

The problem is to assign the EXOR gates to the logic blocks of a 5×3 gate array with the channel capacity of 2 such that the total wire length is minimized. For the purpose of wire length computation, assume that the 15 logic blocks of the gate array are located at coordinates $(2i, 2j), 0 \le i \le 4, 0 \le j \le 2$, and that the wire length inside a logic block is negligible.

   (a) Show a gate assignment and sketch the wiring plan for each net by using the I/O structure depicted in Figure 3(b). What is the total wire length? Note that inputs and outputs are available on both sides of the module (e.g., pin A on the left-hand side is internally shorted to the pin A on the right-hand side).

   (b) Repeat the above problem by using the I/O structure depicted in Figure 3(c). Here inputs and outputs are available on all sides of the logic block.
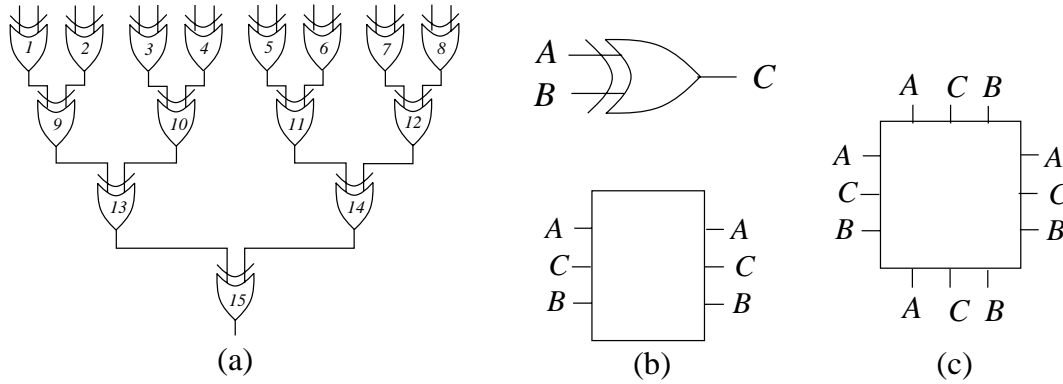

(a)   (b)   (c)

Figure 3: (a) A circuit with 15 EXOR gates. (b)(c) The I/O interface of a 2-input EXOR cell.

6. (9 pts) For the four pins shown in Figure 4, give the wire length estimation for the following methods:

   (a) Semi-perimeter approximation
   (b) Minimum rectilinear Steiner tree
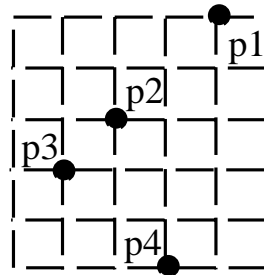   (c) Minimum rectilinear spanning tree

Figure 4: A placement with four pins.

7. (10 pts) Maze routing.

   (a) For the Soukup maze router, there is no guarantee that we can find the **shortest** path if such a path exists. Give an example routing configuration for the situation.

   (b) For the Hightower line-search router, there is no guarantee that we can find **a** path if such a path exists. Give an example routing configuration for the situation.

8. (16 pts) Given the instance of the channel routing problem shown in Figure 5.

   (a) (2 pts) What is the channel density? Find the set of nets that contribute the channel density.

   (b) (2 pts) Draw the HCG and VCG.

   (c) (4 pts) Can the basic left-edge algorithm apply to this channel routing instance? Route the instance if Figure 5 gives a feasible routing instance; explain why the algorithm does not apply to this instance, otherwise.

   (d) (4 pts) Can the constrained left-edge algorithm apply to this channel routing instance? Route the instance if Figure 5 gives a feasible routing instance; explain why the algorithm does not apply to this instance, otherwise.

   (e) (4 pts) Can the dogleg channel router apply to this channel routing instance? Route the instance if Figure 5 gives a feasible routing instance; explain why the algorithm does not apply to this instance, otherwise.
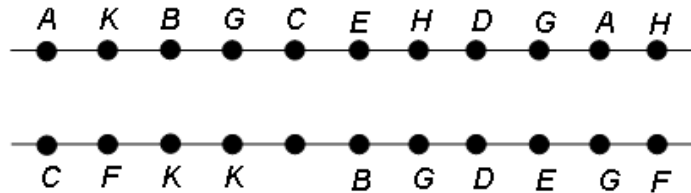

Figure 5: A channel routing instance.

9. (8 pts) Apply the robust channel router to route the instance shown in Figure 6.
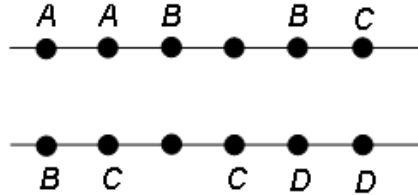

Figure 6: A channel routing instance.

10. (8 pts) Given a netlist $N = \{[(1,1),(2,2)], [(2,10),(2,14)], [(6,2),(10,10)], [(6,10),(10,14)], [(10,2),(14,2)]\}$, where $[(p,q),(r,s)]$ denotes a route from the coordinate (p,q) to (r,s), you are ask to apply a 3-level routing (multilevel routing with three levels) to route the instance N on a 16×16 chip plane. Suppose only straight and L-shaped routes are allowed during the coarsening stage while maze routing is applied during uncoarsening. Also, all wire spacing (including point-to-wire spacing) must be at least 4 units. Show how you obtain the routing solution **step by step**.