Power IC

Design and Simulation Tool Setup

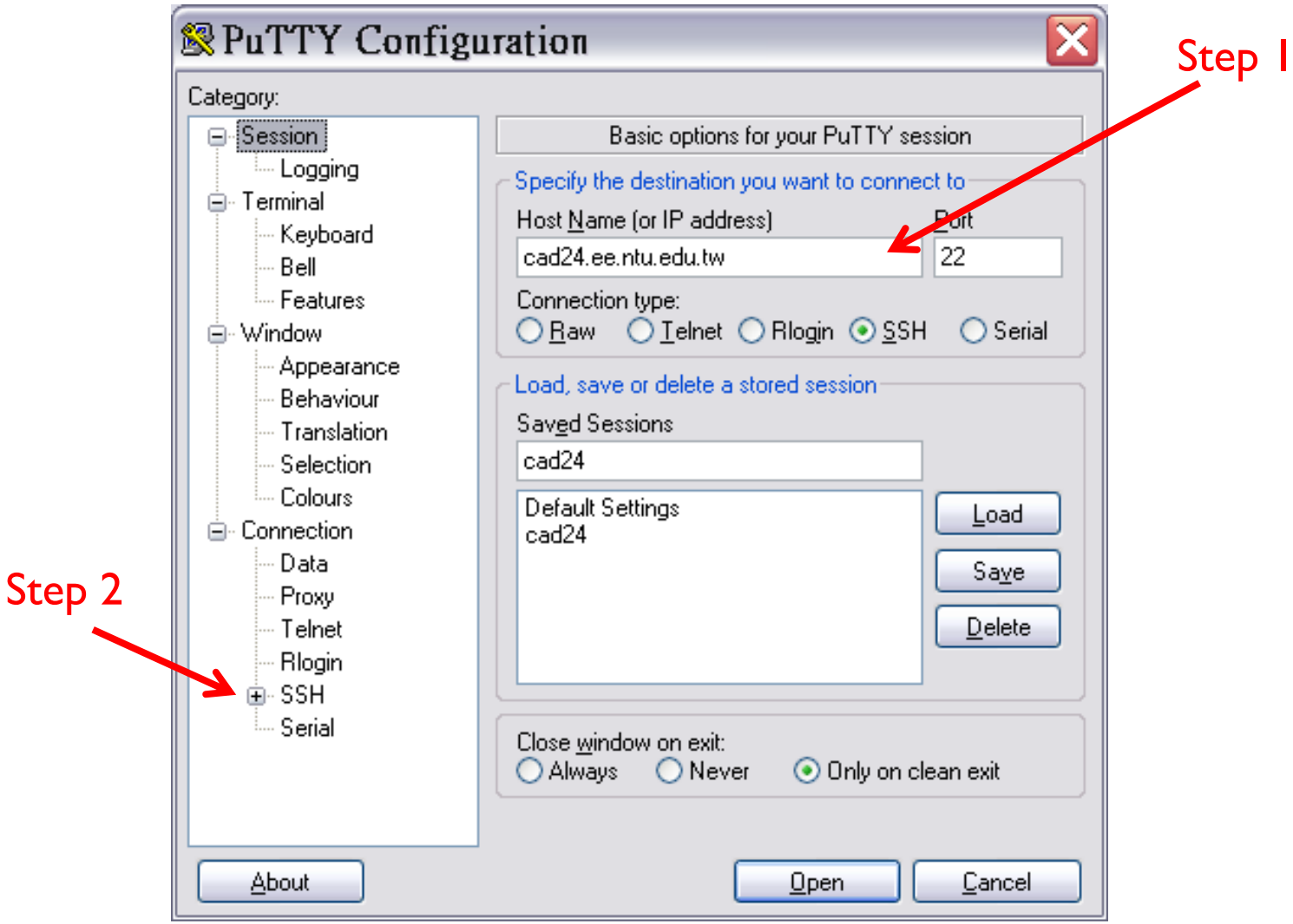
outline

- Welcome to IC Design Lab
- Hspice
- Cadence IC

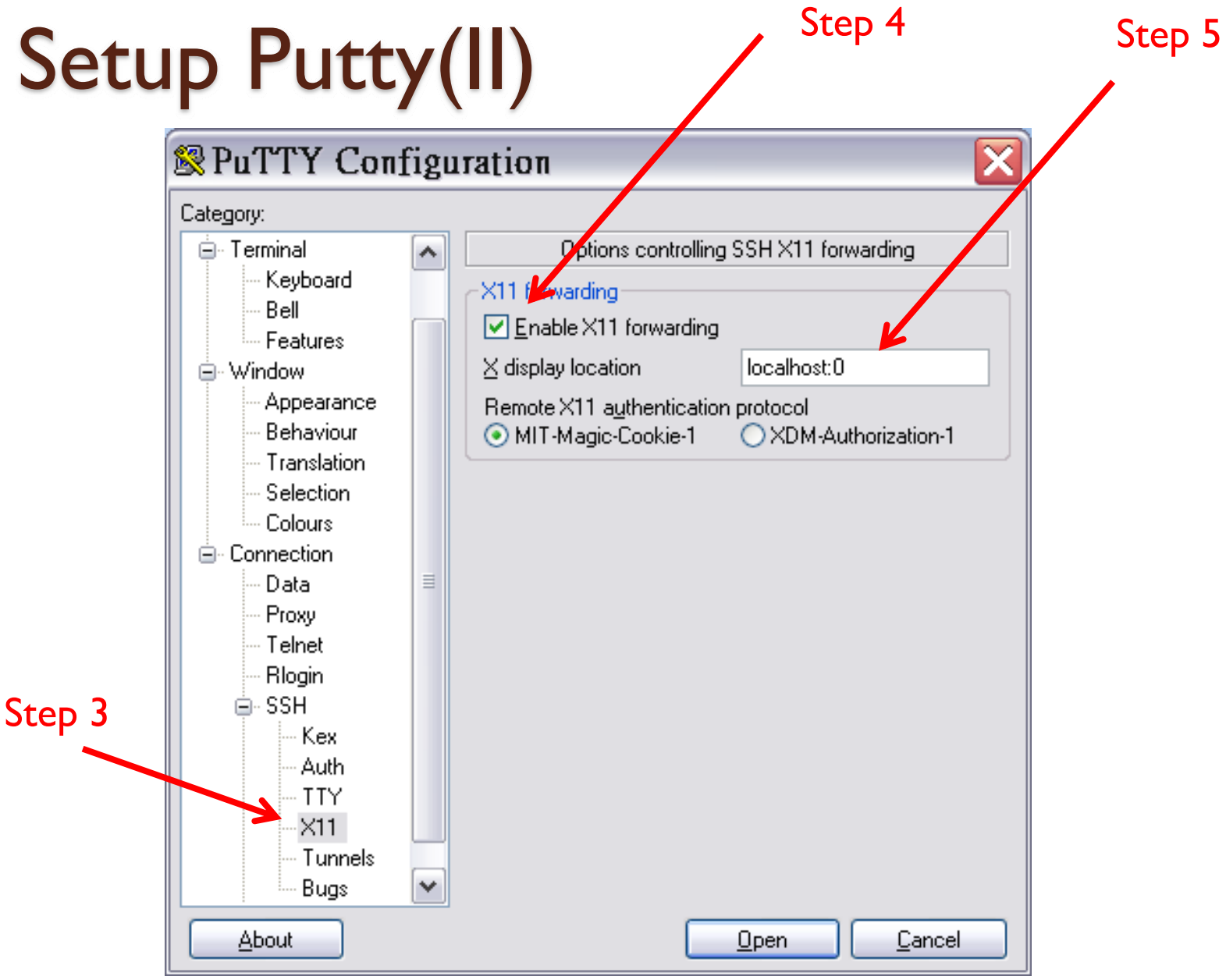
Welcome to IC Design Lab

- Lab 231
- http://cad.ee.ntu.edu.tw
- Create an account
- Setup Putty
- X-win
- Setup the design tool environment

Setup Putty(I)



Setup Putty(II)

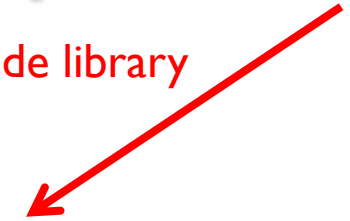


Hspice

- Tool setup
  - Hspice simulater
  - AvanWaves Debugger
  - Source /usr/cad/synopsys/CIC/hspice.csh

- Include .18 Virtual Library
  - Virtual Library path /home/raid1_1/cic/Virtual_018_CMOS/model/
    - .lib './cic018.l' tt
  - 0.18um CMOS design kit
    - .lib './rf018.l' tt

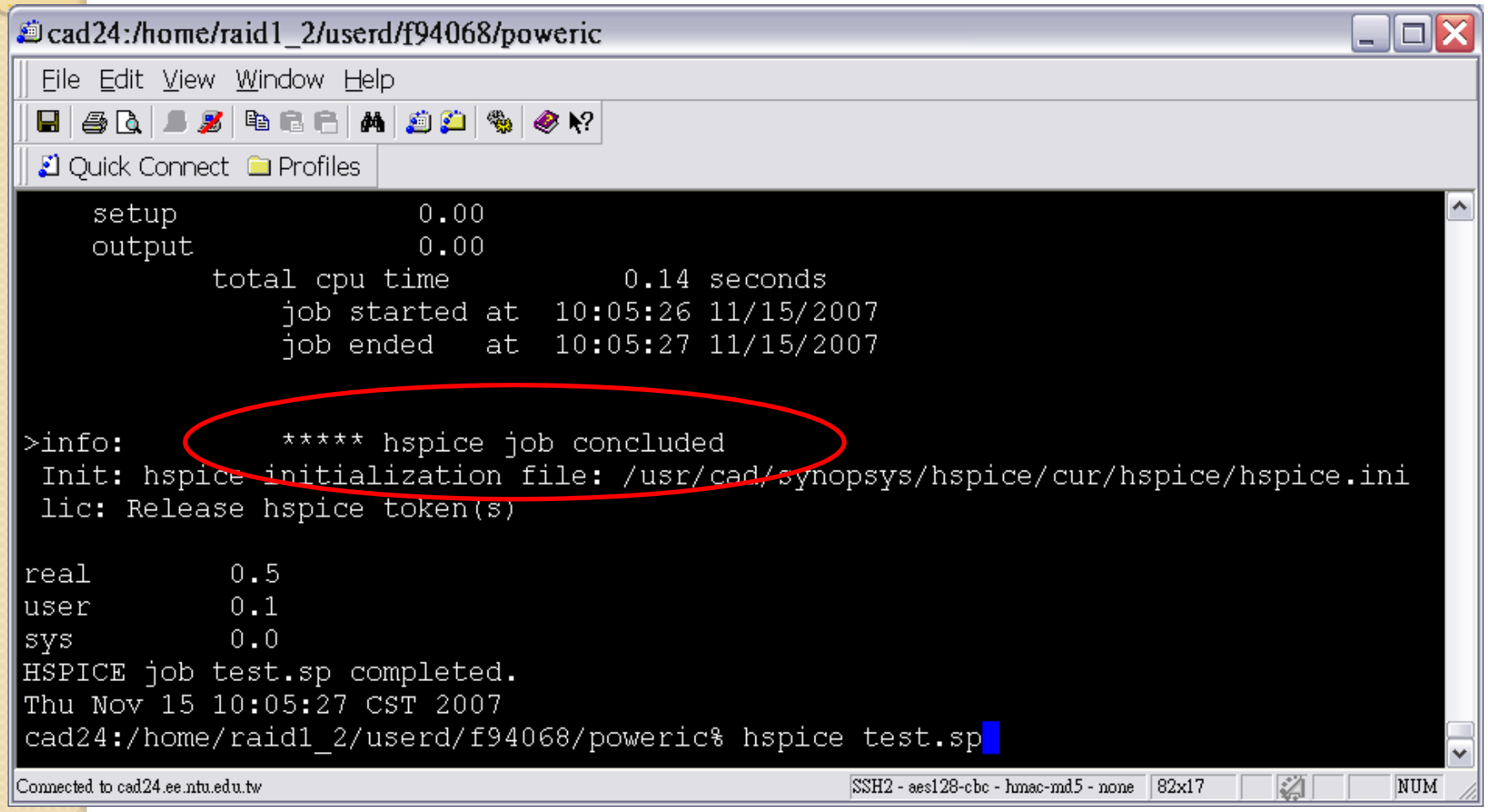
Hspice – simple example




```
*inverter

.protect
.lib '/home/raid1_1/cic/Virtual_018_CMOS/model/cic018.l' tt
.unprotect

Mn vout vin 0   0   N_18 w=1u l=1u m=1
Mp vout vin VDD VDD P_18 w=1u l=1u m=1

Vdd VDD 0 PWL (0 0 10U 1.8V)
VIN VIN 0 PULSE(0 1.8 0 10N 10N 10U 20U)

.TRAN 10N 100U
.op
.option post
.END
```

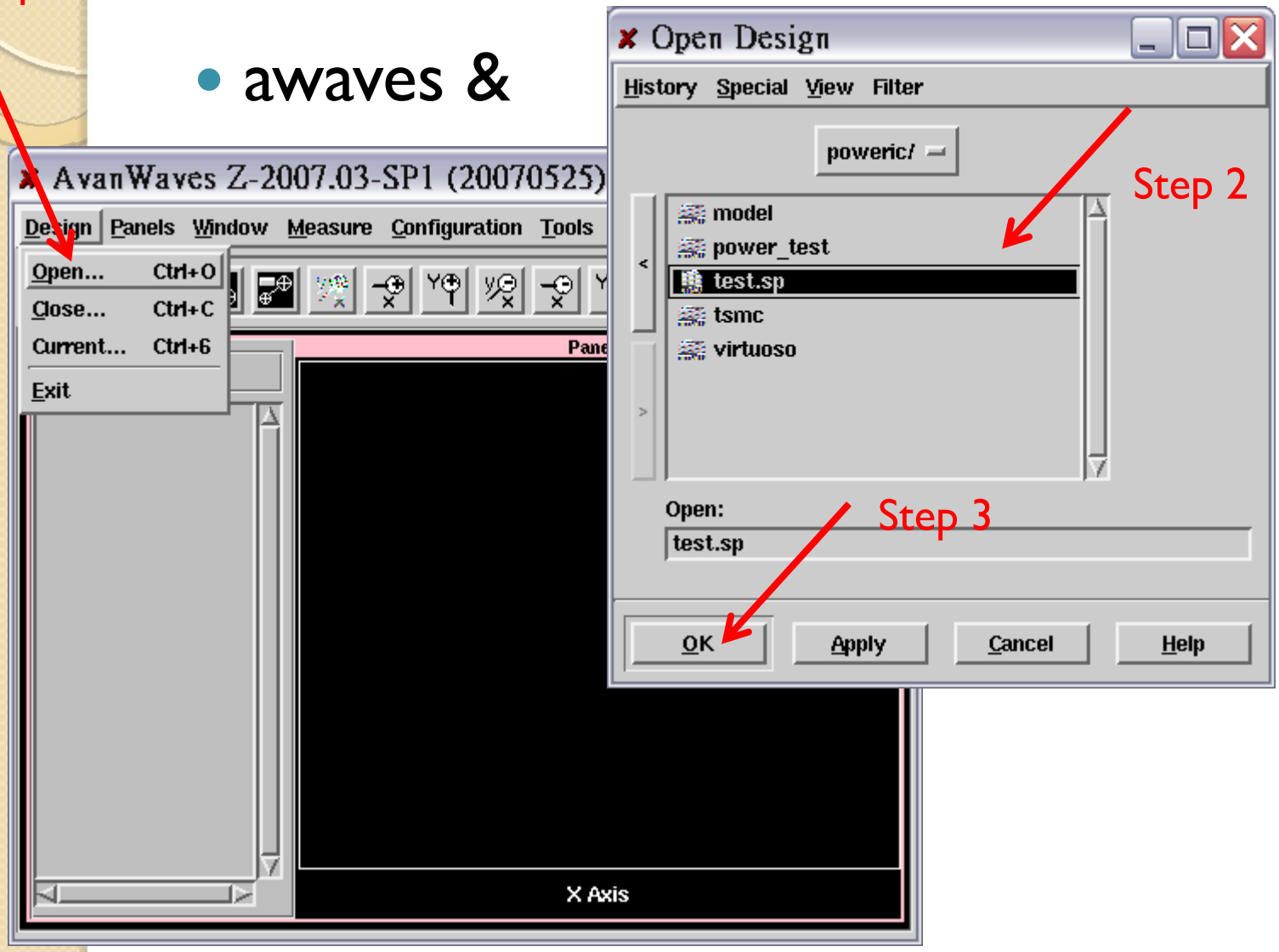
Run - Simulation

- hspice xxx.sp

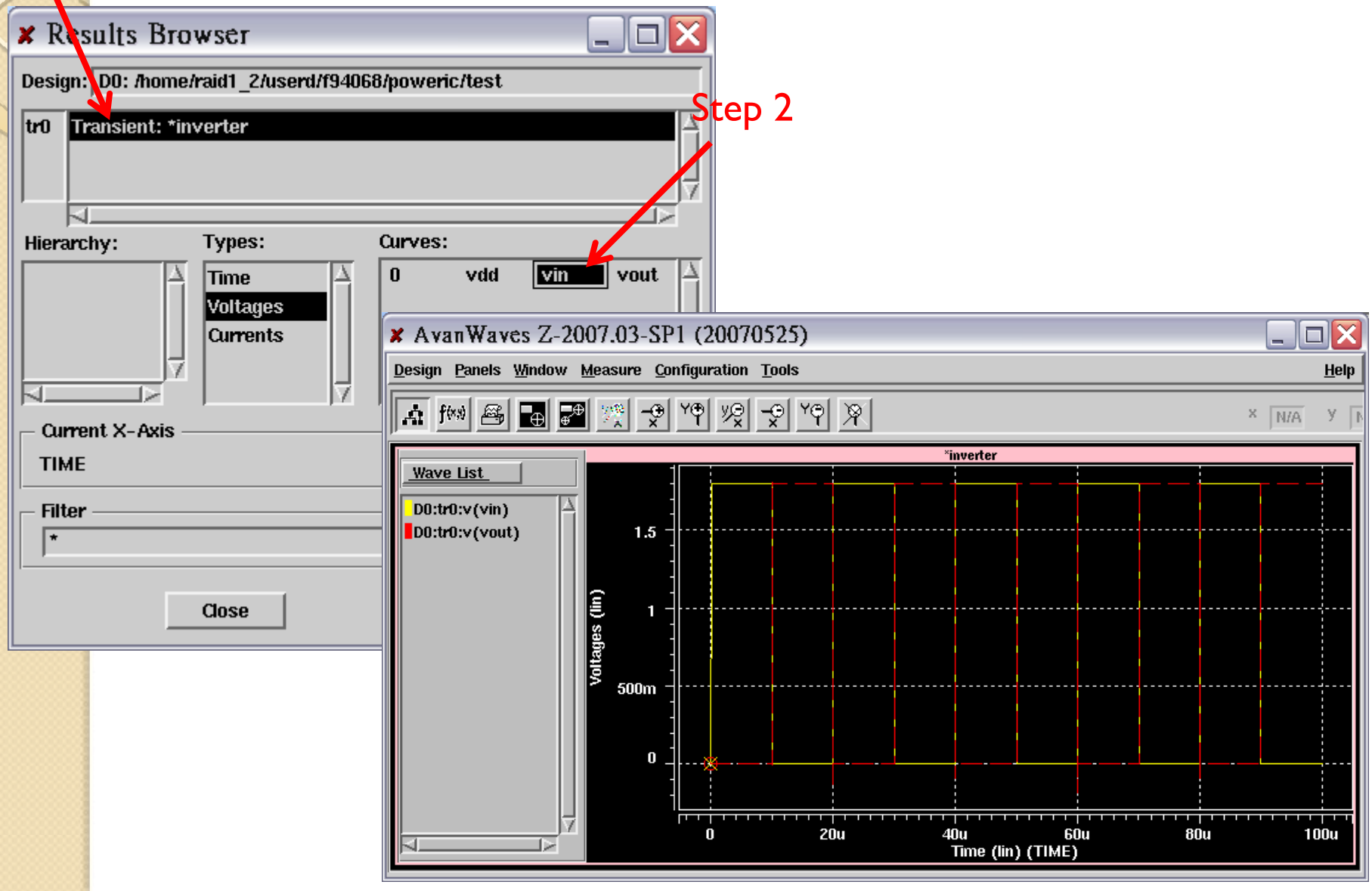


Run - Debug

- awaves &



Run - Debug

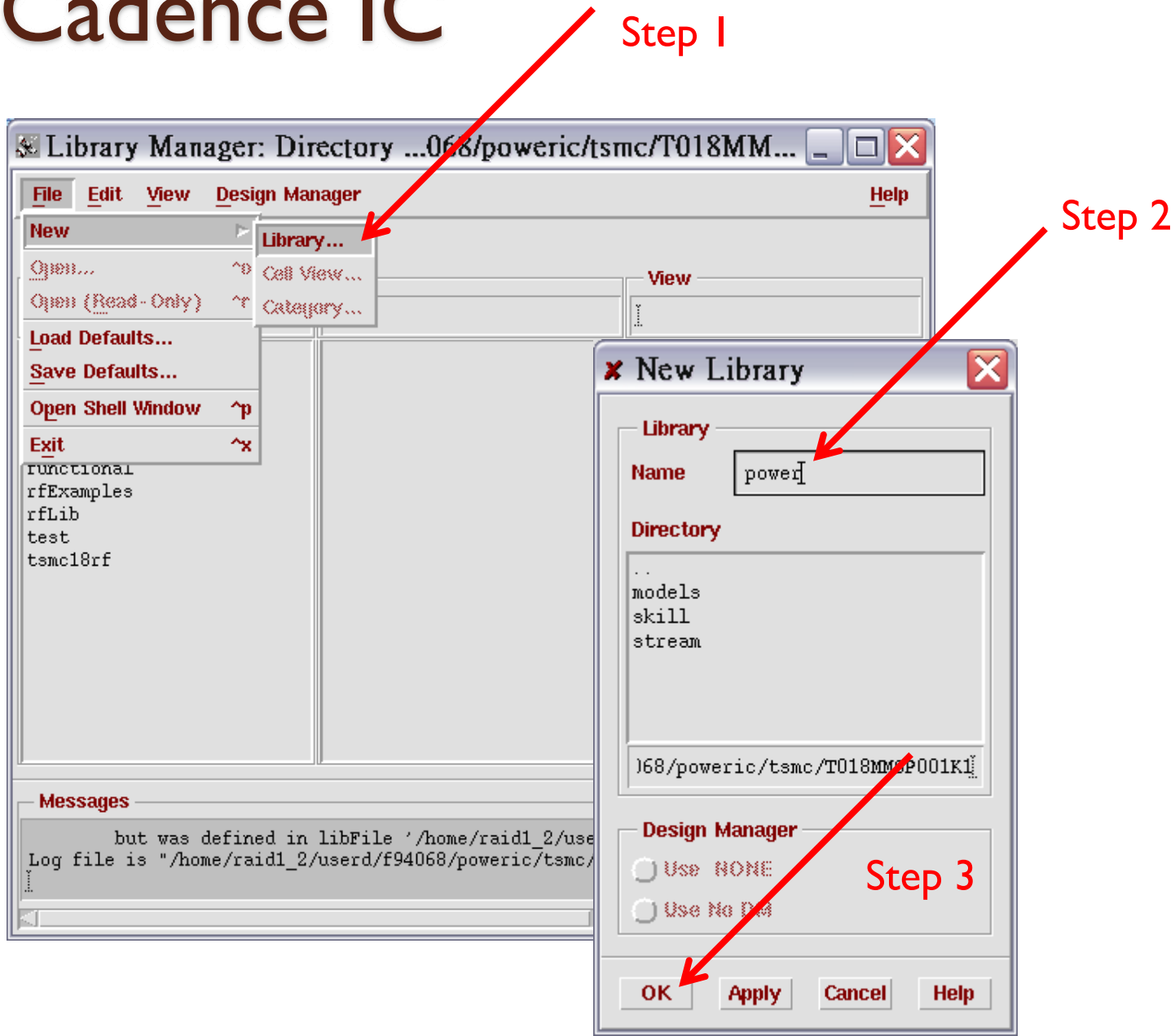

Step 1
Step 2
Results Browser
Design: D0: /home/raid1_2/userd/f94068/poweric/test
tr0
Transient: *inverter
Hierarchy:
Types:
Time
Voltages
Currents
Curves:
0
vdd
vin
vout
Current X-Axis
TIME
Filter
*
Close
AvanWaves Z-2007.03-SP1 (20070525)
Design Panels Window Measure Configuration Tools Help
Wave List
D0:tr0:v(vin)
D0:tr0:v(vout)
*inverter
Voltages (lin)
1.5
1
500m
0
0
20u
40u
60u
80u
100u
Time (lin) (TIME)

Cadence IC

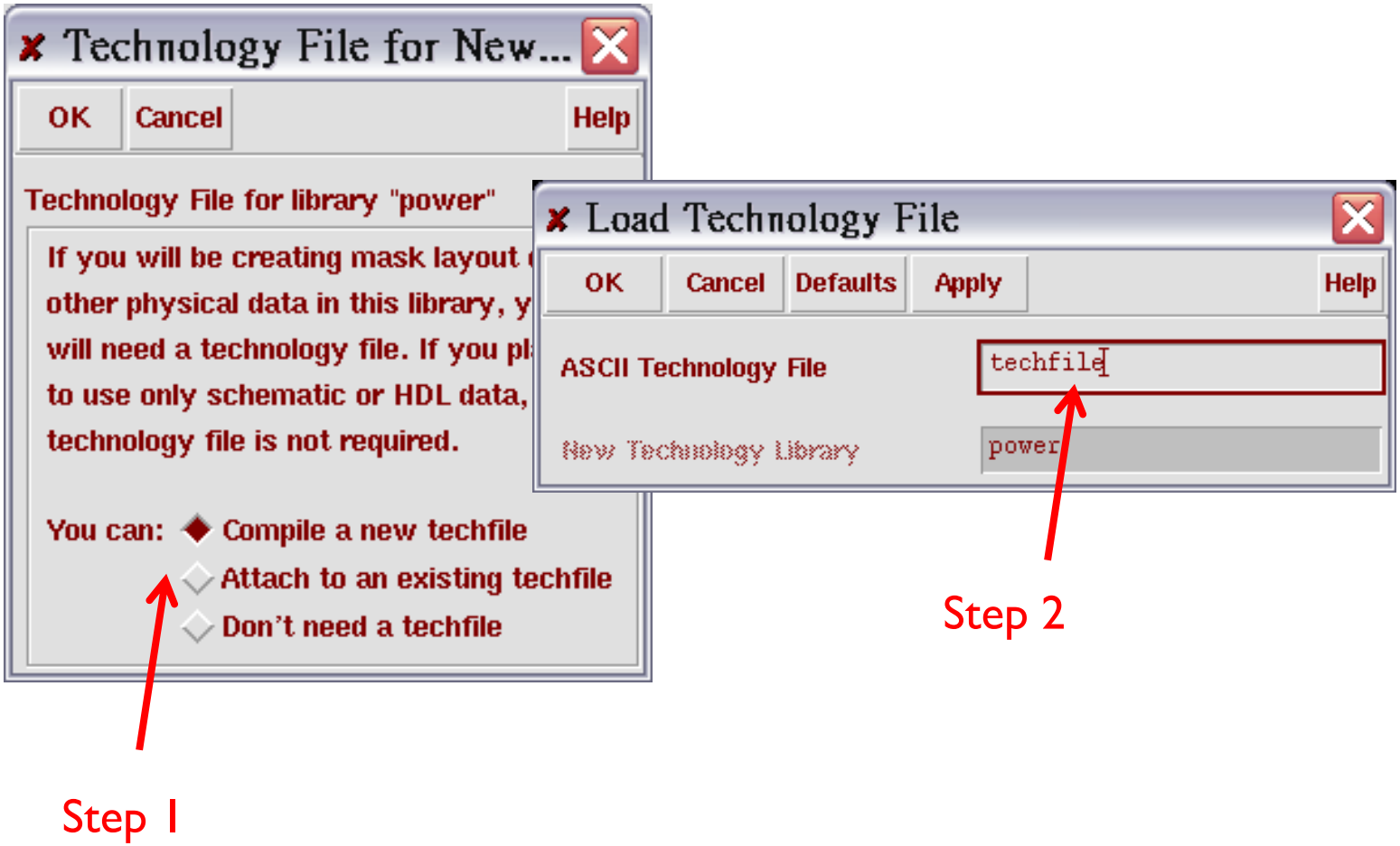
- Tool setup
  - Source /usr/cadence/IC/CIC/ic.csh
- 0.18um CMOS design kit

- icfb &

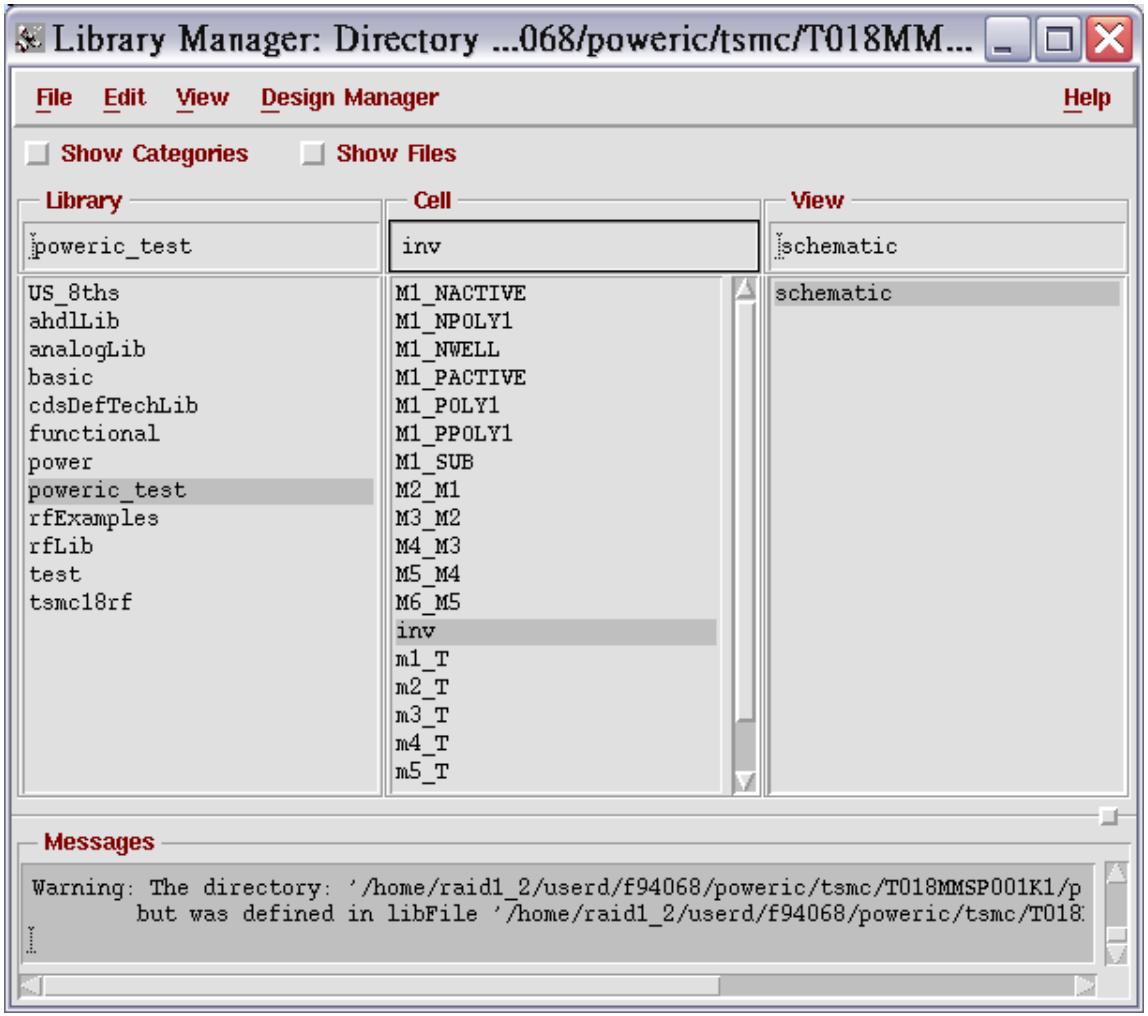
Cadence IC


Step 1
Step 2
Step 3
Library Manager: Directory ...068/poweric/tsmc/T018MM...
File
Edit
View
Design Manager
Help
New
Library...
Cell View...
Category...
Open...
Open (Read-Only)
Load Defaults...
Save Defaults...
Open Shell Window ^p
Exit ^x
functional
rfExamples
rfLib
test
tsmc18rf
View
Messages
but was defined in libFile '/home/raid1_2/use
Log file is "/home/raid1_2/userd/f94068/poweric/tsmc/
New Library
Library
Name
power
Directory
..
models
skill
stream
)68/poweric/tsmc/T018MM
P001K1
Design Manager
Use NONE
Use No DM
OK
Apply
Cancel
Help

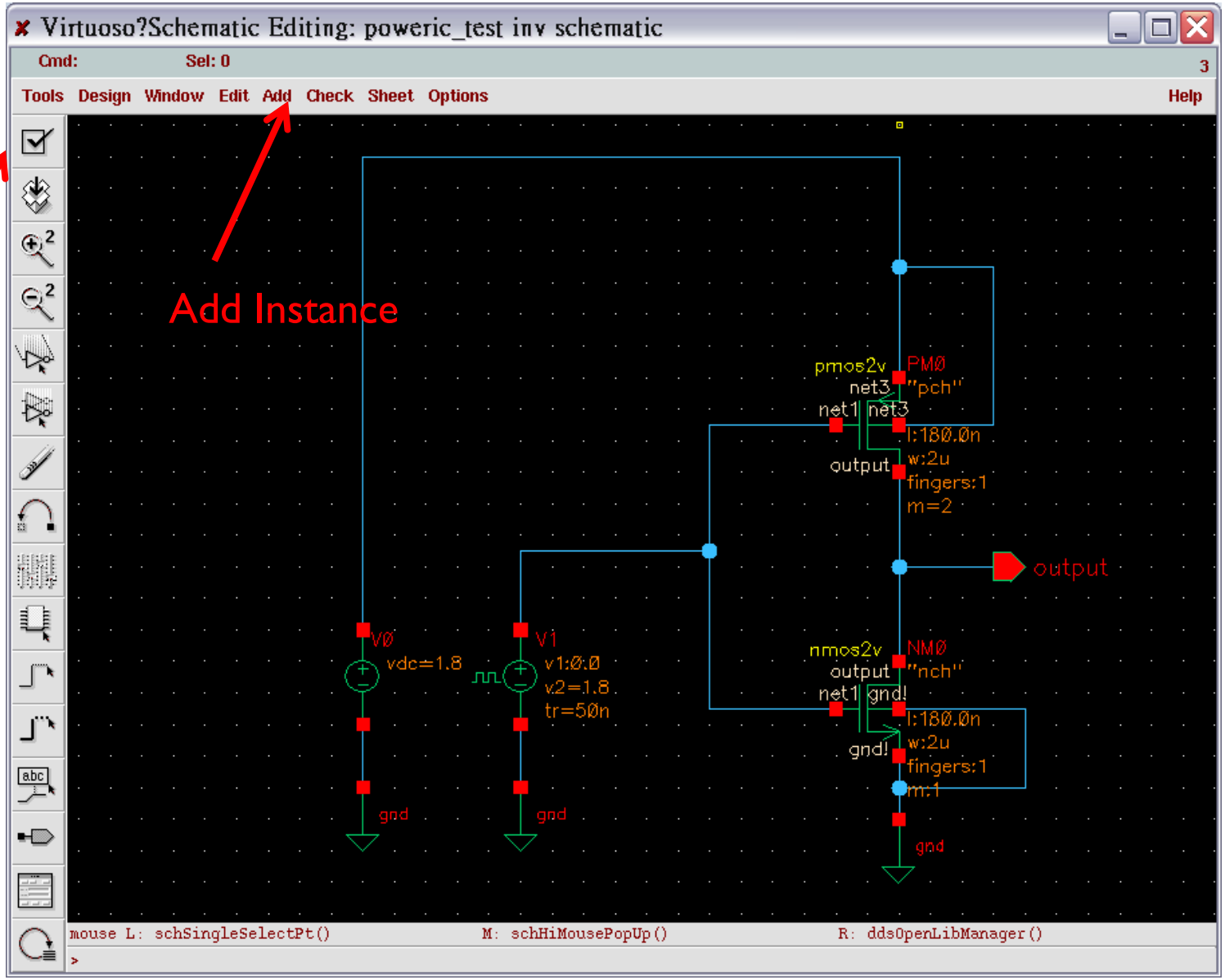
Cadence IC


Technology File for New...
OK
Cancel
Help
Technology File for library "power"
If you will be creating mask layout
other physical data in this library, y
will need a technology file. If you pl
to use only schematic or HDL data,
technology file is not required.
You can:
Compile a new techfile
Attach to an existing techfile
Don't need a techfile
Load Technology File
OK
Cancel
Defaults
Apply
Help
ASCII Technology File
techfile
New Technology Library
power
Step 1
Step 2

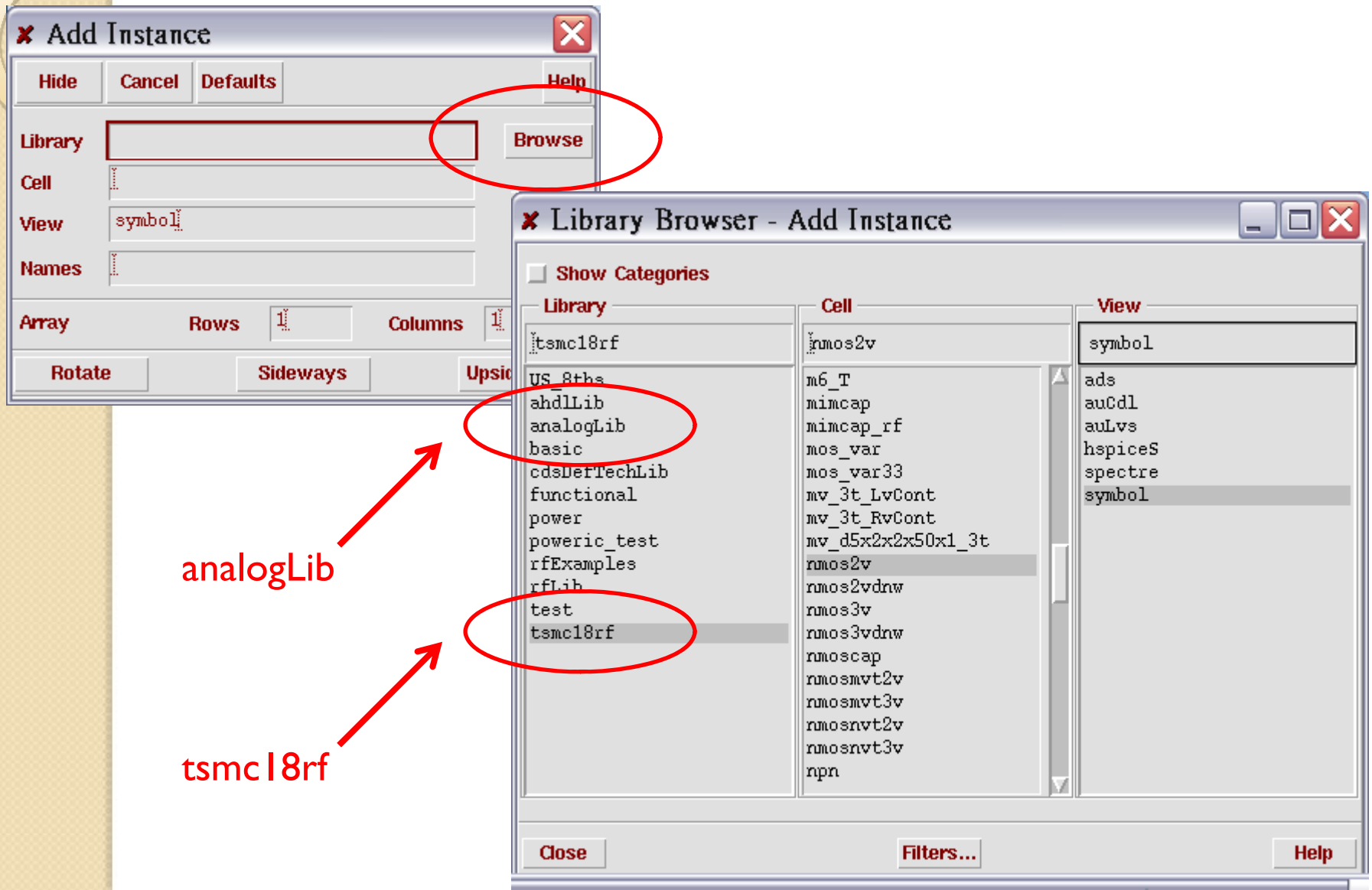
Cadence IC


Library Manager: Directory ...068/poweric/tsmc/T018MM...
File
Edit
View
Design Manager
Help
Show Categories
Show Files
Library
Cell
View
poweric_test
inv
schematic
US_8ths
ahdlLib
analogLib
basic
cdsDefTechLib
functional
power
poweric_test
rfExamples
rfLib
test
tsmc18rf
M1_NACTIVE
M1_NPOLY1
M1_NWELL
M1_PACTIVE
M1_POLY1
M1_PPOLY1
M1_SUB
M2_M1
M3_M2
M4_M3
M5_M4
M6_M5
inv
m1_T
m2_T
m3_T
m4_T
m5_T
schematic
Messages
Warning: The directory: '/home/raid1_2/userd/f94068/poweric/tsmc/T018MMSP001K1/p
but was defined in libFile '/home/raid1_2/userd/f94068/poweric/tsmc/T018

Cadence IC

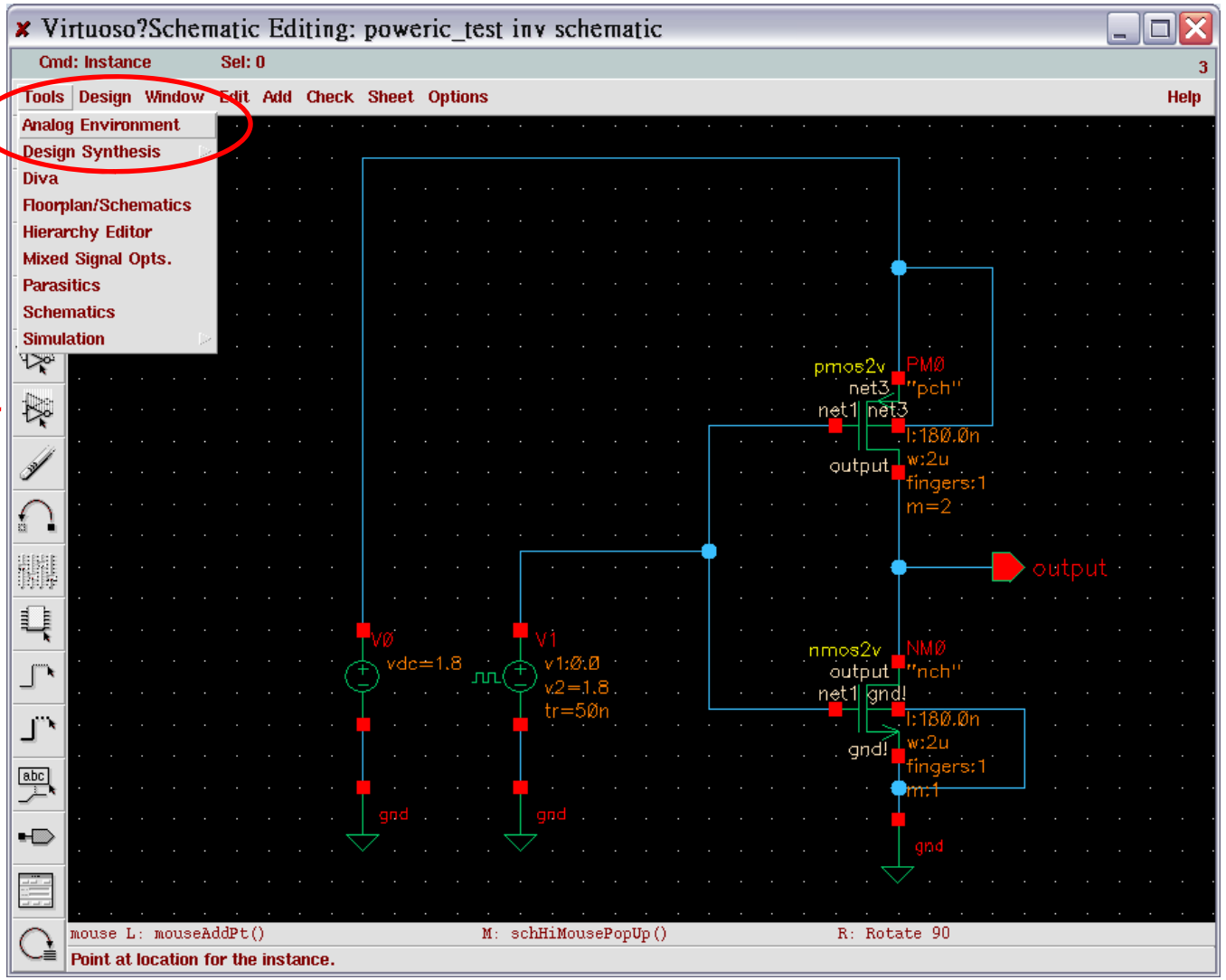

Virtuoso?Schematic Editing: poweric_test inv schematic
Cmd:
Sel: 0
3
Tools Design Window Edit Add Check Sheet Options
Help
Add Instance
Design check
pmos2v
PM0
"pch"
net3
net1
net3
l:180.0n
output
w:2u
fingers:1
m=2
output
V0
vdc=1.8
V1
v1:0:0
v2=1.8
tr=50n
nmos2v
NM0
"nch"
output
net1
gnd!
l:180.0n
gnd!
w:2u
fingers:1
m:1
gnd
gnd
gnd
mouse L: schSingleSelectPt()
M: schHiMousePopUp()
R: ddsOpenLibManager()
>

Cadence IC

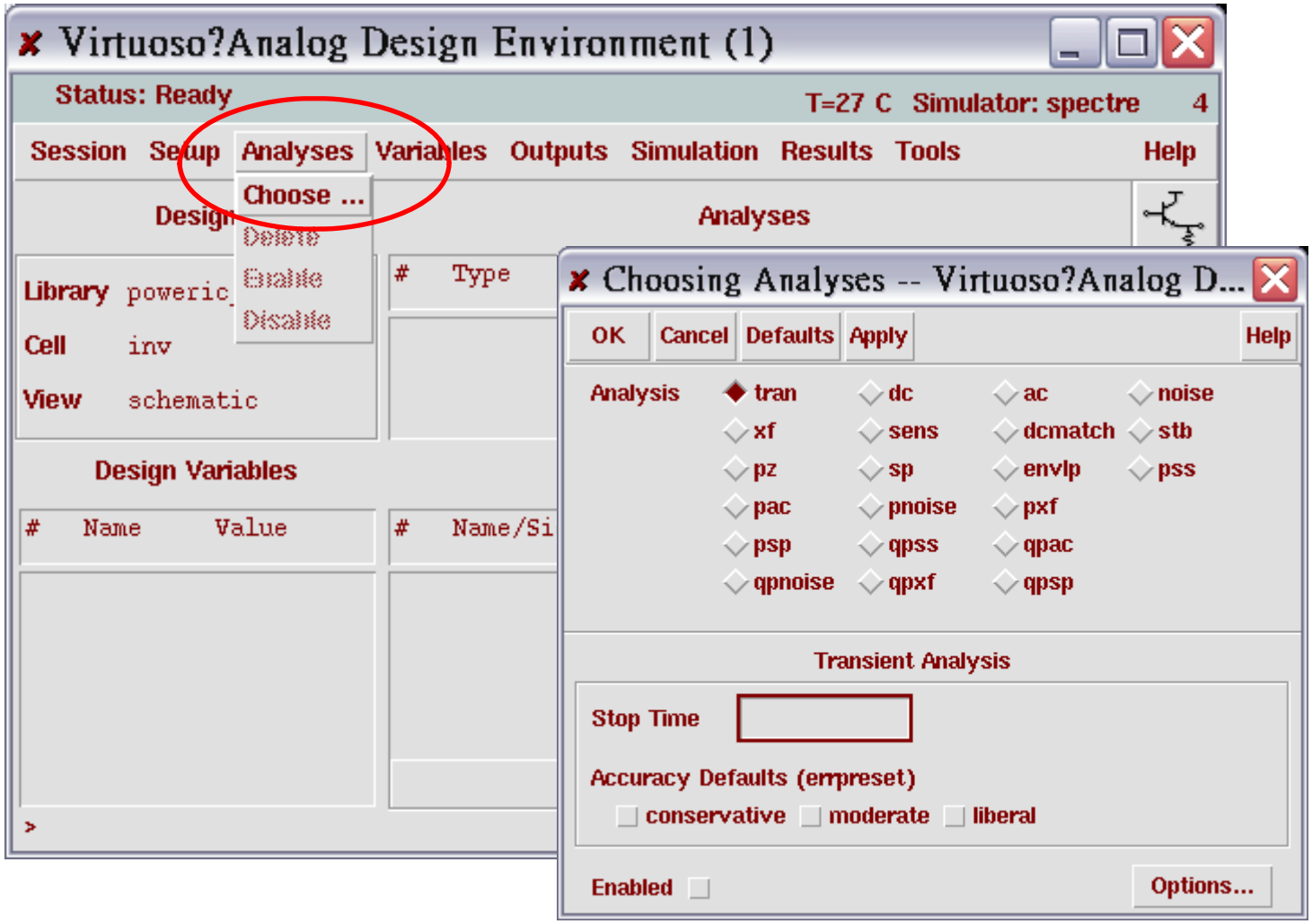

Add Instance
Hide
Cancel
Defaults
Help
Library
Browse
Cell
View
symbol
Names
Array
Rows
1
Columns
1
Rotate
Sideways
Library Browser - Add Instance
Show Categories
Library
Cell
View
tsmc18rf
rmos2v
symbol
US_8ths
ahdlLib
analogLib
basic
cdsDefTechLib
functional
power
poweric_test
rfExamples
rfLib
test
tsmc18rf
m6_T
mimcap
mimcap_rf
mos_var
mos_var33
mv_3t_LvCont
mv_3t_RvCont
mv_d5x2x2x50x1_3t
rmos2v
rmos2vdnw
rmos3v
rmos3vdnw
rmoscap
rmosmvt2v
rmosmvt3v
rmosnvt2v
rmosnvt3v
npn
ads
auCdl
auLvs
hspiceS
spectre
symbol
Close
Filters...
Help
analogLib
tsmc18rf

Cadence IC

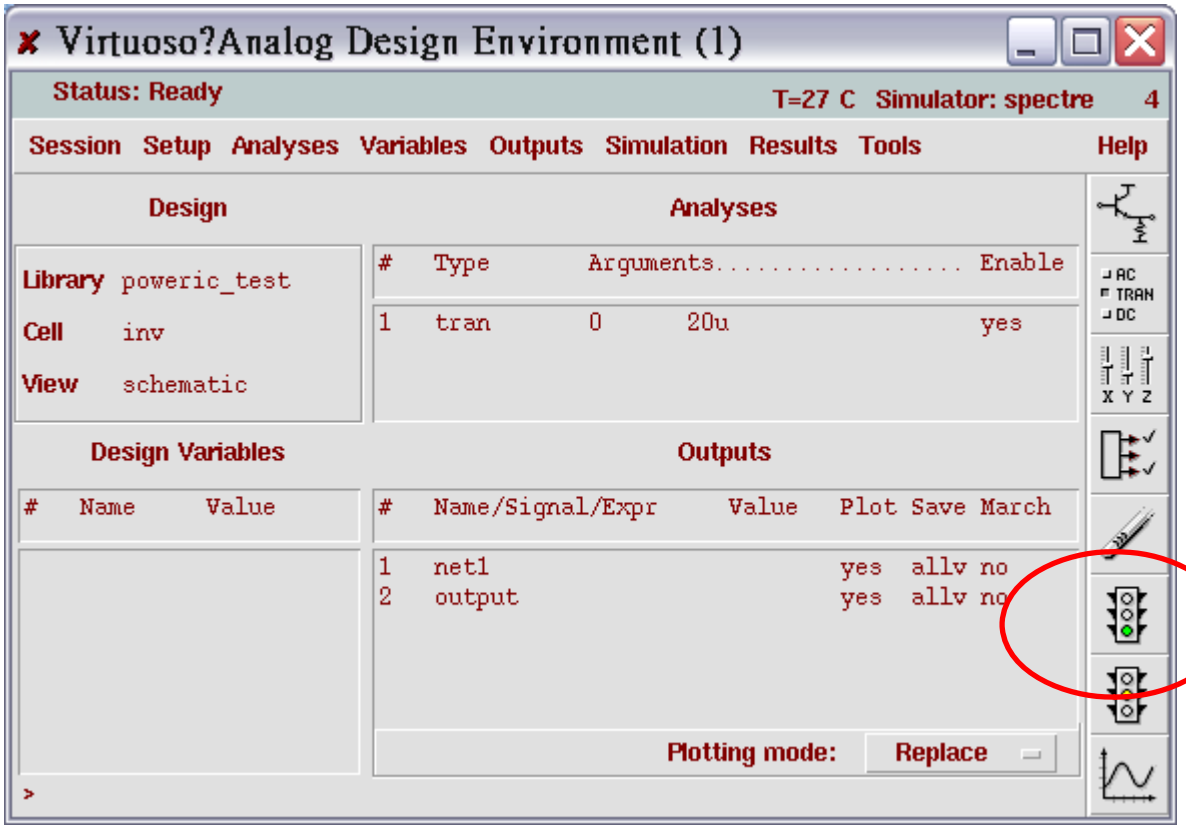
Analog Environment



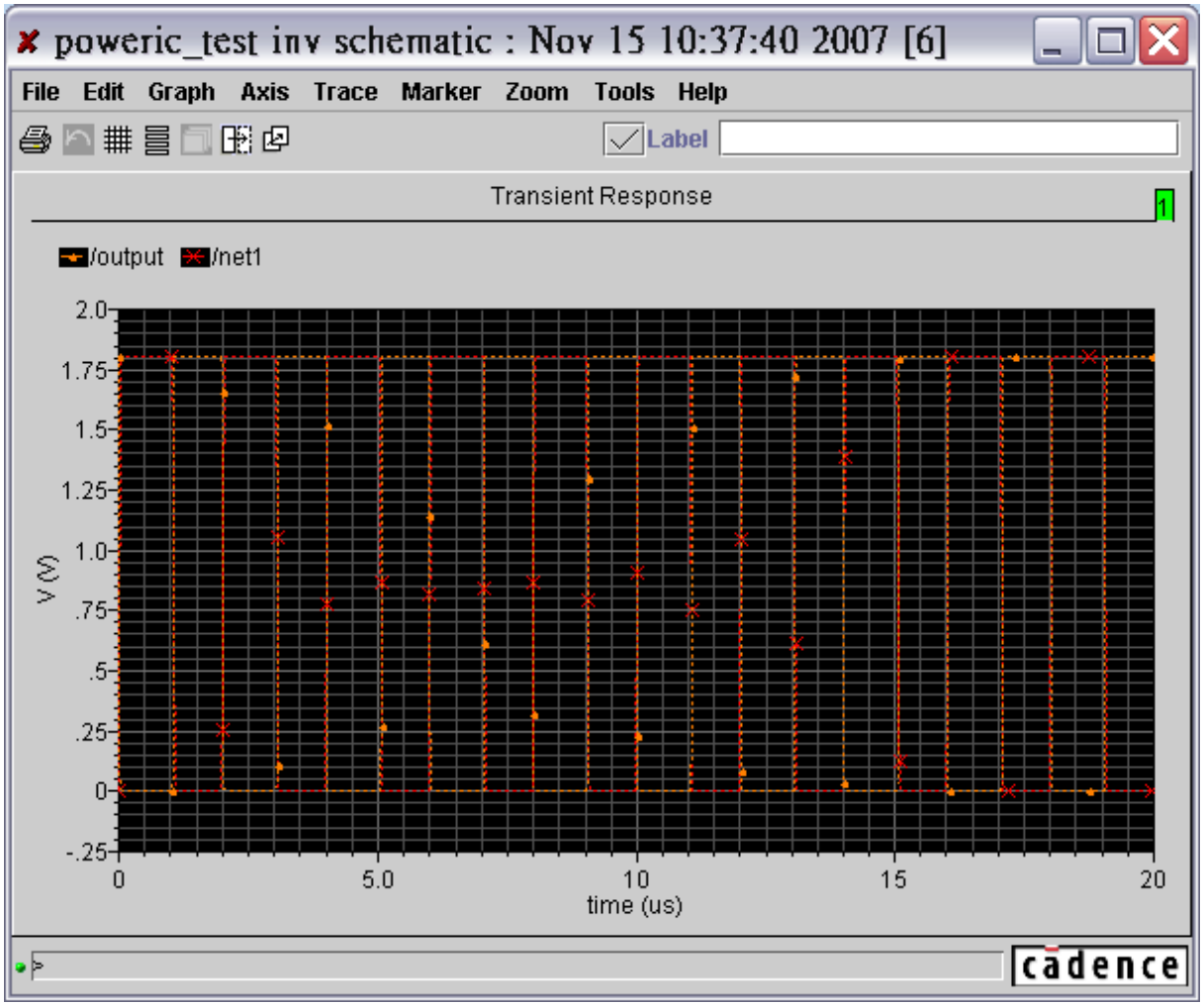
Cadence IC


Virtuoso?Analog Design Environment (1)
Status: Ready
T=27 C Simulator: spectre 4
Session Setup Analyses Variables Outputs Simulation Results Tools Help
Choose ...
Delete
Enable
Disable
Design
Analyses
Library poweric
Cell inv
View schematic
Type
Design Variables
Name Value
Name/Si
>
Choosing Analyses -- Virtuoso?Analog D...
OK Cancel Defaults Apply Help
Analysis
tran dc ac noise
xf sens dcmatch stb
pz sp envlp pss
pac pnoise pxf
psp qpss qpac
qpnoise qpxf qpsp
Transient Analysis
Stop Time
Accuracy Defaults (errpreset)
conservative moderate liberal
Enabled
Options...

Cadence IC


Virtuoso?Analog Design Environment (1)
Status: Ready
T=27 C Simulator: spectre 4
Session Setup Analyses Variables Outputs Simulation Results Tools Help
Design
Library poweric_test
Cell inv
View schematic
Analyses
Type Arguments Enable
1 tran 0 20u yes
Design Variables
Name Value
Outputs
Name/Signal/Expr Value Plot Save March
1 net1 yes allv no
2 output yes allv no
Plotting mode: Replace
>
AC
TRAN
DC
X Y Z
run

Cadence IC


poweric_test inv schematic : Nov 15 10:37:40 2007 [6]
File Edit Graph Axis Trace Marker Zoom Tools Help
Label
Transient Response
1
/output
/net1
2.0
1.75
1.5
1.25
1.0
.75
.5
.25
0
-.25
V (V)
0
5.0
10
15
20
time (us)
cadence

Midterm Presentation List