國立台灣大學 系統晶片中心

培訓課程規劃表

課程名稱（中文／英文）：

低功耗低電壓連續漸進式類比/數位轉換器設計

Low-Power Low-Voltage SAR ADC Design

演講者 ： 陳信樹 教授

時數（hr）： 3

摘要:

Architecture and power bottleneck of SAR (Successive Approximation Register) ADC (Analog to Digital Converter) will be introduced. Design considerations on the key building blocks, DAC, comparator and SAR logic, would be discussed. Practical low-power CMOS circuit design examples will be given.

大綱：

- Introduction to SAR ADC
- Low-Power Low-Voltage SAR ADC
  - Low Power Techniques
    - DAC Average Switching Energy
    - Dynamic Comparator
  - Low Voltage
    - Conventional Low Voltage Techniques
    - Low Voltage Issues
  - Small Area
    - DAC Capacitor Matching
- Summary
- Design Example

所須背景知識:

Microelectronics、Analog IC design

建議參加對象:

IC 設計工程師、CAD 工程師、研究生