High Energy-Efficient Data Converter and Power Converter IC Design

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Outline (I)

- Introduction
- A/D Converter ICs
  - Published Works (http://www.ee.ntu.edu.tw/publist?id=85)
    - A 10b 320MS/s Stage-Gain-Error Self-Calibration Pipeline ADC in 90nm
    - A 5.3mW 6b 1.25GS/s Delay-Shift SAR ADC in 40nm CMOS
    - A 0.85fJ/c.-s. 0.45V 10b 200kS/s Subrange SAR ADC in 40nm
    - A 0.6V 10b 150 MS/s Subrange SAR ADC in 40nm CMOS
    - A 2.2mW 8b 900MS/s Two-Step SAR ADC in 40nm CMOS
    - A 2fJ/c.-s. 12b 200kS/s Subrange SAR ADC in 40nm CMOS
    - A 2-Channel 3.1mW 8b 1.5GS/s Two-Step SAR ADC in 40nm
    - A 510nW 12-bit 200kS/s Subrange SAR ADC in 40nm CMOS
  - On-Going Works
    - A 1.5fJ/c.-s. 12-bit 1MS/s Subrange SAR ADC with Cap Calibration in 40nm
    - A 1.6 fJ/c.-s.10-bit 400KS/s Subrange SAR ADC with LDO in 40nm
    - A 10b 320MS/s SAR ADC in 40nm CMOS
    - A Time-Interleaved 6b 8GS/s SAR ADC in 40nm CMOS
    - A Time-Interleaved 10b 1GS/s Subrange SAR ADC in 40nm CMOS

Outline (II)

- DC/DC Converter ICs
  - Published Works (http://www.ee.ntu.edu.tw/publist?id=85)
    - A High-Efficiency DC-DC Converter with 9μs Transient Recovery Time in 0.35μm CMOS
    - A Frequency-Hopping DC-DC Converter with Transient Spur Reduction in 0.35μm CMOS
    - A Fast Transient DC-DC Converter using Hysteresis Prediction Voltage Control in 0.35μm CMOS
  - On-Going Works
    - A LED Driver Using Two-Input Floating Buck Converter with Variable Off-Time Control Scheme in 0.25μm HV CMOS
    - Capacitive DC-DC Converter
    - Power Management Circuits for Energy Harvester System

Dr. Hsin-Shu Chen(陳信樹) Background

- Position/Affiliation/Education
  - Professor
  - Graduate Institute of Electronics Engineering and Department of Electrical Engineering, NTU
  - PhD, UIUC
- Research Interests
  - High-Speed Low-power CMOS ADC/DAC
  - Power IC design (AC/DC-DC Converter, Energy Harvesting System)
- Work Experiences

Professor, EE/NTU	2/2003~
Senior Member of Technical Staff, Maxim, USA	3/2002~2/2003
Staff Engineer, Intersil, USA	2/1996~3/2002

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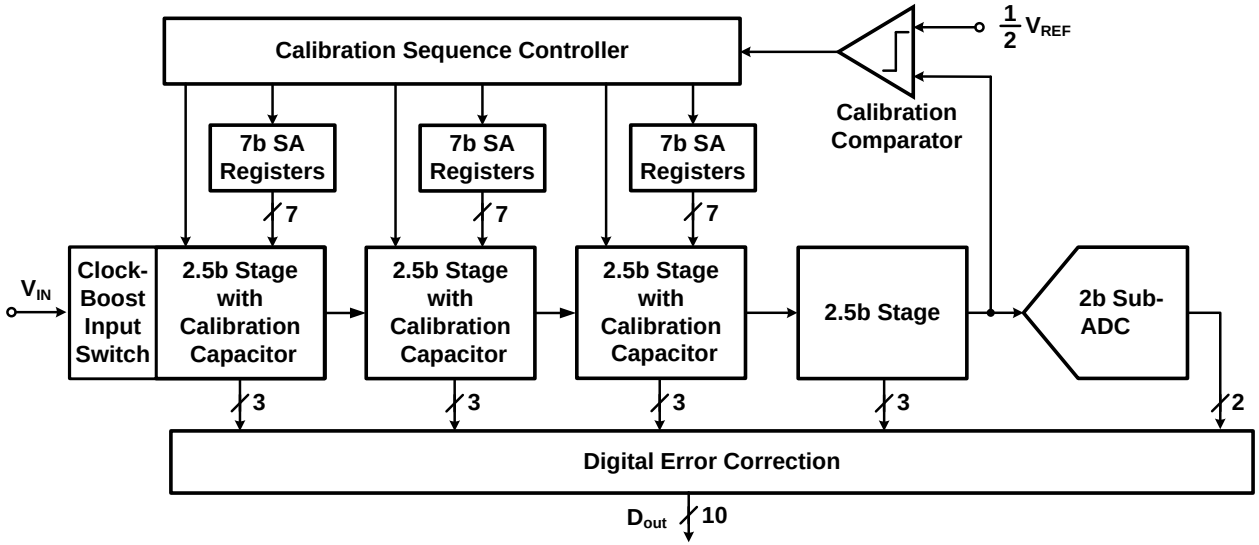
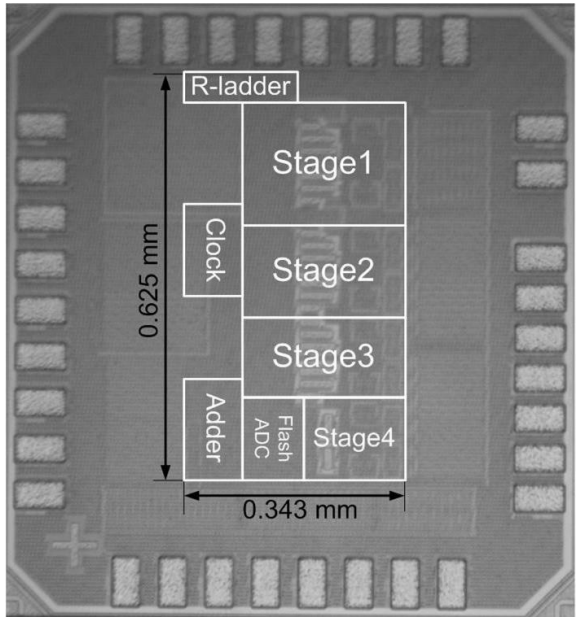
A/D Converter ICs

A 10-bit 320MS/s Stage-Gain-Error Self-Calibration Pipeline ADC in 90-nm low-power CMOS

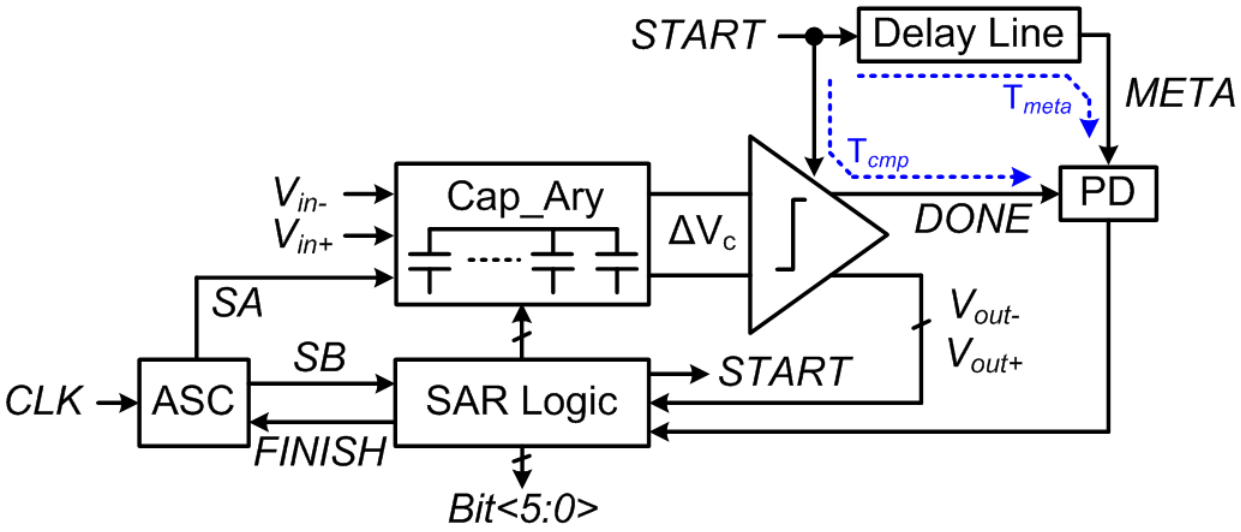


Technology	90nm LP
Resolution	10-bit
Active area	0.21mm^2
Supply voltage	1.2V
Sample rate	320MS/s
SFDR (F_{in}@Nq)	66.7dB
SNDR (F_{in}@Nq)	51.2dB
Power	42mW
FoM	0.44pJ/c.s.



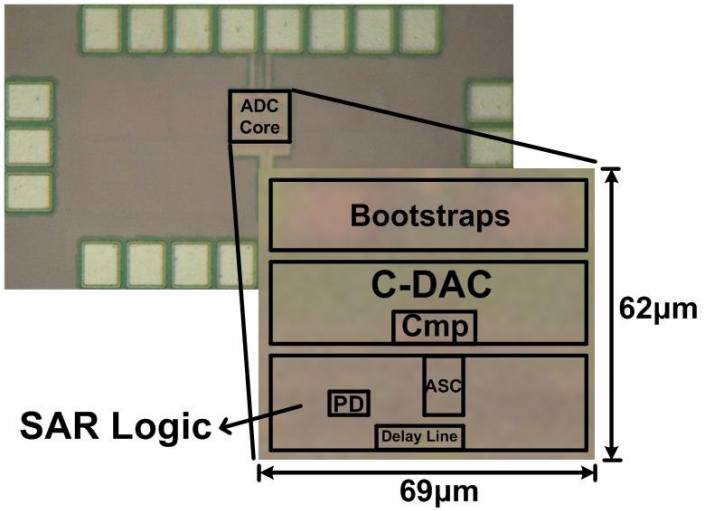
- Achieve high speed with a low-gain OPA by using digitally-assisted architecture, thus the OPAs have excellent energy efficiency
- A simple gain-error self calibration method without external precise references requires only 168 calibration clock cycles.
- *IEEE JSSC*, Vol. 47, No. 6, pp. 1334-1343, Jun. 2012

A Single-Channel 6-bit 1.25GS/s Delay-Shift SAR ADC in 40nm

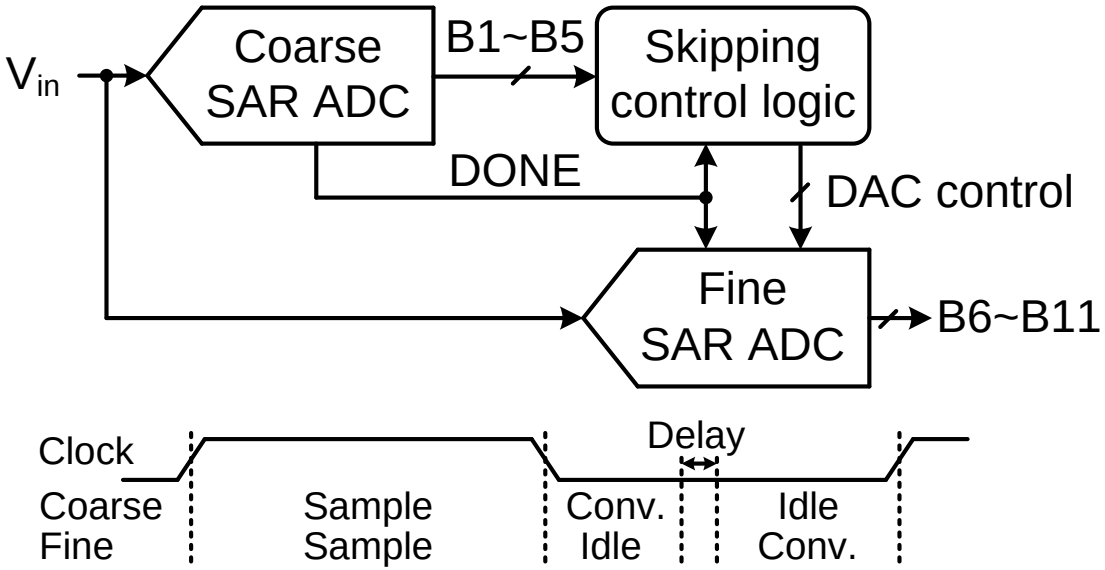


Measurement Result	
Technology	40nm GP
Resolution	6b
Active area	0.004mm^2
Supply voltage	1.2V
Conversion rate	1.25GS/s
ENOB (F_{in}@Nq)	5.3b
Power	5.3mW
FOM_{peak}	73fJ/c.-s.

- Accelerate high speed without inherent meta-stability issue
- Use time quantization to provide an effective 1.5b/cycle redundancy for the first and second cycles
- *2013 IEEE ASSCC.*

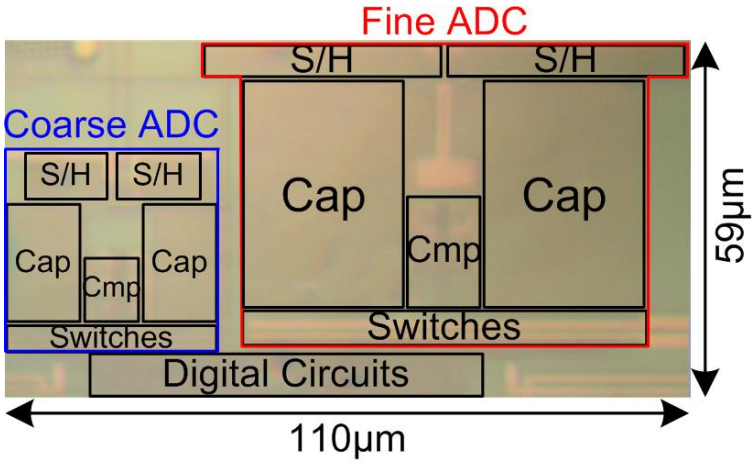


A 0.85fJ/c.-s. 10b 200kS/s Subranging SAR ADC in 40nm CMOS

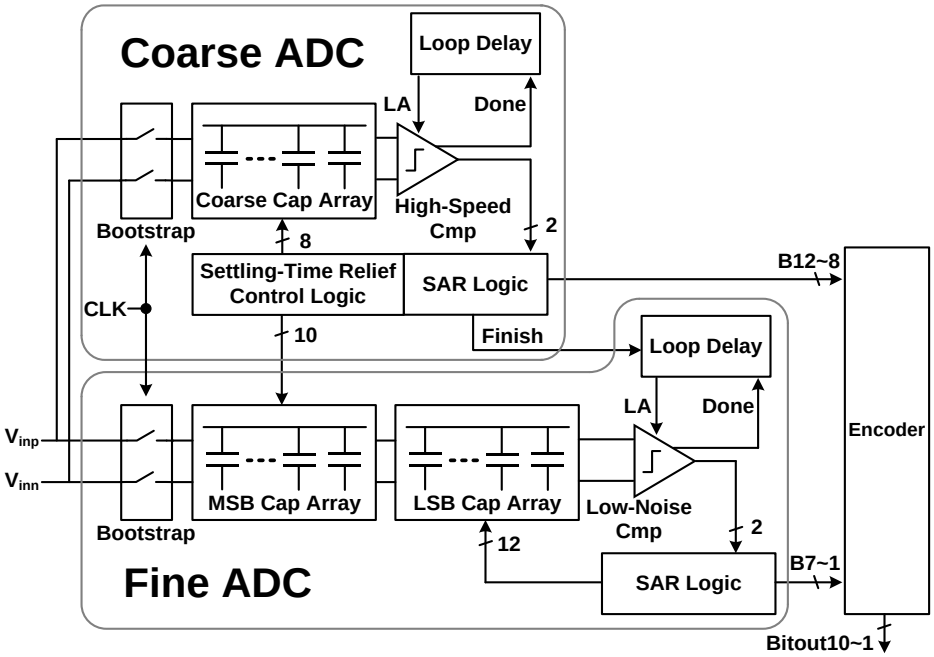


Technology	40nm LP
Resolution	10-bit
Active area	0.0065mm^2
Supply voltage	0.45V
Sample rate	200kS/s
SFDR (F_{in}@Nq)	76.3dB
SNDR (F_{in}@Nq)	55.6dB
Power	84nW
FoM	0.85fJ/c.-s.

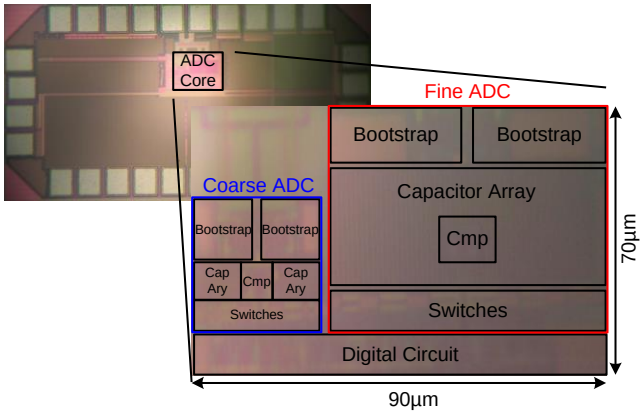
- Achieve high energy efficiency by using the proposed subranging SAR architecture.
- Reduce DAC switching energy, relax reference buffer design and enhance linearity with detect-and-skip algorithm and aligned switching technique.
- Accomplish the lowest FoM result in reported literatures in 2014!
- *2014 IEEE ISSCC.*



A 0.6V 10-bit 150 MS/s Subrange SAR ADC in 40nm

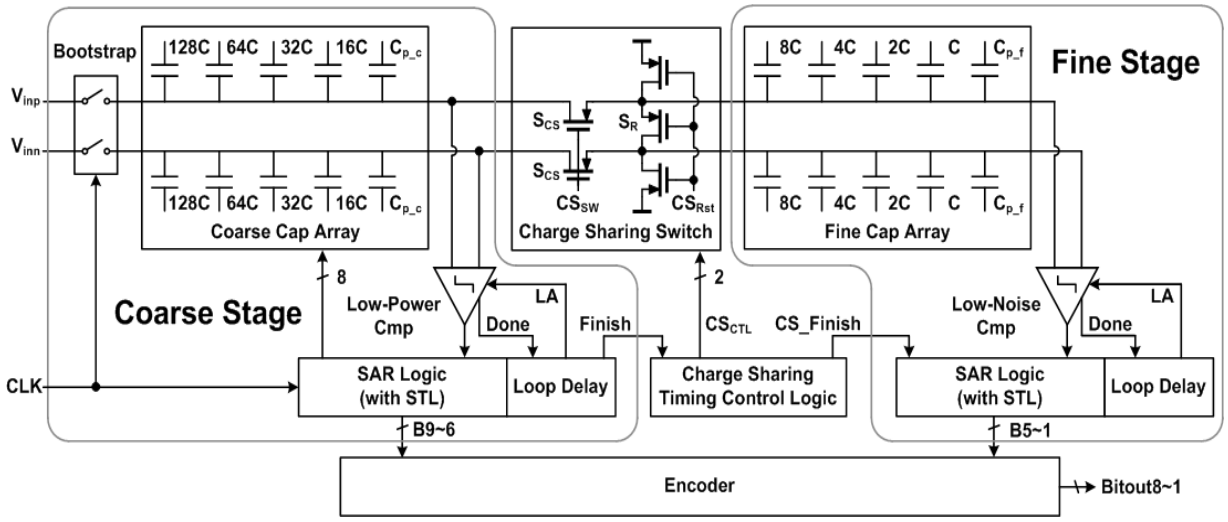


Measurement Result	
Technology	40nm GP
Resolution	10b
Supply Voltage	0.6V
Conversion rate	150MS/s
Core Area	0.0063mm^2
ENOB$_{peak}$	8.98b
Power	0.264mW
FOM$_{peak}$	3.5fJ/c.-s.



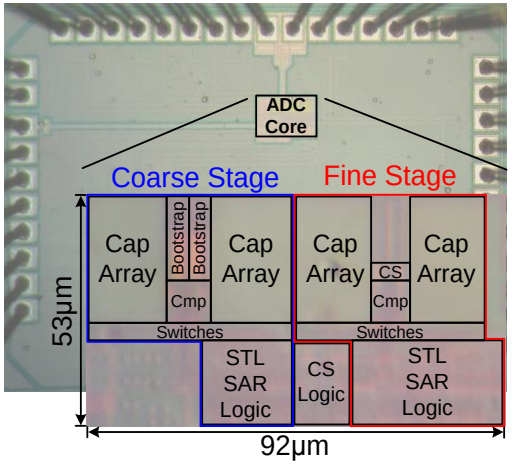
- Use a settling-time relief technique with a low-power coarse SAR ADC to accelerate conversion speed
- Use a redundancy technique to compensate comparator offset mismatches without calibration
- *2014 IEEE ASSCC*

A Single-Channel 8-bit 900MS/s Two-Step SAR ADC in 40nm

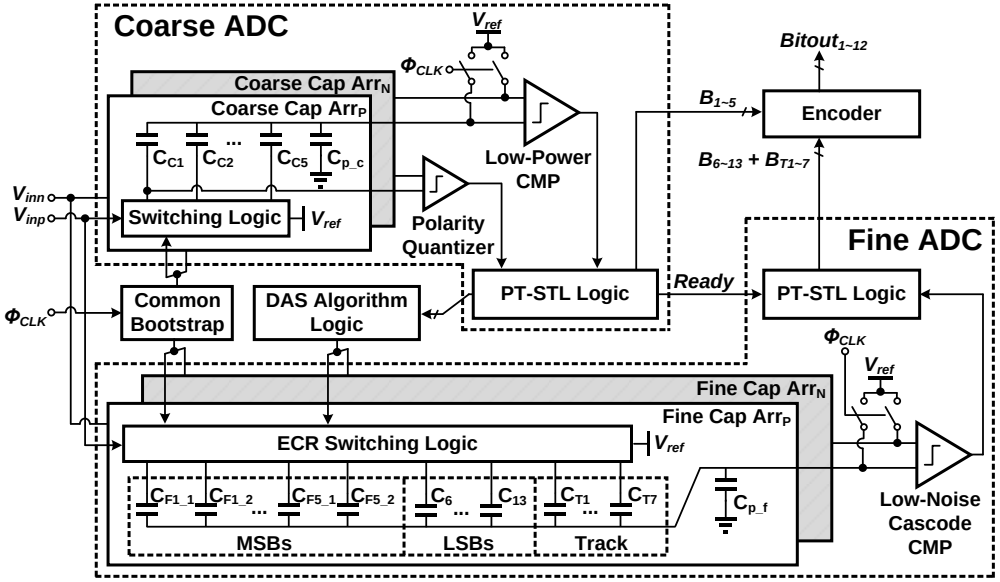


Measurement Result	
Technology	40nm GP
Resolution	8b
Active area	0.0049mm^2
Supply voltage	1.0V
Conversion rate	900MS/s
ENOB (F_{in}@Nq)	7bit
Power	2.2mW
FOM_{nq}	19.1fJ/c.-s.

- Two-step architecture to achieve high speed without an inter-stage residue amplifier
- Using self-triggered latch (STL) technique to save digital power and to accelerate the conversion speed
- C_{in}=272fF, C_u=1fF
- *2016 IEEE ISCAS LBN*; *IEEE TCAS-II*, Vol. x, No. 12, pp x, Dec. 2016

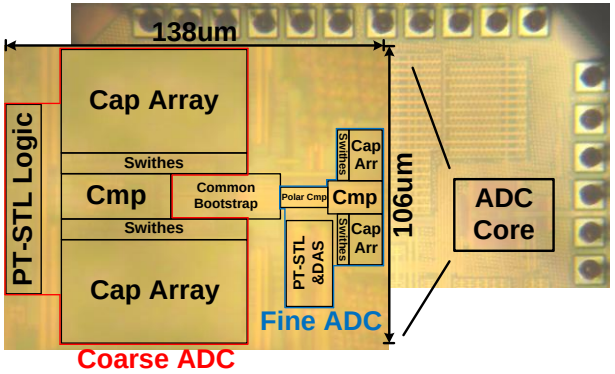


A 2fJ/c.-s. 12-bit 200kS/s Subrange SAR ADC in 40nm

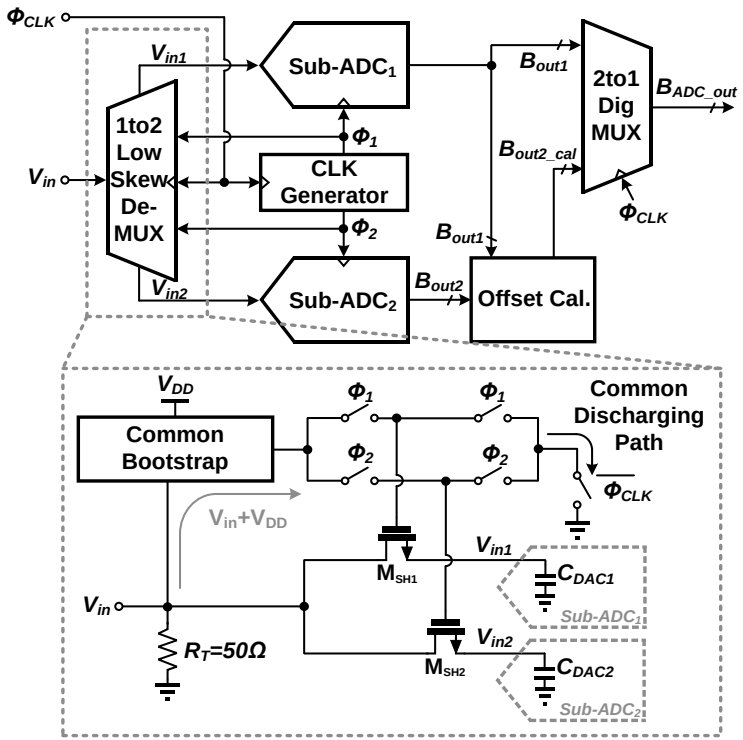


Measurement Result	
Technology	40nm LP
Resolution	12-bit
Active area	0.0146mm^2
Supply voltage	0.7V
Conversion rate	200kS/s
SFDR (F_{in}@Nq)	80.2dB
SNDR (F_{in}@Nq)	68.12dB
ENOB (F_{in}@Nq)	11.21b
Power	944nW
FOM	2fJ/c.-s.

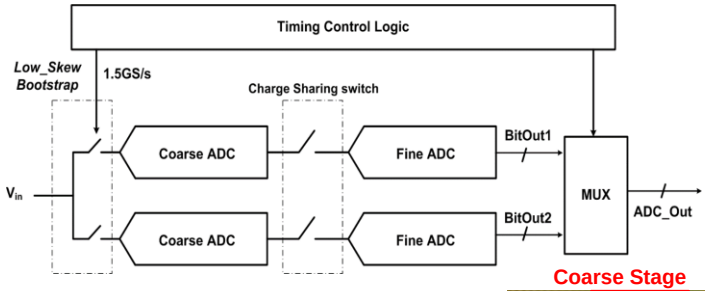
- High energy efficiency with the proprietary subranging SAR architecture, detect-and-skip algorithm and aligned switching technique
- Reduce the switching energy by using the energy-curve reshape technique in touch sensing applications
- Utilize the tracking technique and the bottom plate sample technique to achieve 12-bit resolution
- *2016 IEEE ASSCC*

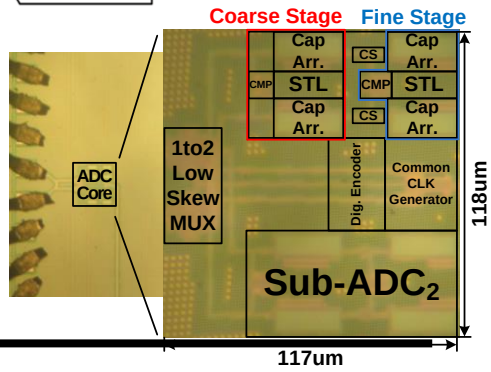


A 2-Channel 3.1mW 8-bit 1.5GS/s Two-Step SAR ADC in 40nm



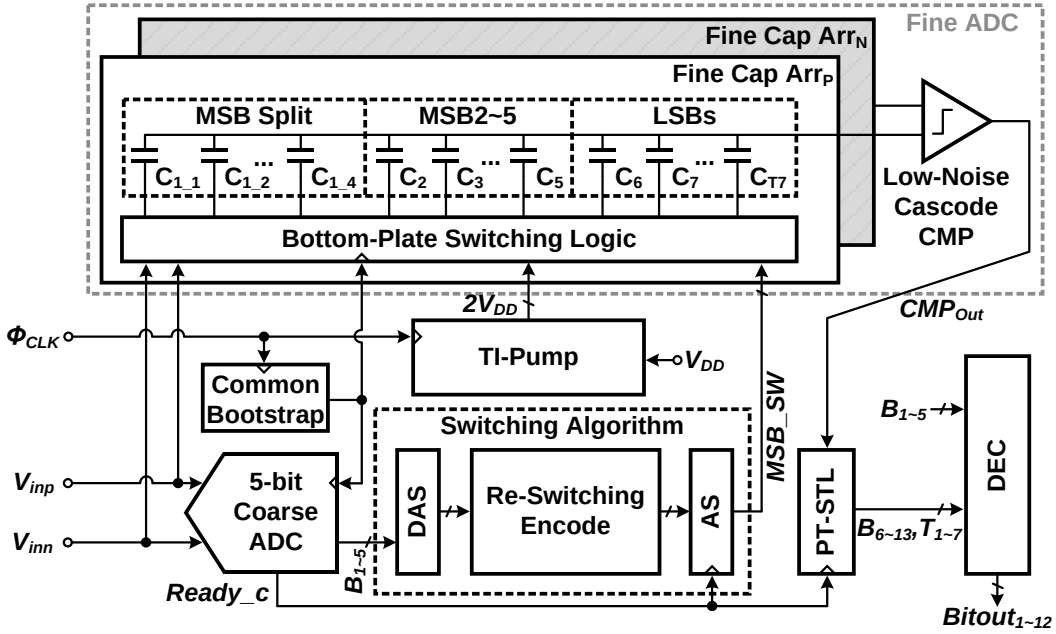
Measurement Result	
Technology	40nm GP
Resolution	8b
Active area	0.014mm^2
Supply voltage	0.9V
Conversion rate	1.5GS/s
ENOB (F_{in}@Nq)	7.1bit
Power	3.1mW
FOM	15fJ/c.-s.





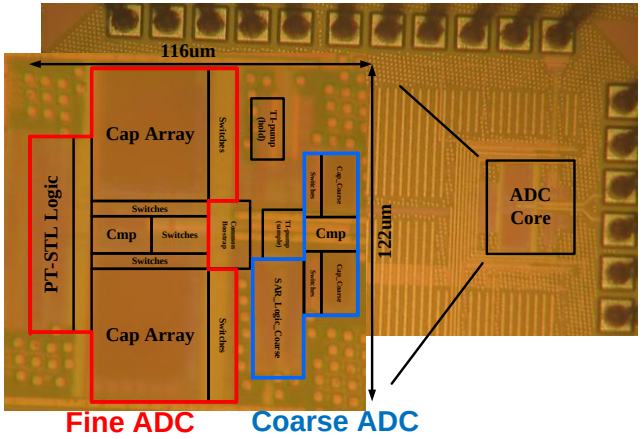
- Time-interleaved SAR ADC with a low-skew de-multiplexer
- Use dual references to scale down the total capacitance by 2
- *C_{in}=136fF, C_u=1fF*
- *2016 IEEE ASSCC*

A 1.1fJ/c.-s. 12-bit 200kS/s Subrange SAR ADC in 40nm

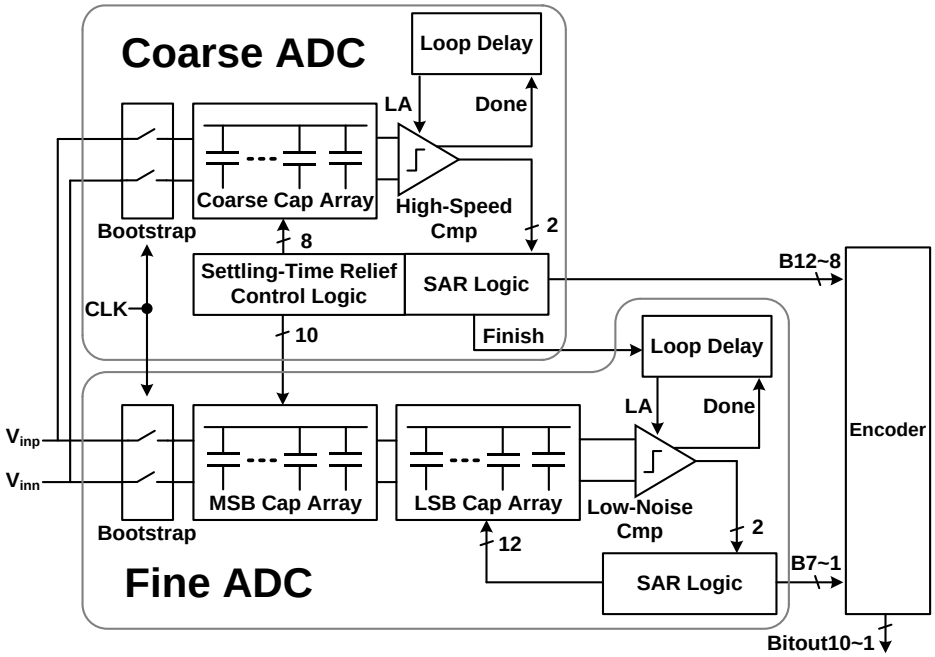


Measurement Result	
Technology	40nm LP
Resolution	12-bit
Active area	0.014mm^2
Supply voltage	0.7V
Conversion rate	200kS/s
SFDR (F_{in}@Nq)	81.72dB
SNDR (F_{in}@Nq)	69.1dB
ENOB (F_{in}@Nq)	11.19b
Power	510nW
FOM	1.1fJ/c.-s.

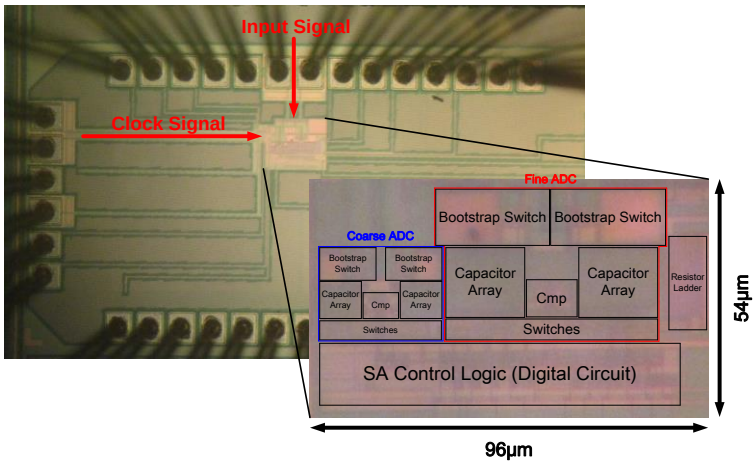
- High energy efficiency with the proprietary subranging SAR architecture, detect-and-skip algorithm and aligned switching technique
- Enhance DNL by Re-switching detect-and-skip.
- Use 2-way charge pump to reduce large turn-on resistance caused by the adopted Vcm-based switching method
- *2017 IEEE VLSI Symposia.*



A Single-Channel 10-bit 320 MS/s Subrange SAR ADC in 40nm

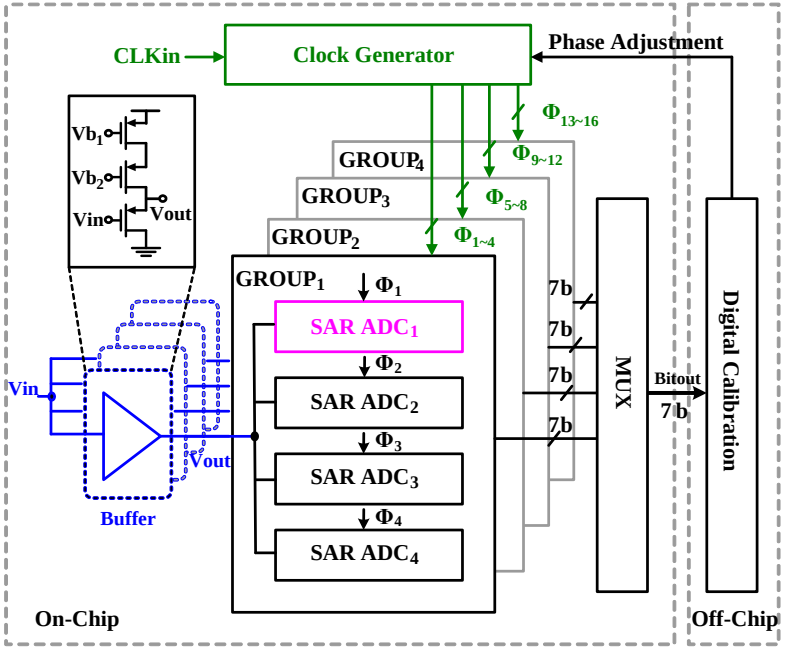


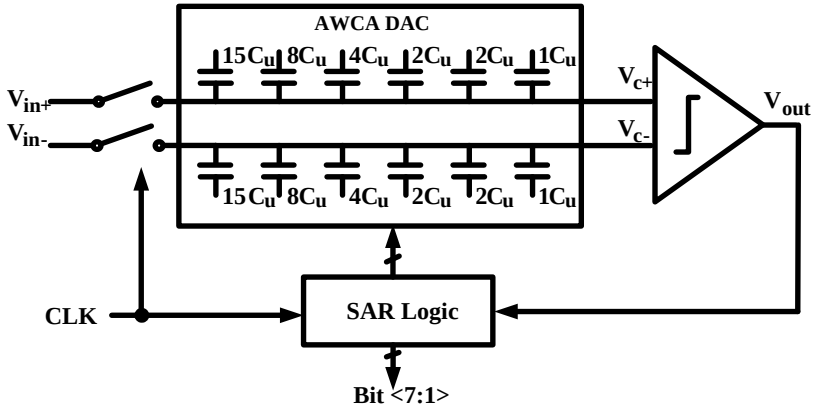
Measurement Result	
Technology	40nm GP
Resolution	10b
Supply Voltage	0.9V
Conversion rate	320MS/s
Core Area	0.0052mm^2
ENOB	7.5b
Power	0.673mW
FOM	12fJ/c.-s.



- SAR-assisted SAR ADC using a Settling-Time Relief (STR) technique to accelerate conversion rate
- Dual-reference technique is utilized to reduce chip area and to increase conversion speed
- *Status: 2nd gen. test chip under evaluation*
- C_{in}=620fF, C_u=1fF

A Time-Interleaved 6-bit 8GS/s SAR ADC in 40nm

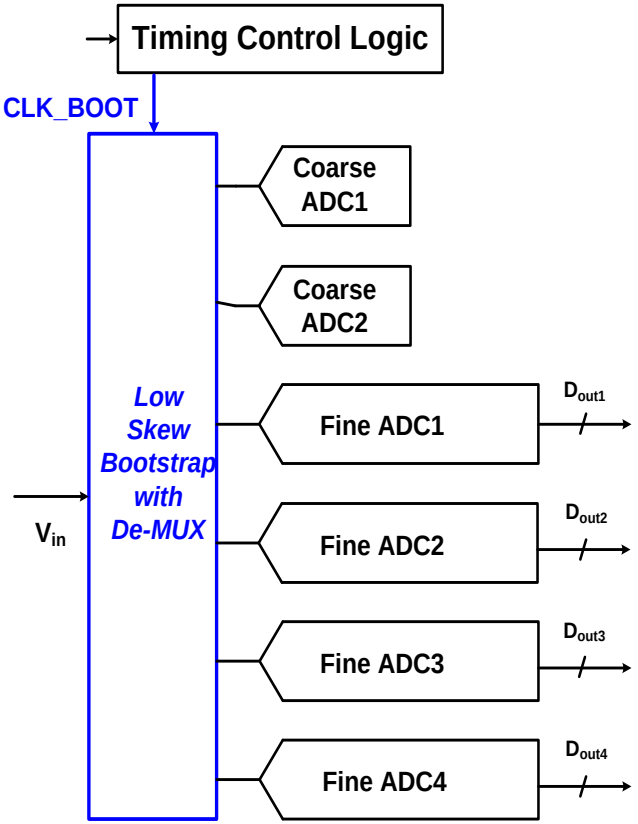




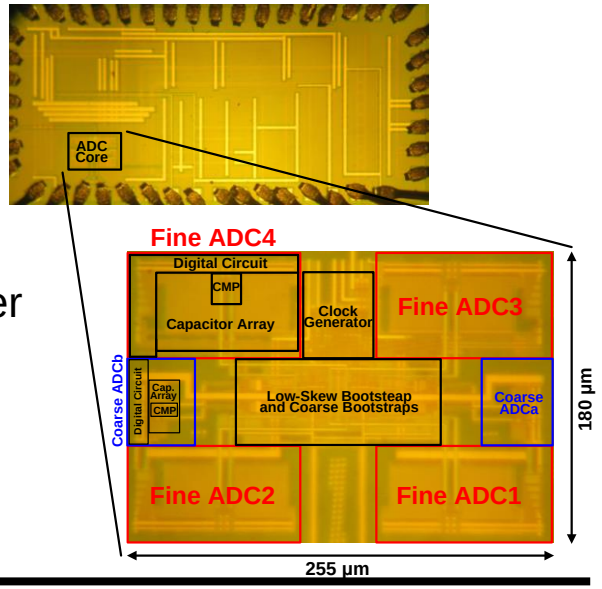
- A grouping technique is used for the front-end sampling to increase input bandwidth and to avoid charge sharing
- Use a timing mismatch detection technique for skew calibration.
- *Status: 3rd gen. test chip in fabrication*

Post-Simulation result	
Technology	40nm GP
Area(mm^2)	0.21
Resolution(bit)	6
Voltage(V)	1.2
Sampling(GS/s)	8
Power(mW)	53.6
SNDR@Nyquist(dB)	35.62
FoM(fJ/C.S.)	135.3
Calibration	Yes

A 4-Channel 10-bit 1GS/s Subrange SAR ADC in 40nm



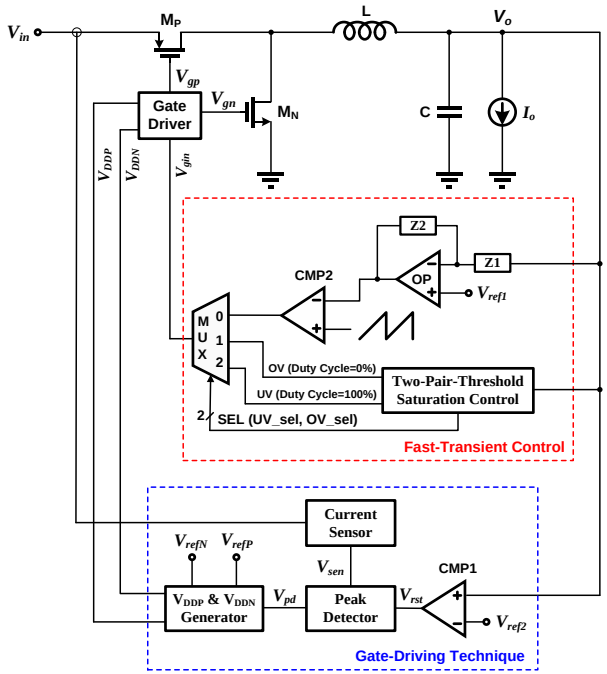
Measurement Result	
Technology	40nm GP
Resolution	10b
Channel	4
Supply voltage	0.9V
Conversion rate	1GS/s
Core Area	0.046mm^2
ENOB@Fin=1M	8.284b
Power	5.0881mW



- One rank THA with a low-skew bootstrap and de-multiplexer
- Use hybrid architecture of sub-ranging and SAR to improve energy efficiency
- *C_{in}=544fF, C_u=1fF*
- *Status: 3rd gen. test chip under evaluation*

DC-DC Converter ICs

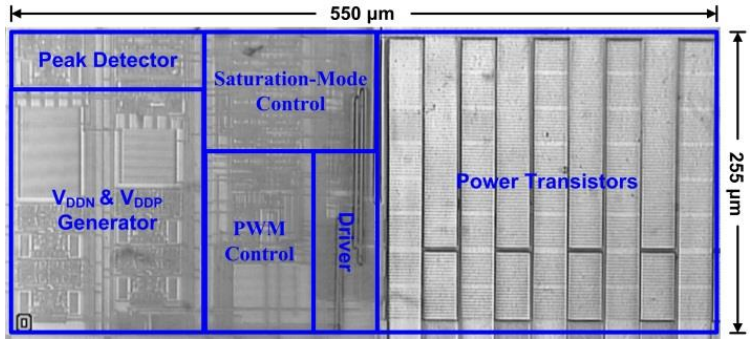
A High-Efficiency DC-DC Converter with 9μs Transient Recovery Time in 0.35μm CMOS



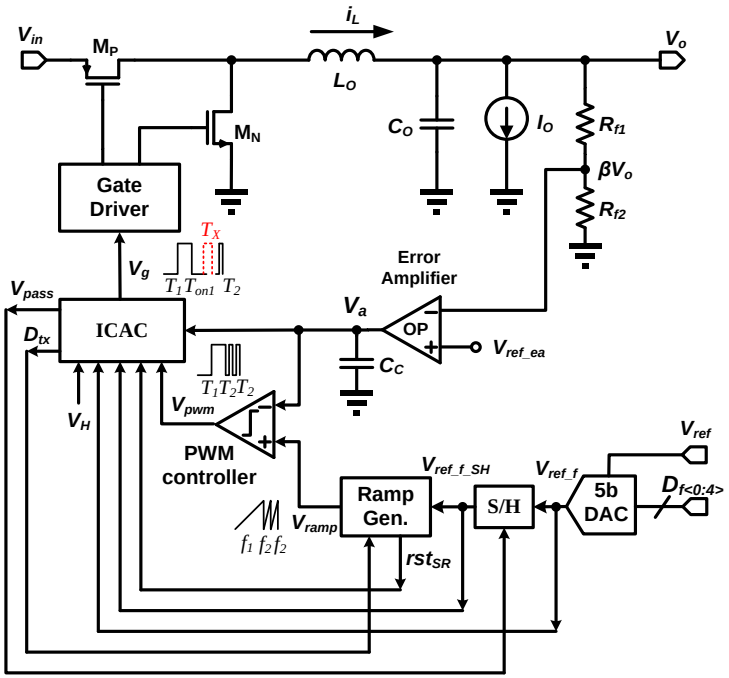
Technology	0.35μm
Active area*	0.14mm^2
Input voltage range	2.6~3.6V
Output voltage range	0.6~2.1V
Switch Frequency	1MHz
Maximum Efficiency	90%@60mA
Transient Recovery Time	9μs@450mA load step
Transient Ripple	200mV@450 mA load step
Output Inductor L / Capacitor C	22μH / 22μF (ESR=25mΩ)

*On-chip power transistors

- Operate under a PWM mode during steady state and enables a saturation-mode during transient to attain fast transient response
- Optimize the gate-driving voltage by the linearly scaled gate-driving technique for light-load efficiency
- *IEEE TCAS-I*, Vol. 59, No. 3, pp. 575-583, Mar. 2012

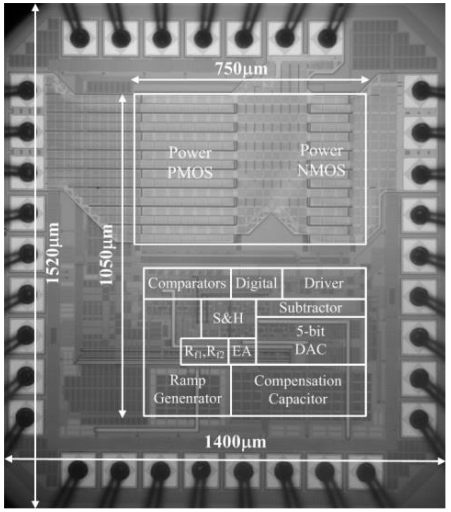


A Frequency-Hopping DC-DC Converter with Transient Spur Reduction in 0.35μm CMOS



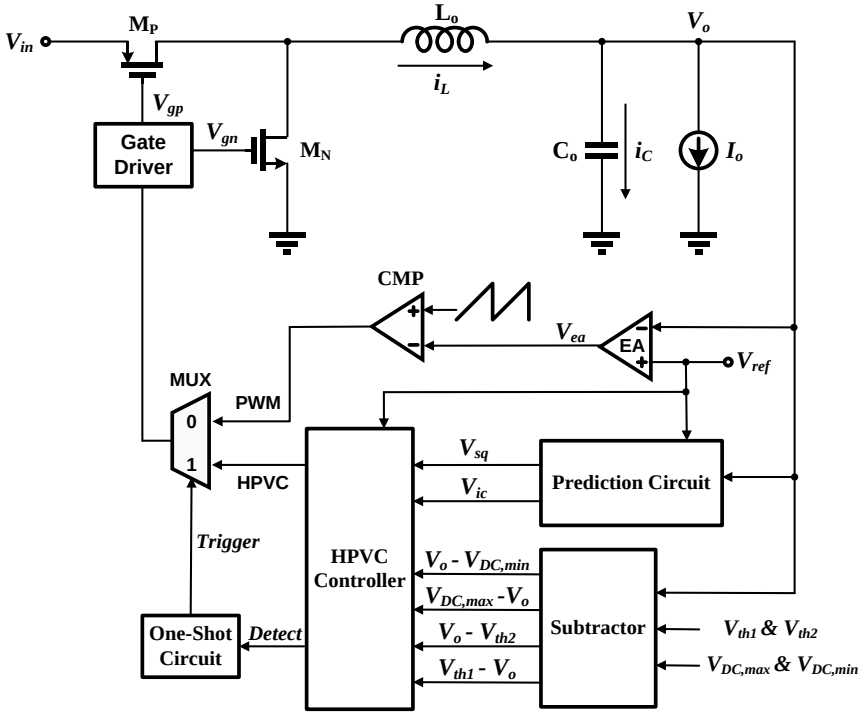
Technology	0.35μm
Active area*	0.79mm^2
Input voltage	5V
Output voltage	2.5V
Avg. switch frequency	2MHz
Transient spur reduction with 2 hopping frequencies	14.1dB
Maximum Efficiency	89.5%@180mA
Output Inductor L / Capacitor C	1μH / 1μF (ESR=20mΩ)

*On-chip power transistors



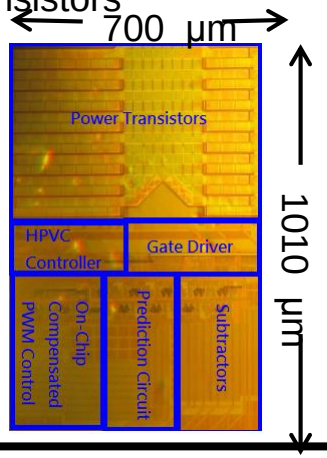
- Select the frequency hopping instant such that the average inductor current is undisturbed when the switching frequency hops
- *IEEE TPE*, Vol. 27, No. 11, pp. 4763-4771, Nov. 2012

A Fast Transient DC-DC Converter using Hysteresis Prediction Voltage Control in 0.35μm CMOS



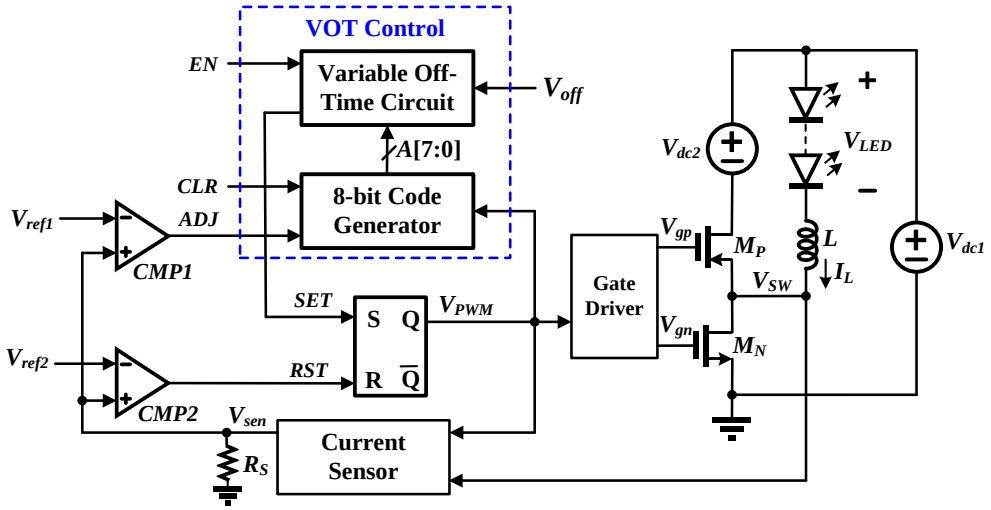
Technology	0.35μm
Active area*	0.707mm^2
Input voltage range	4.5~5.5V
Output voltage	2.5 V
Switch Frequency	1MHz
Maximum Efficiency	87.2%
Transient Recovery Time	<2.5μs@500 mA load step
Transient Ripple	74mV@500 mA load step
Output Inductor L / Capacitor C	4.7μH/ 4.7μF (ESR=30mΩ)

*On-chip power transistors



- Use a prediction method with early actions to suppress the output voltage ringing, and to mitigate the output voltage overshoot/undershoot
- Operate under PWM mode during steady state and early switch to the proposed HPVC mode during transient to saturate duty-cycle for fast transient recovery time
- *IET Transactions on Power Electronics 2016*

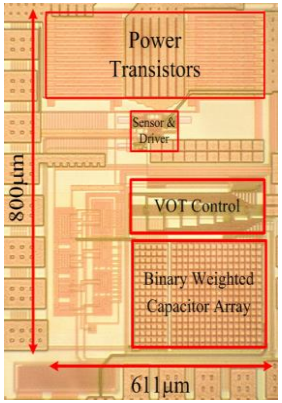
A LED Driver Using Two-Input Floating Buck Converter with Variable Off-Time Control Scheme in 0.25μm HV CMOS



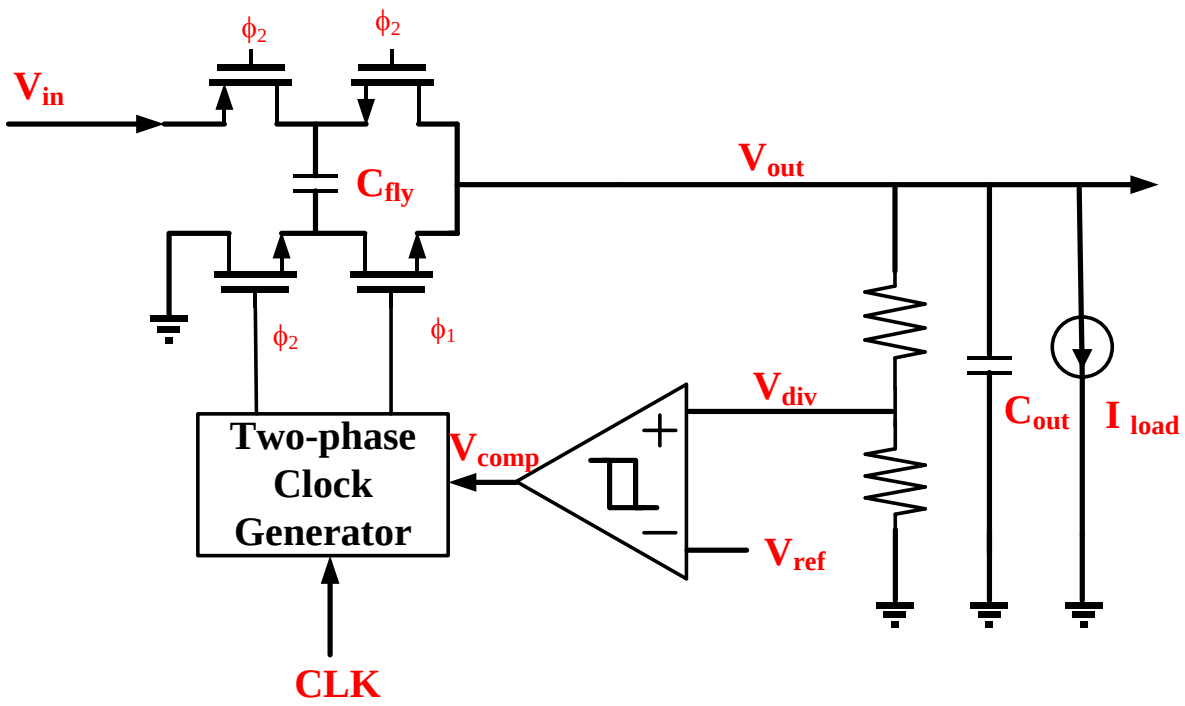
Technology	0.25μm HV
Active area*	0.49mm^2
Input voltage range	23~21 V & 20~18 V
Topology	current-mode TIFB
Switch Frequency	<1.5MHz
Maximum Efficiency	97.6%
No. of LEDs	up to 6
LED current accuracy	3 %
Output Inductor L	10μH

*On-chip power transistors

- A two-input floating buck (TIFB) converter decreases voltage stress to accomplish high power efficiency
- Variable off-time (VOT) control with an on-chip current sensor to achieve high accuracy
- *Status: submit to IEEE Journal of Emerging and Selected Topics in Power Electronics*

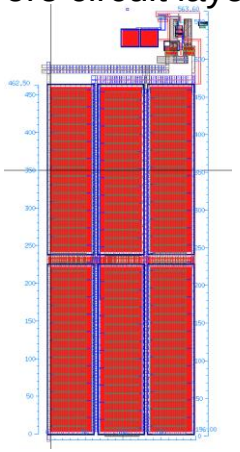


Capacitive DC-DC Converter



Technology	40LP
V_{in}	1.8V
V_{out}	0.8~0.85V
Flying Cap	480pF MOScap 100pF MOMcap 200um x450um
V_{ref}	0.75V
Clock Freq	1~10M
Max current loading	0.15mA @ 1MHz 1.2mA @ 10MHz
Power efficiency	70%
C_{out}	2nF
Core Area	200um x550um

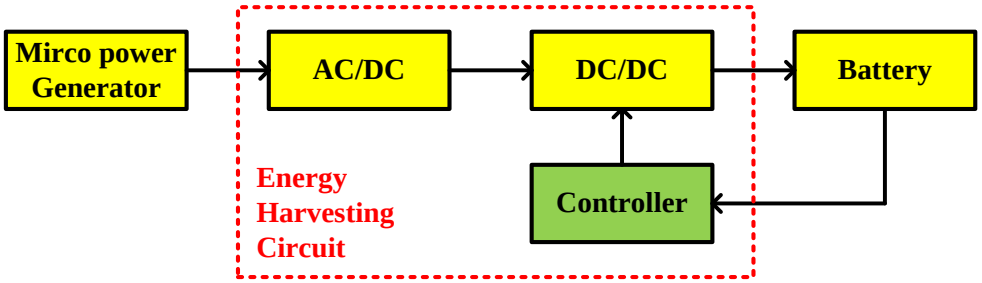
Core circuit layout



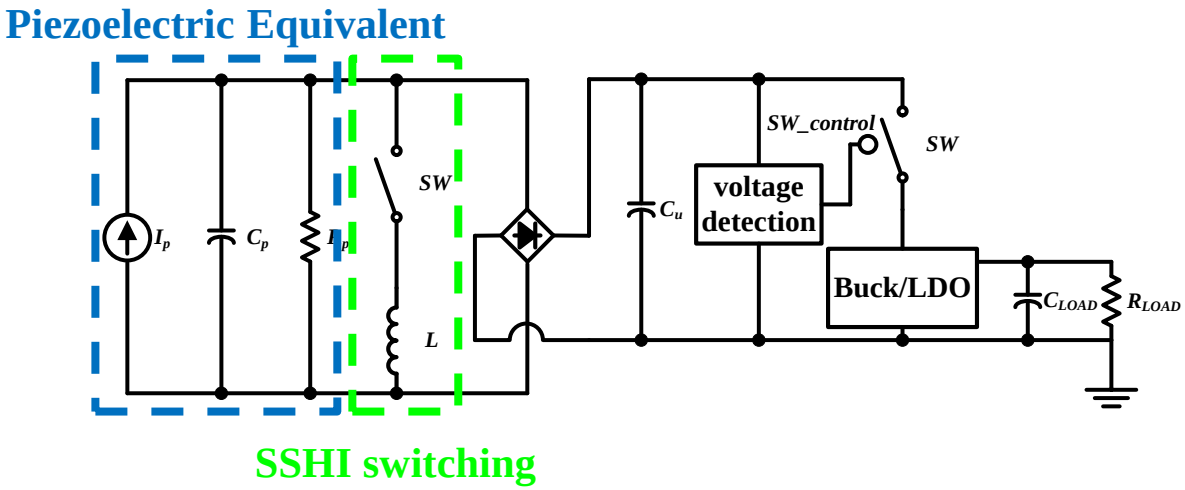
- PFM control by using a hysteretic comparator to switch the clock on/off
- Switched capacitor power stage with 2:1 ratio
- Status: *1st gen. test chip under evaluation*

Power Management Circuits for Energy Harvester System

- Energy harvesting circuits consist of a rectifier AC/DC converter with a switching interfacing circuit, a DC–DC converter and a controller.



- Rectifier AC/DC converter integrates with a switching interfacing circuit of Synchronized Switch Harvesting on Inductor(SSHI)



- Status: *under construction*

Thank You!