High Energy-Efficient Data Converter and Power Converter IC Design

陳信樹 Hsin-Shu Chen

Mixed-Signal IC Lab.
Webpage: http://cc.ee.ntu.edu.tw/~hschen/

National Taiwan University
Department of Electrical Engineering
Outline (I)

- Introduction
- A/D Converter ICs
  - Published Works (http://www.ee.ntu.edu.tw/publist?id=85)
    - A 10b 320MS/s Stage-Gain-Error Self-Calibration Pipeline ADC in 90nm
    - A 5.3mW 6b 1.25GS/s Delay-Shift SAR ADC in 40nm CMOS
    - A 0.85fJ/c.-s. 0.45V 10b 200kS/s Subrange SAR ADC in 40nm
    - A 0.6V 10b 150 MS/s Subrange SAR ADC in 40nm CMOS
    - A 2.2mW 8b 900MS/s Two-Step SAR ADC in 40nm CMOS
    - A 2fJ/c.-s. 12b 200kS/s Subrange SAR ADC in 40nm CMOS
    - A 2-Channel 3.1mW 8b 1.5GS/s Two-Step SAR ADC in 40nm
    - A 510nW 12-bit 200kS/s Subrange SAR ADC in 40nm CMOS
  - On-Going Works
    - A 1.5fJ/c.-s. 12-bit 1MS/s Subrange SAR ADC with Cap Calibration in 40nm
    - A 1.6 fJ/c.-s.10-bit 400KS/s Subrange SAR ADC with LDO in 40nm
    - A 10b 320MS/s SAR ADC in 40nm CMOS
    - A Time-Interleaved 6b 8GS/s SAR ADC in 40nm CMOS
    - A Time-Interleaved 10b 1GS/s Subrange SAR ADC in 40nm CMOS
Outline (II)

• DC/DC Converter ICs
  - Published Works (http://www.ee.ntu.edu.tw/publist?id=85)
    - A High-Efficiency DC-DC Converter with 9μs Transient Recovery Time in 0.35μm CMOS
    - A Frequency-Hopping DC-DC Converter with Transient Spur Reduction in 0.35μm CMOS
    - A Fast Transient DC-DC Converter using Hysteresis Prediction Voltage Control in 0.35μm CMOS
  - On-Going Works
    - A LED Driver Using Two-Input Floating Buck Converter with Variable Off-Time Control Scheme in 0.25μm HV CMOS
    - Capacitive DC-DC Converter
    - Power Management Circuits for Energy Harvester System
Dr. Hsin-Shu Chen (陳信樹) Background

- **Position/Affiliation/Education**
  - Professor
  - Graduate Institute of Electronics Engineering and Department of Electrical Engineering, NTU
  - PhD, UIUC

- **Research Interests**
  - High-Speed Low-power CMOS ADC/DAC
  - Power IC design (AC/DC-DC Converter, Energy Harvesting System)

- **Work Experiences**
  - Professor, EE/NTU 2/2003~
  - Senior Member of Technical Staff, Maxim, USA 3/2002~2/2003
  - Staff Engineer, Intersil, USA 2/1996~3/2002

Mixed-Signal IC Lab.

Webpage: http://cc.ee.ntu.edu.tw/~hschen/
A/D Converter ICs
A 10-bit 320MS/s Stage-Gain-Error Self-Calibration Pipeline ADC in 90-nm low-power CMOS

- Achieve high speed with a low-gain OPA by using digitally-assisted architecture, thus the OPAs have excellent energy efficiency
- A simple gain-error self calibration method without external precise references requires only 168 calibration clock cycles.

**Components and Specifications**

- **Technology**: 90nm LP
- **Resolution**: 10-bit
- **Active area**: 0.21mm²
- **Supply voltage**: 1.2V
- **Sample rate**: 320MS/s
- **SFDR (F_{in}@Nq)**: 66.7dB
- **SNDR (F_{in}@Nq)**: 51.2dB
- **Power**: 42mW
- **FoM**: 0.44pJ/c.s.
A Single-Channel 6-bit 1.25GS/s Delay-Shift SAR ADC in 40nm

- Accelerate high speed without inherent meta-stability issue
- Use time quantization to provide an effective 1.5b/cycle redundancy for the first and second cycles
- 2013 IEEE ASSCC.

**Measurement Result**

<table>
<thead>
<tr>
<th>Technology</th>
<th>40nm GP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>6b</td>
</tr>
<tr>
<td>Active area</td>
<td>0.004mm²</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>1.2V</td>
</tr>
<tr>
<td>Conversion rate</td>
<td>1.25GS/s</td>
</tr>
<tr>
<td>ENOB (F_{in}@Nq)</td>
<td>5.3b</td>
</tr>
<tr>
<td>Power</td>
<td>5.3mW</td>
</tr>
<tr>
<td>FOM (_{peak})</td>
<td>73fJ/c.-s.</td>
</tr>
</tbody>
</table>

- **Figure**
  - A Single-Channel 6-bit 1.25GS/s Delay-Shift SAR ADC in 40nm technology. The figure illustrates the block diagram of the ADC, including components such as the SAR Logic, Cap_Ary, Delay Line, and PD. The ADC features a resolution of 6b, an active area of 0.004mm², a supply voltage of 1.2V, a conversion rate of 1.25GS/s, an ENOB of 5.3b, a power consumption of 5.3mW, and a peak FOM of 73fJ/c.-s. The ADChip Core is 62μm tall, with a C-DAC Cmp of 69μm and Bootstraps. The SAR Logic includes PDs, ASCs, and Delay Lines.
Achieve high energy efficiency by using the proposed subranging SAR architecture.

Reduce DAC switching energy, relax reference buffer design and enhance linearity with detect-and-skip algorithm and aligned switching technique.

Accomplish the lowest FoM result in reported literatures in 2014!

2014 IEEE ISSCC.
A 0.6V 10-bit 150 MS/s Subrange SAR ADC in 40nm

- Use a settling-time relief technique with a low-power coarse SAR ADC to accelerate conversion speed
- Use a redundancy technique to compensate comparator offset mismatches without calibration
- 2014 IEEE ASSCC

<table>
<thead>
<tr>
<th>Measurement Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
</tr>
<tr>
<td>Resolution</td>
</tr>
<tr>
<td>Supply Voltage</td>
</tr>
<tr>
<td>Conversion rate</td>
</tr>
<tr>
<td>Core Area</td>
</tr>
<tr>
<td>ENOB$_{\text{peak}}$</td>
</tr>
<tr>
<td>Power</td>
</tr>
<tr>
<td>FOM$_{\text{peak}}$</td>
</tr>
</tbody>
</table>

Hsin-Shu Chen
Two-step architecture to achieve high speed without an inter-stage residue amplifier

Using self-triggered latch (STL) technique to save digital power and to accelerate the conversion speed

\( C_{\text{in}} = 272fF, \ C_u = 1fF \)

High energy efficiency with the proprietary subranging SAR architecture, detect-and-skip algorithm and aligned switching technique

Reduce the switching energy by using the energy-curve reshape technique in touch sensing applications

Utilize the tracking technique and the bottom plate sample technique to achieve 12-bit resolution

2016 IEEE ASSCC
A 2-Channel 3.1mW 8-bit 1.5GS/s Two-Step SAR ADC in 40nm

- Time-interleaved SAR ADC with a low-skew de-multiplexer
- Use dual references to scale down the total capacitance by 2
- $C_{in}=136fF$, $C_u=1fF$
- 2016 IEEE ASSCC

Measurement Result

<table>
<thead>
<tr>
<th>Technology</th>
<th>40nm GP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>8b</td>
</tr>
<tr>
<td>Active area</td>
<td>0.014mm$^2$</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>0.9V</td>
</tr>
<tr>
<td>Conversion rate</td>
<td>1.5GS/s</td>
</tr>
<tr>
<td>ENOB ($F_{in}@Nq$)</td>
<td>7.1bit</td>
</tr>
<tr>
<td>Power</td>
<td>3.1mW</td>
</tr>
<tr>
<td>FOM</td>
<td>15fJ/c.-s.</td>
</tr>
</tbody>
</table>

NTU Confidential
High energy efficiency with the proprietary subranging SAR architecture, detect-and-skip algorithm and aligned switching technique

Enhance DNL by Re-switching detect-and-skip.

Use 2-way charge pump to reduce large turn-on resistance caused by the adopted Vcm-based switching method

2017 IEEE VLSI Symposium.
A Single-Channel 10-bit 320 MS/s Subrange SAR ADC in 40nm

- SAR-assisted SAR ADC using a Settling-Time Relief (STR) technique to accelerate conversion rate
- Dual-reference technique is utilized to reduce chip area and to increase conversion speed
- Status: 2nd gen. test chip under evaluation
- $C_{in}=620fF$, $C_u=1fF$
A grouping technique is used for the front-end sampling to increase input bandwidth and to avoid charge sharing.

- Use a timing mismatch detection technique for skew calibration.

- Status: 3\textsuperscript{rd} gen. test chip in fabrication.
A 4-Channel 10-bit 1GS/s Subrange SAR ADC in 40nm

- One rank THA with a low-skew bootstrap and de-multiplexer
- Use hybrid architecture of sub-ranging and SAR to improve energy efficiency
- $C_{in}=544fF$, $C_u=1fF$
- Status: 3rd gen. test chip under evaluation

<table>
<thead>
<tr>
<th>Measurement Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
</tr>
<tr>
<td>Resolution</td>
</tr>
<tr>
<td>Channel</td>
</tr>
<tr>
<td>Supply voltage</td>
</tr>
<tr>
<td>Conversion rate</td>
</tr>
<tr>
<td>Core Area</td>
</tr>
<tr>
<td>ENOB@Fin=1M</td>
</tr>
<tr>
<td>Power</td>
</tr>
</tbody>
</table>

Hsin-Shu Chen
DC-DC Converter ICs
Operate under a PWM mode during steady state and enables a saturation-mode during transient to attain fast transient response

Optimize the gate-driving voltage by the linearly scaled gate-driving technique for light-load efficiency

Select the frequency hopping instant such that the average inductor current is undisturbed when the switching frequency hops

*IEEE TPE, Vol. 27, No. 11, pp. 4763-4771, Nov. 2012*
- Use a prediction method with early actions to suppress the output voltage ringing, and to mitigate the output voltage overshoot/undershoot.

- Operate under PWM mode during steady state and early switch to the proposed HPVC mode during transient to saturate duty-cycle for fast transient recovery time.

- *IET Transactions on Power Electronics 2016*
A two-input floating buck (TIFB) converter decreases voltage stress to accomplish high power efficiency.

Variable off-time (VOT) control with an on-chip current sensor to achieve high accuracy.

Status: submit to IEEE Journal of Emerging and Selected Topics in Power Electronics
Capacitive DC-DC Converter

- PFM control by using a hysteretic comparator to switch the clock on/off
- Switched capacitor power stage with 2:1 ratio
- Status: 1st gen. test chip under evaluation

**Technology**

<table>
<thead>
<tr>
<th>Technology</th>
<th>40LP</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{in}$</td>
<td>1.8V</td>
</tr>
<tr>
<td>$V_{out}$</td>
<td>0.8~0.85V</td>
</tr>
<tr>
<td>Flying Cap</td>
<td>480pF MOScap 100pF MOMcap 200um x450um</td>
</tr>
<tr>
<td>$V_{ref}$</td>
<td>0.75V</td>
</tr>
<tr>
<td>Clock Freq</td>
<td>1~10M</td>
</tr>
<tr>
<td>Max current loading</td>
<td>0.15mA @ 1MHz 1.2mA @ 10MHz</td>
</tr>
<tr>
<td>Power efficiency</td>
<td>70%</td>
</tr>
<tr>
<td>$C_{out}$ C</td>
<td>2nF</td>
</tr>
<tr>
<td>Core Area</td>
<td>200um x550um</td>
</tr>
</tbody>
</table>

**Core circuit layout**
Power Management Circuits for Energy Harvester System

- Energy harvesting circuits consist of a rectifier AC/DC converter with a switching interfacing circuit, a DC–DC converter and a controller.

- Rectifier AC/DC converter integrates with a switching interfacing circuit of Synchronized Switch Harvesting on Inductor (SSHI)

Status: under construction
Thank You!