Active and Adaptive Charging Method on Data Lines for Delay Compensation

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***Abstract*—Charging time is a critical constraint in the design of large-size or high-resolution liquid crystal display. A fast charging method is proposed to generate adaptive charging voltages by comparing the pixel values between previous and current frames. Data line segmentation is also proposed to charge different subpixels on the data line precisely, which is implemented by using operational amplifiers and resistor networks.**

***Index Terms*—Liquid crystal display (LCD) driver, thin-film transistor (TFT) LCD, display.**

I. Introduction

HIGH-RESOLUTION TV has more rows to charge in one frame time, thus the available charging time for each row is shorter than that for standard TV. The voltage levels on data lines change with the picture content, and such change must be completed during the allocated charging period. If the voltage levels on a data line are significantly different between two consecutive frames, pre-charge method is usually used to shorten the charging time.

In [1], the charging period for a data line is divided into two phases, a voltage higher than needed is applied during the pre-charge phase, then the data voltage is applied during the fine-tune phase. However, when the voltage levels of one pixel in two consecutive frames are close, this pre-charge method may overcharge this pixel. Since the pre-charge voltage is fixed, the fine-tune phase must be long enough if the voltage difference is large.

In [2], the charging period is divided into the pre-charge phase and the fine-tune phase as in [1]. Apply the voltage corresponding to the highest gray level during the pre-charge phase and apply the data voltage during the fine-tune phase. The higher the pixel gray level is, the longer the pre-charge phase takes, and vice versa. Similar to [1], when the previous gray level is significantly different from the current one, the fine-tune may not be complete in time.

In [3], a line time extension method is proposed to extend the equivalent charging time for a pixel. Two adjacent rows are pulled up at the same time. After a charging time of $T_{\rm row}$, the scan line of the first row is pulled down and the data voltage is applied to the second row. This method can effectively extend the charging time. However, if the data on two adjacent rows differ too much, the fine-tune phase may not be sufficient for the second row.

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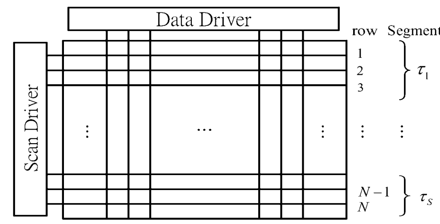

Fig. 1. Segmentation of data lines.

In [4], a frame buffer is used to store the previous frame, and a lookup table is used to generate the overdrive voltage by comparing the previous frame and the current one. This method can charge the pixel faster but not very precisely. In [5], the charging period for a data line is divided into the pre-charge phase and the fine-tune phase, and a lookup table is used to generate the pre-charge voltage. This method has the same drawbacks as [4].

In [6], an overdrive voltage is calculated by using a VGA chip, based on the data line voltages. It has the same drawbacks as conventional overdrive method. The scan-line delay near the scan driver is shorter than that away from it, due to the resistive and capacitive loads contributed by the data lines.

In [7], the panel is split into an upper part and a lower part, with separate data driver serving each part. The signal delay on a data line can thus be reduced by half. This method requires a memory to store one frame of data before sending to the two data drivers.

In these pre-charging methods, the charging period is divided into a pre-charge phase followed by a fine-tune phase. A fixed voltage is applied in the pre-charge phase, and the data voltage is applied in the fine-tune phase. If a buffer is used to store the previous frame, the fine-tune phase can be executed more efficiently with the additional load of computing the voltage difference between two consecutive frames.

In this paper, we propose an active and adaptive charging method to charge the LCD panel fast by comparing the previous and the current frames of data to generate the charging voltage. A resistor network is implemented to compare the voltages sent to the operational amplifier to compensate for the data-line delay at different distances from the data driver.

II. Design Approach

Without loss of generality, a 60'' LCD with full HD resolution of 1920×1080 will be considered throughout this paper. To charge data lines more precisely, a data line serving 1080 subpixels is divided into multiple segments, as shown in Fig. 1.

TABLE I
PARAMETERS OF 40'' FULL HD TFT-LCD [3]

Parameter	Value
resolution	1,920 × 1,080
pixel size (μm^2)	151 × 454
resistance of vertical line (kΩ)	18
capacitance of vertical line (pF)	276
resistance of horizontal line (kΩ)	5
capacitance of horizontal line (pF)	480
pixel capacitance (pF)	1.35
LCD mode	TN

Define the charging ratio as the ratio between the charged voltage and the intended voltage. For example, if the intended voltage at a pixel is 6 V and the pixel voltage reaches 5.5 V at the end of the charging period, the charging ratio will be $5.5/6 = 0.917$.

Based on the signal line model consisted of infinitesimal RC segments, the voltage waveform on a data line or a scan line can be expressed as

$$\frac{v(z,t)}{V_d} \simeq 1 - \frac{4}{\pi} \exp\left(-\frac{\pi^2 t}{4RCz^2}\right) \quad (1)$$

where R and C are the per-unit-length resistance and capacitance, respectively, along the line, V_d is the intended voltage, and $v(z,t)$ is the voltage on the line at time t and at a distance z from the source. To reach the charging ratio of 0.995, the delay time will be $T_{0.995} = 2.245RCz^2$.

In general, the delay time for the voltage at z to reach the charging ratio α is approximately

$$T_\alpha(z) = -\frac{4RCz^2}{\pi^2} \ln \frac{\pi(1-\alpha)}{4}. \quad (2)$$

Since the signal line can be viewed as a cascade of infinitesimal resistive and capacitive loads, the signal line from the driver at $z = 0$ to any subpixel location z can be modeled as an equivalent RC circuit with an effective time constant $\tau_\alpha(z)$ which can be expressed in terms of $T_\alpha(z)$ as

$$\tau_\alpha(z) = \frac{T_\alpha(z)}{-\ln(1-\alpha)} = \frac{4RCz^2}{\pi^2 \ln(1-\alpha)} \ln \frac{\pi(1-\alpha)}{4}. \quad (3)$$

Since no data of line resistance and capacitance are available for a 60'' LCD panel with full HD resolution, we assume the per-unit-length resistance and capacitance of the 60'' LCD panel are the same as those of the 40'' LCD panel. Table I lists the parameters of a 40'' TFT-LCD with full HD resolution. The length of a scan line is $\ell = 1\,920 \times 151\mu \times 3 = 86.976$ cm, hence $R = 5/0.86976 = 5.7487$ kΩ/m, $C = 480/0.86976 = 551.876$ pF/m. The length of a data line is $\ell = 1\,080 \times 454\ \mu = 49.032$ cm, hence, $R = 18/0.49032 = 36.71$ kΩ/m, and $C = 276/0.49032 = 562.897$ pF/m.

Fig. 2(a) and (b) shows the delay time $T_\alpha(z)$ and the effective time constants $\tau_\alpha(z)$, respectively, at different charging ratios.

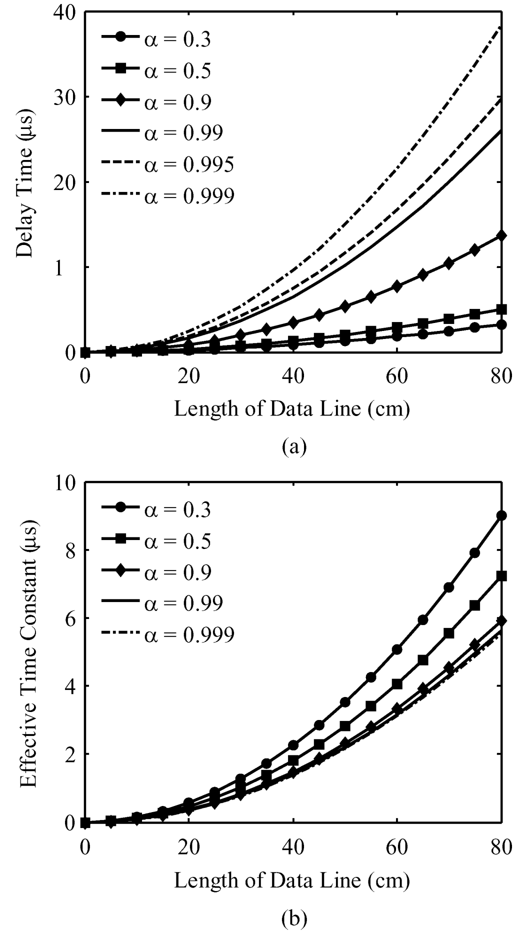

Fig. 2. (a) Delay time T_α and (b) effective time constant τ_α, along a data line.

It is observed that $\tau_\alpha(z)$ is insensitive to α, especially when α is closed to unity. In practical applications, the value of α is chosen to be greater than 0.995 to have high fidelity. Thus, we may set $\tau_\alpha(z) = \tau(z)$.

The time allocated for displaying each row is

$$T_{\text{row}} = \frac{1}{\text{frame rate}} \times \frac{1}{\text{number of rows}} \times (1 - \alpha_{\text{sync}})$$

where α_{sync} is the fraction of time reserved for horizontal sync. When the data line is being charged, the transistors on the designated row must be turned on by sending a pulse along the associated scan line. The pixels will wait for $t_{\text{d,scan}}$ before the pulse arrives, where $t_{\text{d,scan}}$ is the delay on scan line which can be calculated using (2). Note that $t_{\text{d,scan}}$ of the farthest pixel from the scan driver must be shorter than T_{row} to have enough margin. Since the loading effect of a single pixel on a data line is negligible, the available charging time is $T_{\text{charge}} = T_{\text{row}}$.

The signal delay is longer for those subpixels which are farther from the data driver, and is shorter for those which are closer to the data driver. The effective time constant for the subpixels in segment s can be approximated by a constant τ_s at certain point $z = \ell_s$ in segment s at which the voltage waveform is

$$v_s(t) = [v_s(\infty) - v_s(0+)](1 - e^{-t/\tau_s}) + v_s(0+) \quad (4)$$

where $v_s(t)$ is the voltage at time t, $v_s(\infty)$ is the intended voltage, and $v_s(0+)$ is the initial voltage.

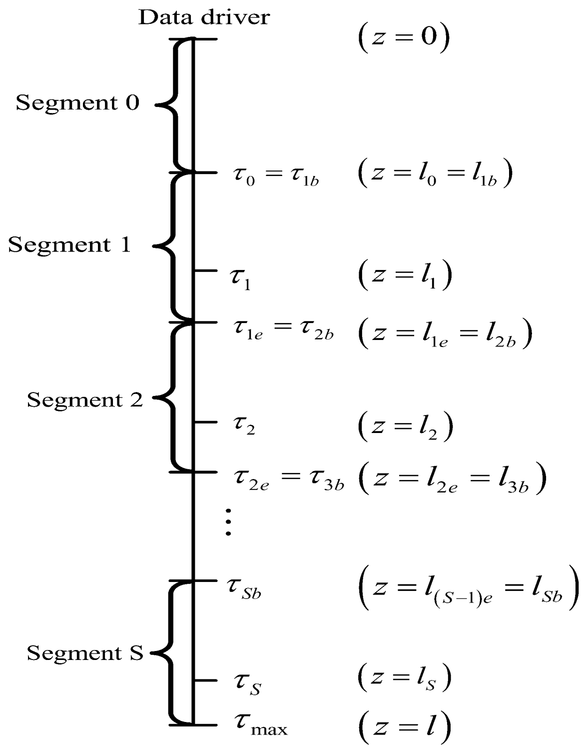

Fig. 3. Segmentation plan of a data line.

Fig. 3 shows the segmentation plan of a data line. Segment $0(0 \le z \le \ell_0)$ is close enough to the data drive so that no active charging is required. Segment $1(\ell_{1b} \le z \le \ell_{1e})$ lies next to segment 0 so that $\ell_{1b} = \ell_0$. The effective time constant in segment 1 is approximated as a constant τ_1 for the ease of implementation. The value of τ_1 is chosen so that the voltage level at $t = T_{\text{charge}}$ at $z = \ell_{1b}$ is $1-\alpha$ above the intended level. The other end point $z = \ell_{1e}$ is chosen so that its voltage level at $t = T_{\text{charge}}$ is $1-\alpha$ below the intended level. The parameters in the next segment are then determined in the same way.

The applied voltage $v_{\text{d,amp}}$ is determined by letting $v_s(T_{\text{charge}}) = v_{\text{d,now}}$, $v_s(\infty) = v_{\text{d,amp}}$, $v_s(0+) = v_{\text{d,pre}}$ in (4) to have

$$v_{\text{d,amp}} = \frac{1}{1-e^{-T_{\text{charge}}/\tau_s}} v_{\text{d,now}} - \frac{e^{-T_{\text{charge}}/\tau_s}}{1-e^{-T_{\text{charge}}/\tau_s}} v_{\text{d,pre}} \tag{5}$$

where $v_{\text{d,pre}}$ and $v_{\text{d,now}}$ are the voltage levels of the previous and the current frames, respectively. The subpixel at $z = \ell_s$ reaches the charging ratio of exactly 100% at $t = T_{\text{charge}}$.

The data line from $z = 0$ to $z = \ell_0$ does not require active charging because its voltage level can exceed the specified charging ratio α at T_{charge}. To find the time constant τ_0 at $z = \ell_0$, let

$$\Delta V(1-e^{-T_{\text{charge}}/\tau_0}) = \alpha \Delta V$$

or

$$\tau_0 = \frac{-T_{\text{charge}}}{\ln(1-\alpha)} \tag{6}$$

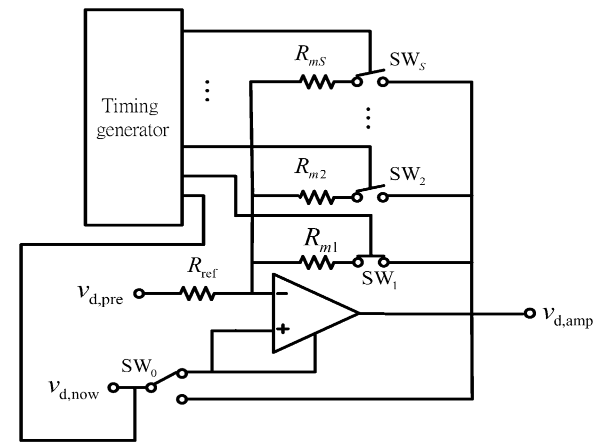

Fig. 4. Operational amplifier with resistor network and switches for data line m.

where ΔV is the difference of voltage between two consecutive frames.

At the specified charging ratio α, the maximum allowable deviation of voltage level in segment s occurs at both ends, $z = \ell_{sb}$ and $z = \ell_{se}$. At $z = \ell_{sb}$, the voltage level is $(1-\alpha)\Delta V$ too high, namely,

$$(v_{\text{d,amp}} - v_{\text{d,pre}})(1-e^{-T_{\text{charge}}/\tau_{sb}}) - \Delta V = (1-\alpha)\Delta V$$

or

$$\tau_s = \frac{-T_{\text{charge}}}{\ln\left(\frac{1-\alpha+e^{-T_{\text{charge}}/\tau_{sb}}}{2-\alpha}\right)}. \tag{7}$$

At $z = \ell_{se}$, the voltage level is $(1-\alpha)\Delta V$ too low, namely,

$$\Delta V - (v_{\text{d,amp}} - v_{\text{d,pre}})(1-e^{-T_{\text{charge}}/\tau_{se}}) = (1-\alpha)\Delta V$$

or

$$\tau_{se} = \frac{-T_{\text{charge}}}{\ln(1-\alpha+\alpha e^{-T_{\text{charge}}/\tau_s})}. \tag{8}$$

To determine the parameters in Fig. 3, first calculate τ_0 using (6), then calculate τ_1 by setting $s = 1$ and $\tau_{1b} = \tau_0$ in (7), τ_{1e} is then obtained from (8) by setting $s = 1$, and so on. Based on (3), the distance from the data driver is related to τ as

$$z = \sqrt{\frac{\tau(z)\pi^2 \ln(1-\alpha)}{4RC \ln \frac{\pi(1-\alpha)}{4}}}.$$

Fig. 4 shows the circuit of an operational amplifier to generate the voltage $v_{\text{d,amp}}$. A resistor network is required to implement the S sets of coefficients in (5). When switch SW_s is closed, the output voltage on data line m becomes

$$v_{\text{d,amp}} = v_{\text{d,now}}\left(1+\frac{R_s}{R_{\text{ref}}}\right) - v_{\text{d,pre}}\frac{R_s}{R_{\text{ref}}}. \tag{9}$$

By comparing (9) and (5), the resistance R_{ms} can be determined as

$$\frac{R_{\text{ref}}}{R_s} = \frac{1-e^{-T_{\text{charge}}/\tau_s}}{e^{-T_{\text{charge}}/\tau_s}} = e^{T_{\text{charge}}/\tau_s} - 1. \tag{10}$$

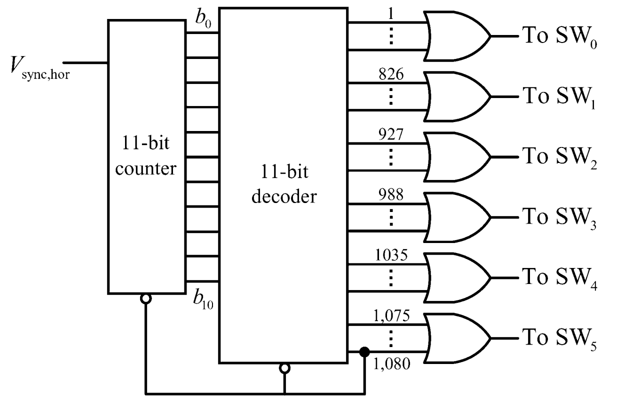

Fig. 5. Timing generator which is reset when scan line 1 080 is on, and changes switch when scan line 826, 927, 988, 1035, or 1075 is on.

Fig. 5 shows the circuit of timing generator designed to change switches in the circuit of Fig. 4 to fulfill the charging ratio of 0.995 for a 60'' LCD panel with full HD resolution. In this case, the pixels from rows 1 to 825 do not need active charging, thus the data voltage is sent via SW_0 to the data line. In charging the pixels from rows 826 to 926, the data voltage is sent via SW_1, and the output voltage is determined by resistance R_1 and R_{ref} as in (9), and so on.

Fig. 6 shows the driver circuit with a frame buffer to charge data lines. The data in the previous frame is stored in the buffer to be compared with the data in the current frame to calculate the voltage to be sent to the data lines.

Each time a rising edge of $V_{\mathrm{sync,hor}}$ arrives, the first stage of latch layer 1 receives one subpixel data of the current frame, and the first stage of latch layer 2 receives the subpixel data of the previous frame from the frame buffer. When the next $V_{\mathrm{sync,hor}}$ arrives, the second stage of latch layer 1 will receive the first row of data of the current frame, and the second stage of the latch layer 2 will receive the first row of data of the previous frame. The data stored in these stages are then sent to DAC 1 and DAC 2, respectively, to be transformed to the voltage inputs for the operational amplifiers to determine the output voltages for all the data lines.

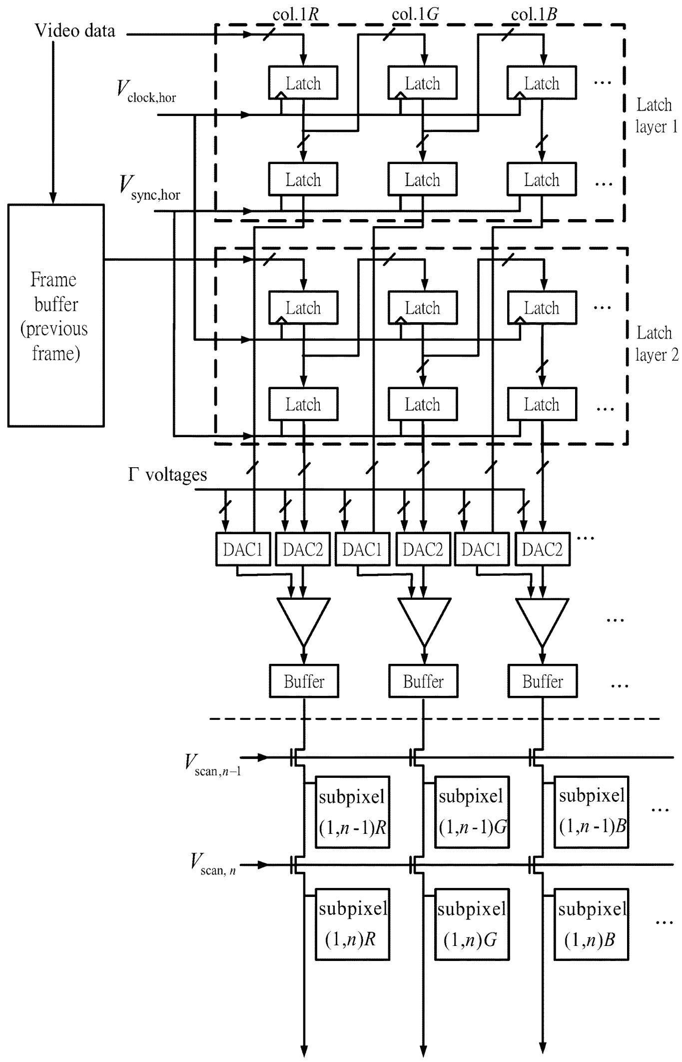

Fig. 6. Active charging circuit on data lines with frame buffer.

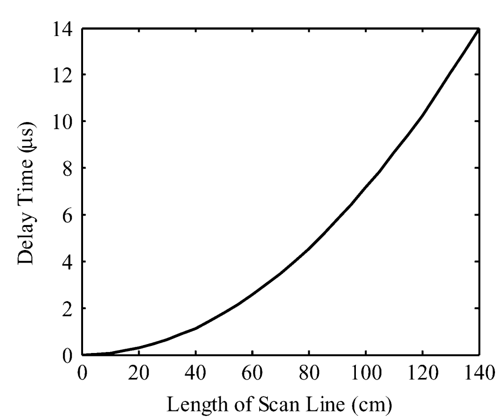

Fig. 7. Delay time on scan line with $\alpha = 0.995$.

III. Design Examples

In the standard HDTV, the frame rate is 60 Hz, thus the frame period is $1/60 = 16.67$ ms. With resolution $1\ 920 \times 1\ 080$, each row is allocated a period $T_{\mathrm{row}} = (1/60/1\ 080) \times 0.95 = 14.67\ \mu$s, where $\alpha_{\mathrm{sync}} = 0.05$.

Fig. 7 shows the delay time on the scan line with the charging ratio $\alpha = 0.995$. Based on (2), the maximum delay time on a scan line at the charging ratio of 0.995 is about 14 μs, too close to $T_{\mathrm{row}} = 14.67\ \mu$s. If both ends of the scan line are driven simultaneously by the scan driver, then the maximum scan-line delay of about 4.4 μs will occur at the middle of the scan line, thus the delay time along the scan line will not prevent any pixel from being turned on early enough.

If the LCD is changed from white to black, the data voltage is changed from 0 to 6 V, rendering $\Delta V = 6$ V. By using conventional method, the voltage on the last subpixel of each data line can only reach 5.7 V at 14.67 μs, which accounts to 13 gray levels of error. On the other hand, the active charging voltage to charge a subpixel from 0 to 6 V is 6.306 V, and the voltage on the subpixel reaches 5.99 V at 14.67 μs, with the error of 0.413 gray level.

Table II lists the effective time constant and the subpixel range of each segment at the charging ratio of 0.995. Applying the segmentation plan, each data line is divided into six segments, and

TABLE II
PARAMETERS OF SEGMENTS AT CHARGING RATIO OF 0.995

Segment	τ_s (μs)	$R_{\rm ref}/R_s$	Subpixel
0	–	–	$1 \sim 825$
1	3.1821	99.501	$826 \sim 926$
2	3.7404	49.502	$927 \sim 987$
3	4.1658	32.836	$988 \sim 1,034$
4	4.5295	24.503	$1,035 \sim 1,074$
5	4.8566	19.504	$1,075 \sim 1,080$

TABLE III
SEGMENTATION OF SUBPIXELS ALONG A DATA LINE

Segment	$\alpha = 0.99$	$\alpha = 0.995$	$\alpha = 0.999$
0	$1 \sim 882$	$1 \sim 825$	$1 \sim 726$
1	$883 \sim 1,009$	$826 \sim 926$	$727 \sim 792$
2	$1,010 \sim 1,080$	$927 \sim 987$	$793 \sim 829$
3	–	$988 \sim 1,034$	$830 \sim 856$
4	–	$1,035 \sim 1,074$	$857 \sim 879$
5	–	$1,075 \sim 1,080$	$880 \sim 898$
6	–	–	$899 \sim 915$
7	–	–	$916 \sim 930$
8	–	–	$931 \sim 944$
9	–	–	$945 \sim 957$
10	–	–	$958 \sim 970$
11	–	–	$971 \sim 981$
12	–	–	$982 \sim 992$
13	–	–	$993 \sim 1,002$
14	–	–	$1,003 \sim 1,012$
15	–	–	$1,013 \sim 1,022$
16	–	–	$1,023 \sim 1,031$
17	–	–	$1,032 \sim 1,040$
18	–	–	$1,041 \sim 1,048$
19	–	–	$1,049 \sim 1,056$
20	–	–	$1,057 \sim 1,065$
21	–	–	$1,066 \sim 1,072$
22	–	–	$1,073 \sim 1,080$

the resistance ratios are determined using (10). The switches are controlled by the timing generator shown in Fig. 5. The counter counts from 1 to 1 080 repeatedly, triggered by $V_{\rm sync,hor}$. When the counter counts from 1 to 825, $\rm SW_0$ is closed, no active charging is exerted. When counting from 826 to 926, $\rm SW_1$ is closed, rendering $\tau_1 = 3.1821\ \mu$s for segment 1, and so on.

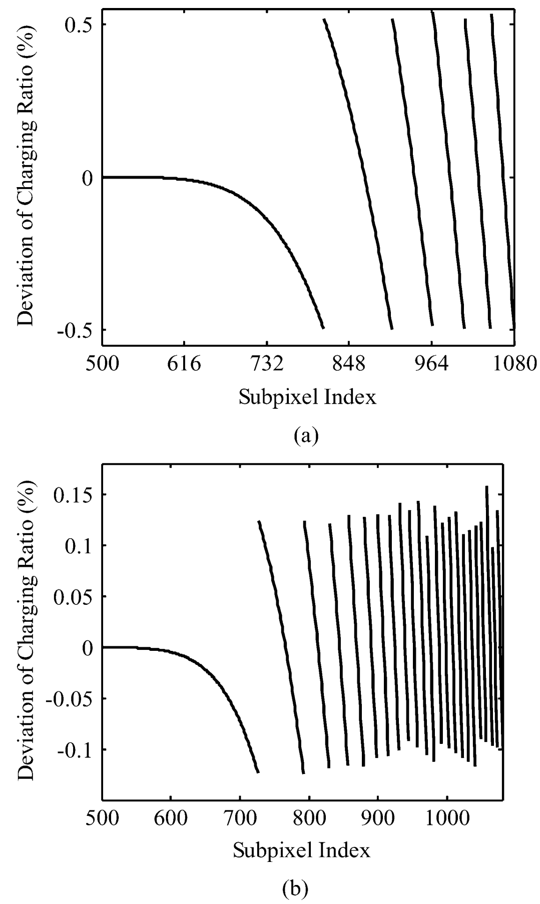

Fig. 8. Deviation of charging ratio along a data line. (a) $\alpha = 0.995$. (b) $\alpha = 0.999$.

Table III lists the segmentation of subpixels along a data line at different charging ratios. At higher charging ratio, more segments are required, and the number of subpixels in each segment is reduced. The number of subpixels in a segment farther away from the driver is smaller than that in a segment closer to the driver.

Fig. 8 shows the deviation of charging ratio along a data line at $\alpha = 0.995$ and $\alpha = 0.999$, which are less than 0.5% and 0.15%, respectively. LCDs are voltage-sensitive display. For voltage error greater than 5 mV, the transmittance difference could be visible. To overcome this problem, a higher value of charging ratio α is suggested. The segmentation plans associated with Fig. 8(a) and (b) is designed based on the voltage error within 25 and 5 mV, respectively.

For LCD in MVA or IPS mode, the voltage swing sometimes can reach 10 V. Considering the inversion feature of LCD, the magnitude of one gray level is about 23 mV. To reduce the error to within one gray level, the charging ratio must be greater than 0.999, and 23 switches are needed for each operational amplifier.

Fig. 9 shows the resistance associated with the resistor networks at different charging ratios. The range of resistance is wider at larger charging ratio.

Fig. 10 shows the relation between the panel size and the number of segments required to reach $\alpha = 0.995$. The number

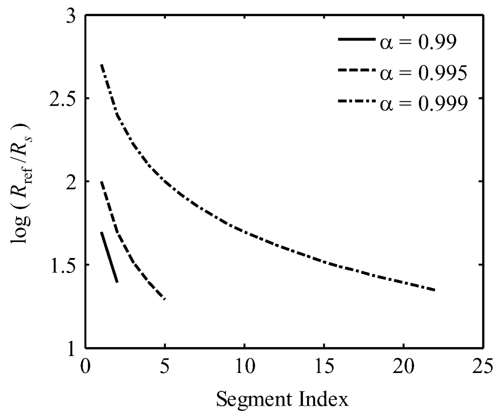

Fig. 9. Resistance of resistor network.

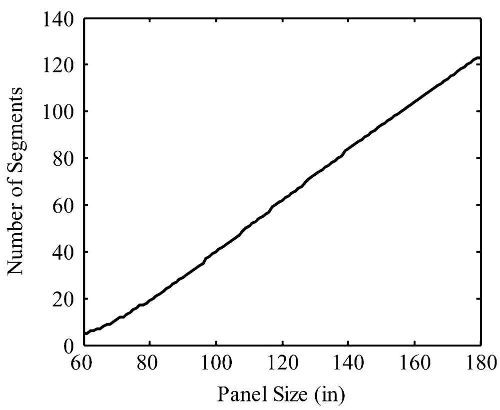

Fig. 10. Number of segments required for different panel sizes at $\alpha = 0.995$.

of segments increases linearly with the panel size. For example, the numbers of segments for 60'', 80'', and 160'' panels are 6, 20, and 105, respectively. For the large one like 160'' panel, two data drivers may be considered to drive the data line from opposite ends, and the total number of segments can be reduced to about 40.

IV. Conclusion

An active charging method for large-size or high-resolution LCD is proposed. In this method, the data between adjacent frames are compared, different effective time constants at different locations on a data line are considered to generate the precise active charging voltage at the given charging ratio. Compared to conventional method, this method can charge large-size panel more precisely within the charging time.

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