Charge Recycling Method on Pixel Level

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***Abstract*—A new power-saving design using charge recycling technique on the pixel level is proposed. Design constraints are derived and design examples are demonstrated. Compared with conventional charging methods, this method consumes only half the power, the charging speed is faster and the aperture ratio is similar.**

***Index Terms*—Liquid crystal display (LCD), power consumption, thin-film transistor (TFT).**

I. Introduction

ERHART and McCartney proposed a charge conservation method in 1997 by using additional switches to recycle the charge between two adjacent data lines in the column inversion or dot inversion modes [1]–[3]. In 1998, Kwon proposed similar designs for the data driver and the gate driver, respectively [4], [5]. A fraction of time allocated for charging the pixels will be deducted by conducting the charge-recycling process.

Kim proposed a multilevel multiphase charge-recycling method in 2000 [6]. Several external capacitors charged at different voltage levels are used to recycle the charge on the data lines. This method demands a time budget to move the charge around, and the power saved is less than 50%. In the field sequential color (FSC) liquid crystal displays (LCDs), the allocated charging time is one-third that of the color filter (CF) LCDs, and the pixel size of the former is three times that of the latter. Thus, the charging time becomes more critical in the FSC LCDs, and all these methods will face tougher challenges.

Lay proposed a power-saving method by using an additional recycling thin-film transistor (TFT) to connect two adjacent electrodes [7]. In the dot-inversion or column-inversion mode, the gate of the additional TFT is connected to an adjacent scan line, its drain and source electrodes are connected to two adjacent pixels in the same row, respectively, to recycle the charge between these two pixels.

In this paper, a new design is proposed, in which the ground instead of an external capacitor at the drvier end serves as the charge reservoir to reduce the power consumption without deducting the charging time. In Section II, the circuit models of the subpixel and the signal line are described. In Section III, the constraints on subpixel design are derived. A dual TFT method is proposed in Section IV and demonstrated in Section V, followed by the conclusion.

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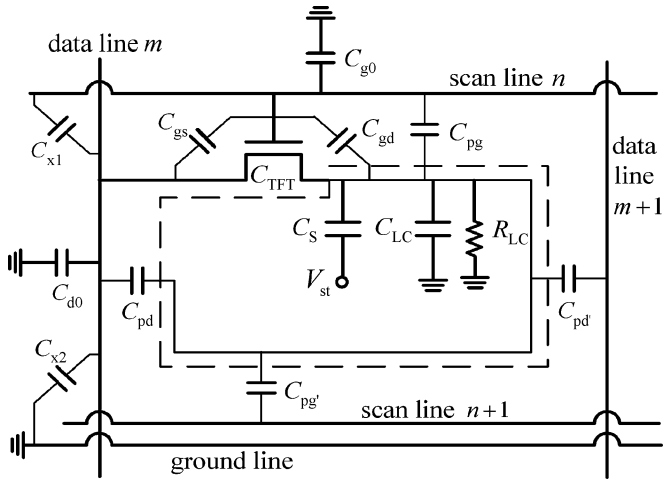

Fig. 1. Equivalent circuit of a subpixel.

II. Circuit Models of Pixel and Signal Line

Fig. 1 shows the equivalent circuit of a subpixel, where $C_{\rm LC}$ and $R_{\rm LC}$ are the capacitance and resistance, respectively, of the subpixel between the ITO and the common electrode [8]–[10], $C_{\rm x1}$ is the capacitance between data line m and scan line n, $C_{\rm x2}$ is the capacitance between data line m and the ground line, $C_{\rm g0}$ is the capacitance between scan line n and the common electrode, and $C_{\rm d0}$ is the capacitance between data line m and the common electrode. Around the TFT, $C_{\rm gs}$ is the capacitance between the gate and the source electrodes, $C_{\rm gd}$ is the capacitance between the gate and the drain electrodes, and $C_{\rm TFT}$ is the capacitance between the gate electrode and the conducting layer of TFT. The storage capacitor C_S is connected between the ITO and metal layer 1, $C_{\rm pg}$, $C_{\rm pg'}$, $C_{\rm pd}$, and $C_{\rm pd'}$ are the capacitances between the display electrode and scan line n, scan line $n+1$, data line m, and data line $m+1$, respectively. The total resistance of a subpixel can be calculated as

$$R_{\rm px} = \frac{R_{\rm off} R_{\rm LC}}{R_{\rm off} + R_{\rm LC}}$$

where $R_{\rm LC}$ is the resistance of the liquid crystal part, and $R_{\rm off}$ is the off-resistance of the TFT. The subpxiel capacitance can be approximated as

$$C_{\rm px} \simeq C_S + C_{\rm LC} \tag{1}$$

where the parasitic capacitances $C_{\rm gd}$, $C_{\rm pd'}$, $C_{\rm pd}$, $C_{\rm pg'}$, and $C_{\rm pg}$ are assumed much smaller than C_S and $C_{\rm LC}$. In this paper, a 30″ WXGA LCD screen will be used as a benchmark for discussion, with typical values $C_S = 9.63$ pF, $C_{\rm LC} = 1.74$ pF, and $C_{\rm px} = 11.37$ pF.

To estimate the loading effect of a subpixel on scan line n, first calculate the equivalent resistance of a scan line across a subpixel as [11], [12]

$$R_{\rm scan} = \rho_{\rm scan}\frac{L_{\rm scan}}{A_{\rm scan}}$$

where $A_{\rm scan} = t_{\rm scan} \times W_{\rm scan}$ is the cross-sectional area of the scan line, $\rho_{\rm scan}$, $W_{\rm scan}$, and $t_{\rm scan}$ are the resistivity, width and thickness, respectively, of the scan line, $L_{\rm scan}$ is the length of the scan line across a subpixel. The capacitive load of a subpixel on the scan line is approximated as

$$C_{\rm scan} \simeq C_{\rm gs} + C_{\rm TFT} + C_{\rm g0} + C_{\rm x1} + C_{\rm gd} + C_{\rm pg} + C_{\rm pg'}. \quad (2)$$

Next, to consider the loading effect of a subpixel on a data line, the equivalent resistance $R_{\rm data}$ can be calculated as

$$R_{\rm data} = \rho_{\rm data}\frac{L_{\rm data}}{A_{\rm data}}$$

where $A_{\rm data} = t_{\rm data} \times W_{\rm data}$ is the cross-sectional area of the data line, $\rho_{\rm data}$, $W_{\rm data}$ and $t_{\rm data}$ are the resistivity, width and thickness, respectively, of the data line, and $L_{\rm data}$ is the length of the data line across a subpixel. The capacitive load of a subpixel on the data line can be approximated as

$$C_{\rm data} \simeq C_{\rm x1} + C_{\rm x2} + C_{\rm d0} + C_{\rm gs} + C_{\rm pd'} + C_{\rm pd}. \quad (3)$$

In the 30″ WXGA LCD, $L_{\rm scan} = 162\ \mu$m, $L_{\rm data} = 486\ \mu$m. Typical copper process is used with $\rho_{\rm scan} = \rho_{\rm data} = 1.68\ \mu\Omega-$cm, $W_{\rm scan} = 20\ \mu$m, $W_{\rm data} = 10\ \mu$m, $t_{\rm scan} = 300$ nm and $t_{\rm data} = 200$ nm, hence $R_{\rm scan} = 0.454\ \Omega$ and $R_{\rm data} = 2.72\ \Omega$. Typical values of capacitances are $C_{\rm x1} = 41$ fF, $C_{\rm x2} = 20$ fF, $C_{\rm g0} = 71$ fF, $C_{\rm d0} = 107$ fF, $C_{\rm gs} = C_{\rm gd} = 10$ fF, $C_{\rm TFT} = 37$ fF, $C_{\rm pg} = C_{\rm pg'} = 0.6$ fF, and $C_{\rm pd} = C_{\rm pd'} = 1.8$ fF.

Fig. 2 shows a lossy transmission line model to analyze signal delay along data lines and scan lines. The signal line can be decomposed into infinitesimal segments of length Δz, with resistance $R\Delta z$ and shunt capacitance $C\Delta z$ over each segment, the series inductance $L\Delta z$ and shunt conductance $G\Delta z$ are neglected. The equations governing the distribution of current and voltage along the line are

$$\frac{\partial v}{\partial z} = -Ri \text{ and } \frac{\partial i}{\partial z} = -C\frac{\partial v}{\partial t}$$

which can be solved by applying the Laplace transform, with the boundary conditions

$$V(s,0) = F(s), \quad I(s,\ell) = 0$$

where $F(s)$ is the Laplace transform of the driving voltage waveform $f(t)$ at $z = 0$. Assume the signal line has a finite length ℓ and is open circuited at the load end $z = \ell$ [8], and the driving voltage is a step function of time, namely, $F(s) = V_g/s$, then the waveform at $z = \ell$ can be calculated as

$$\frac{v(\ell,t)}{V_g} = 1 + \frac{4}{\pi}\sum_{n=1}^{\infty}\left\{\frac{(-1)^n}{2n-1}\exp\left[-\frac{(2n-1)^2\pi^2}{4RC\ell^2}t\right]\right\}. \quad (4)$$

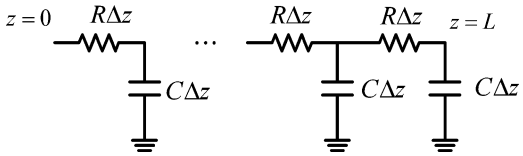

Fig. 2. Signal line modeled as a cascade of infinitesimal RC segments.

When $t > RC\ell^2$, (4) can be approximated as

$$\frac{v(\ell,t)}{V_g} \simeq 1 - \frac{4}{\pi}\exp\left(-\frac{\pi^2 t}{4RC\ell^2}\right).$$

The delay time for $v(\ell,t)$ to reach $v(\ell,t)/V_g = 90\%$ is $1.03RC\ell^2$ [8].

III. Constraints on Subpixel Design

The charge current of TFT can be expressed as [9]

$$i = \beta_0\left[(V_s - V_t - V_D)(V_d - V_e) - \frac{1}{2}(V_d - V_e)^2\right]$$

where $\beta_0 = \mu_{\rm eff}C_gW/L$ is a parameter determined by the TFT geometry and material. As shown in Fig. 1, the voltage V_e at the display electrode, or at the junction of TFT and $C_{\rm LC}$, is a function of the data line voltage V_d as [14]

$$V_e = \frac{1 - ae^{-t/\tau}}{1 - be^{-t/\tau}}V_d \quad (5)$$

with

$$\begin{aligned} a &= \frac{V_d - V_{e0}}{V_d}\frac{2(V_s - V_t - V_d) + V_d}{2(V_s - V_t - V_d) + V_d - V_{e0}} \\ b &= \frac{V_d - V_{e0}}{2(V_s - V_t - V_d) + V_d - V_{e0}} \\ \tau &= \frac{C_{\rm px}}{\beta_0(V_s - V_t - V_d)} \end{aligned} \quad (6)$$

where V_s is the voltage on the scan line, V_t is the threshold voltage of the TFT, V_{e0} is the voltage of V_e at $t = 0$, W and L are the channel width and length, respectively, of the TFT. With $V_s = 40$ V, $V_t = 0.7$ V and $V_d = 2.5$ V, typical values of the parameters in (6) are $\mu_{\rm eff} = 1.5 \times 10^{-5}\ {\rm m}^2/{\rm V}\cdot{\rm s}$, $C_g = 2 \times 10^{-4}$ F/m^2, $a = 1.94$, $b = 0.064$, and $\tau = 5\ \mu$s.

A. Charging Phase

In the charging phase, express the rising time t_r in units of τ as $t_r = k_t\tau$, and define the voltage ratio $r_c = V_e/V_d$. Thus k_t can be expressed as

$$k_t = \ln\frac{a - br_c}{1 - r_c}.$$

Typically, $r_c = 0.99$ and $k_t = 2.93$. The rising time must be shorter than the time budget allocated for displaying one row, deducting the delay over the scan line or the data line, namely,

$$t_r < T_{\rm row} - T_{\rm delay}$$

where $T_{\rm delay}$ is the longer of the allowable delay time over a data line and that over a scan line. For the 30″ WXGA LCDs, $T_{\rm delay} = 1.7\ \mu$s. Thus, we have

$$\frac{W}{L} > \frac{C_{\rm px}}{\mu_{\rm eff} C_g (V_s - V_t - V_d)} \frac{k_t}{(T_{\rm row} - T_{\rm delay})}. \tag{7}$$

The resolution of the 30″ WXGA LCDs is 1366×768, which means $N_{\rm scan} = 768$, $N_{\rm data} = 1366 \times 3$, and $T_{\rm row} = 21.7\ \mu$s, thus the lower bound in (7) becomes 15.

B. Holding Phase

In the holding phase, the charge leaks through the equivalent RC circuit formed by $R_{\rm LC}$, $R_{\rm off}$, and $C_{\rm px}$, where $R_{\rm off} = V_{ed}/I_{\rm off}$ is the off-resistance of the TFT with $V_{ed} = V_e - V_d$ [12]. The RC time constant of the subpixel is

$$\tau_{\rm px} = \frac{R_{\rm LC} R_{\rm off}}{R_{\rm LC} + R_{\rm off}} C_{\rm px}. \tag{8}$$

The leakage current $I_{\rm off}$ can be expressed as [12]

$$I_{\rm off} \simeq \frac{\sigma_{\rm D} t_{\rm semi} V_{ed} W}{L}$$

where $\sigma_{\rm D}$ and $t_{\rm semi}$ are the dark conductivity and thickness, respectively, of the semicoductor layer. Typical values are $\sigma_{\rm D} = 10^{-7}$ S/m, $t_{\rm semi} = 50$ nm, $R_{\rm LC} = 6 \times 10^{12}\ \Omega$, $R_{\rm off} = 10^{13}\ \Omega$, hence, $\tau_{\rm px} = 42$ s.

Define the retention ratio in the holding phase as

$$r = e^{-T_{\rm frame}/\tau_{\rm px}}.$$

If $\tau_{\rm px} \gg T_{\rm frame}$, the retention ratio can be approximated as

$$r \simeq 1 - \frac{T_{\rm frame}}{\tau_{\rm px}} \tag{9}$$

To show no image distortion, the error voltage due to leakage must be less than one grey level, namely,

$$r > 1 - \frac{1}{2^{N_{\rm bit}}} \tag{10}$$

where $N_{\rm bit}$ is the number of bits. For WXGA LCDs, $N_{\rm bit} = 8$ and 256 grey levels are available. Substituting (8) and (9) into (10), we obtain another constraint

$$\frac{W}{L} < \left(\frac{C_{\rm px}}{T_{\rm frame} 2^{N_{\rm bit}}} - \frac{1}{R_{\rm LC}} \right) / \sigma_{\rm D} t_{\rm semi}. \tag{11}$$

Since $\frac{1}{R_{\rm LC}} \ll \frac{C_{\rm px}}{T_{\rm frame} 2^{N_{\rm bit}}}$, (11) can be further reduced to

$$\frac{W}{L} < \frac{C_{\rm px}}{T_{\rm frame} 2^{N_{\rm bit}} \sigma_{\rm D} t_{\rm semi}}. \tag{12}$$

With $T_{\rm frame} = 16.7$ ms, the upper bound in (12) is 143.

C. Asymmetric Kickback

When a TFT is switched from one state to another, a kickback voltage

$$\Delta V_{\rm kb} = |v_{s,\rm on} - v_{s,\rm off}| \frac{C_{\rm gd}}{C_{\rm gd} + C_{\rm LC}(V_e) + C_S}$$

will appear at the display electrode, where $v_{s,\rm on}$ and $v_{s,\rm off}$ are the voltages on the scan line at the on and off states, respectively, and $C_{\rm LC}(V_e)$ is the capacitance across the liquid crystal area of a subpixel. The average of kickback voltage can be reduced by adjusting the voltage level of the common electrode on the color-filter substrate, but the voltage deviation $\Delta(\Delta V_{\rm kb})$ will induce a residual direct current with a preferred polarity, which will degrade the quality of liquid crystal. The deviation of $\Delta V_{\rm kb}$ is defined as

$$\begin{aligned} \Delta(\Delta V_{\rm kb}) &= \frac{\Delta V_{\rm kb,max} - \Delta V_{\rm kb,min}}{2} \\ &= \frac{|v_{s,\rm on} - v_{s,\rm off}| C_{\rm gd} (C_{\rm LC,max} - C_{\rm LC,min})}{2(C_{\rm gd} + C_{\rm LC,min} + C_S)(C_{\rm gd} + C_{\rm LC,max} + C_S)}. \end{aligned} \tag{13}$$

Let $\Delta(\Delta V_{\rm kb})$ be constrained by an acceptable residual voltage $F_{\rm kb}$ [11]

$$\Delta(\Delta V_{\rm kb}) < F_{\rm kb}. \tag{14}$$

The capacitance $C_{\rm gd}$ can be expressed in terms of $\tilde{C}_{\rm gd}$, the gate-to-drain capacitance per unit channel width, as

$$C_{\rm gd} = \tilde{C}_{\rm gd} W. \tag{15}$$

Substituting (13) and (15) into (14), we obtain the design constraint based on the asymmetric kickback voltage as

$$W < \frac{2(C_{\rm LC,min} + C_S)(C_{\rm LC,max} + C_S) F_{\rm kb}}{|v_{s,\rm on} - v_{s,\rm off}| \tilde{C}_{\rm gd} (C_{\rm LC,max} - C_{\rm LC,min})}. \tag{16}$$

With typical values of $C_{\rm LC,min} = 0.56$ pF, $C_{\rm LC,max} = 1.74$ pF, $F_{\rm kb} = 0.1$ V, $v_{s,\rm on} = 40$ V, $v_{s,\rm off} = -5$ V and $\tilde{C}_{\rm gd} = 170$ pF/m, the upper bound in (16) is 2.6 mm, too large to be exceeded in practice.

D. Delay

To consider the delay along a scan line, first define $R = R_{\rm scan}/L_{\rm scan}$, $C = C_{\rm scan}/L_{\rm scan}$, and $\ell = N_{\rm data} L_{\rm scan}$, where $N_{\rm data}$ is the number of subpixels along a scan line for CF LCDs or the number of pixels along a scan line for FSC LCDs. The gate delay $t_{\rm d,scan}$ at the end of a scan line with the voltage reaching 90% of its intended level can be estimated as

$$t_{\rm d,scan} = 1.03 N_{\rm data}^2 R_{\rm scan} C_{\rm scan}. \tag{17}$$

This gate delay must be shorter than $T_{\rm delay}$, namely,

$$t_{\rm d,scan} < T_{\rm delay}. \tag{18}$$

Substituting (2) and (17) into (18), we obtain another constraint on the gate width W as

$$W < \frac{(T_{\rm delay}/1.03 N_{\rm data}^2 R_{\rm scan}) - (C_{\rm g0} + C_{\rm x1} + C_{\rm pg} + C_{\rm pg'})}{2\tilde{C}_{\rm gd} + \epsilon_{\rm insu} \epsilon_0 L / t_{\rm insu}} \tag{19}$$

where $C_{\rm gs} \simeq C_{\rm gd} = \tilde{C}_{\rm gd} W$ and $C_{\rm TFT} = \epsilon_{\rm insu} \epsilon_0 W L / t_{\rm insu}$. Typical value of channel length is $L = 3\ \mu$m and $\epsilon_{\rm insu} = 6.9$,

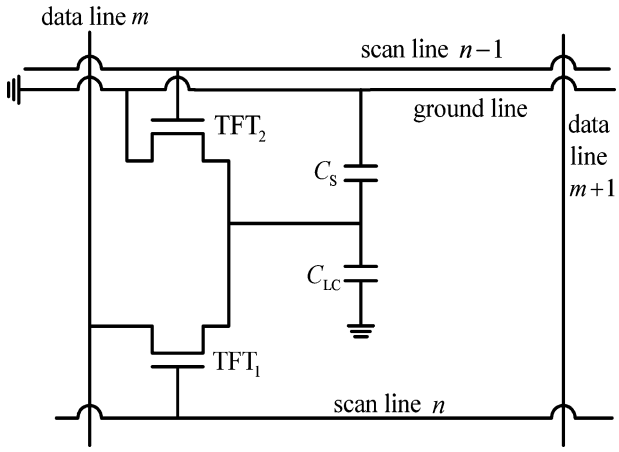

Fig. 3. Configuration of charge-recycling circuit using DTFTs.

thus $\epsilon_{\rm insu}\epsilon_0 L/t_{\rm insu} = 610$ pF/m. Hence, the upper bound in (19) is about 109 μm.

Similarly, to consider the delay along a data line, substitute $R = R_{\rm data}/L_{\rm data}$, $C = C_{\rm data}/L_{\rm data}$, and $\ell = N_{\rm scan}L_{\rm data}$ into the delay time formula to obtain another constraint

$$W < \frac{\frac{T_{\rm delay}}{1.03N_{\rm scan}^2 R_{\rm data}} - (C_{\rm x1} + C_{\rm x2} + C_{\rm d0} + C_{\rm pd} + C_{\rm pd'})}{\tilde{C}_{\rm gd}}. \tag{20}$$

The upper bound thus obtained is about 5 mm, too large to be exceeded in practice.

IV. DTFT Method

In this paper, a dual TFT (DTFT) method is proposed to speed up the charging process in any inversion mode. Fig. 3 shows the configuration of charge-recycling circuit using the DTFT method. Before subpixel (m, n) is charged, connect the display electrode to the ground by turning on $\rm TFT_2$. No external power will be consumed while the charges are pushed to or pulled from the ground. Then, connect the display electrode to data line m via $\rm TFT_1$ to charge the display electrode to the intended data voltage. Thus, the charging voltage gap required in the DTFT method is half that in the conventional single TFT (STFT) method, the charge and the charging current are also reduced by half. As a result, this method consumes less power and charges faster than the STFT method.

In this DTFT method, no time budget is deducted from the normal charging phase as in the charge-recycling method [2] or the multilevel multiphase charge-recycling method [6]. In the FSC LCDs, the allocated charging time is one-third that of the CF LCDs, and the pixel size is three times that of the CF LCDs, hence the DTFT method exhibits obvious advantage over the STFT method.

Fig. 4 shows the equivalent circuit of a DTFT subpixel. The subpixel capacitance can be approximated as

$$C_{\rm px,DTFT} \simeq C_S + C_{\rm LC}. \tag{21}$$

Comparing (21) with (1), the capacitive load of the DTFT circuit is about the same as that of the STFT circuit shwon in Fig. 1.

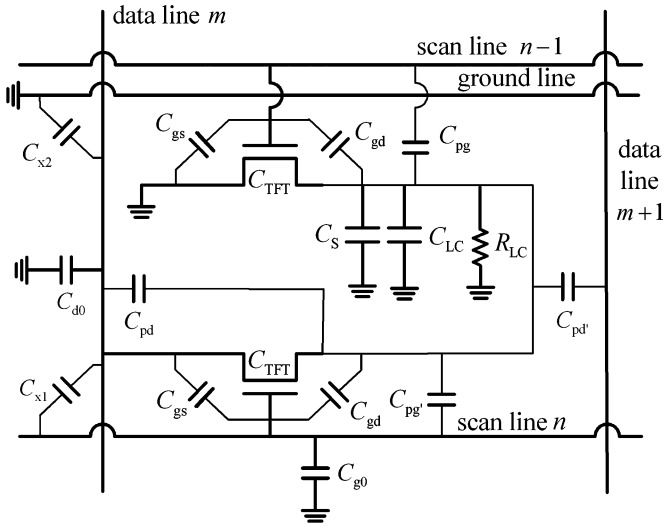

Fig. 4. Equivalent circuit of a DTFT subpixel.

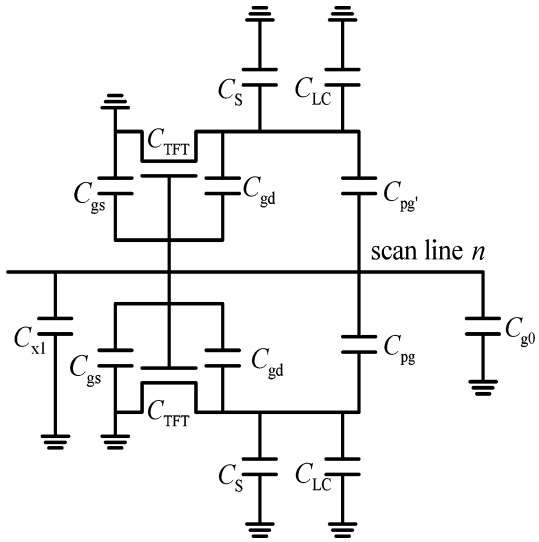

Fig. 5. Dominant load of scan line contributed by one DTFT subpixel.

The equivalent subpixel resistance in the holding phase can be calculated as

$$R_{\rm px,DTFT} = \frac{0.5R_{\rm off}R_{\rm LC}}{0.5R_{\rm off} + R_{\rm LC}}$$

because the two TFTs are in parallel. The dominant capacitive load of a DTFT subpixel on a scan line is shown in Fig. 5, which is

$$C_{\rm scan,DTFT} \simeq 2(C_{\rm gs}+C_{\rm gd}+C_{\rm TFT})+C_{\rm g0}+C_{\rm x1}+C_{\rm pg'}+C_{\rm pg}. \tag{22}$$

For the 30″ WXGA LCDs, we have $C_{\rm scan,DTFT} = 227$ fF. Comparing (22) with (2), the difference of capacitive load on a scan line is

$$C_{\rm scan,DTFT} - C_{\rm scan} = C_{\rm gs} + C_{\rm TFT} + C_{\rm gd} \simeq 57 \text{ fF}.$$

Thus, the delay on scan line in the DTFT method is about 25% longer than that in the STFT method.

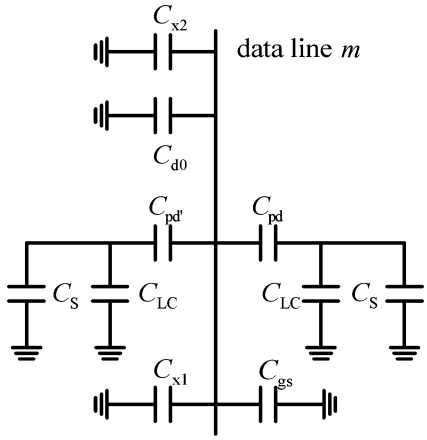

Fig. 6. Dominant load of data line contributed by one DTFT subpixel.

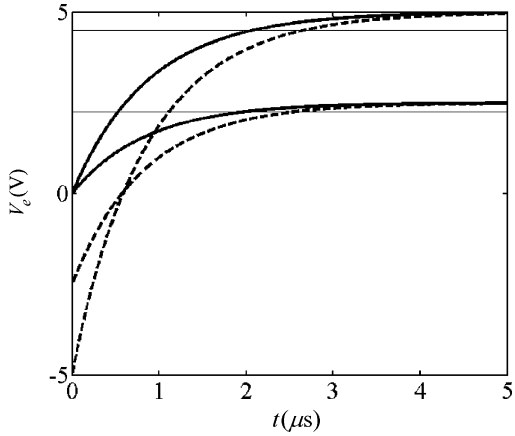

Fig. 7. Charging voltage waveforms, ——:DTFT, − −:STFT.

The dominant load of a DTFT subpixel on a data line is shown in Fig. 6, in which

$$C_{\mathrm{data,DTFT}} \simeq C_{\mathrm{x1}}+C_{\mathrm{x2}}+C_{\mathrm{d0}}+C_{\mathrm{gs}}+C_{\mathrm{pd'}}+C_{\mathrm{pd}} \simeq 182\ \mathrm{fF}. \tag{23}$$

Comparing (23) with (3), the capacitive load on data line of the DTFT subpixel is close to that of the STFT subpixel. Thus, the delays on data line in both circuits are about the same.

V. Design With DTFT

A. Charging Phase

Since $V_{e0}=0$ in the DTFT LCDs, (6) is reduced to

$$\begin{aligned} a_{\mathrm{DTFT}} &= 1 < a \\ b_{\mathrm{DTFT}} &= \frac{V_d}{2(V_s-V_t-V_d)+V_d} < b \\ k_{t,\mathrm{DTFT}} &= \ln\frac{a_{\mathrm{DTFT}}-b_{\mathrm{DTFT}}r_c}{1-r_c} < k_t \end{aligned} \tag{24}$$

where $b_{\mathrm{DTFT}}=0.033$ and $k_{t,\mathrm{DTFT}}=2.27$. Note that $a-a_{\mathrm{DTFT}} > b-b_{\mathrm{DTFT}}$. In general, the data voltage can vary from 0 V to ±5 V. Take the 30″ WXGA LCDs for example, Fig. 7 shows the charging characteristics of DTFT LCDs and STFT LCDs when the data voltage are 2.5 and 5 V, respectively. The display electrode of DTFT LCDs is grounded before charging, thus $V_{e0}=0$ V. The voltage at the display electrode in the STFT LCDs is changed from one polarity to the other due to inversion. If the data voltage is 5 V, 2.09 μs and 2.64 μs will be required for the DTFT and the STFT subpixels, respectively, to reach 90% of the intended voltage level. If the data voltage is 2.5 V, the required time for the DTFT and the STFT subpixels will be 1.97 and 2.48 μs, respectively.

Similar to (7), the design equation for the DTFT LCDs in the charging phase can be derived as

$$\frac{W}{L} > \frac{C_{\mathrm{px}}}{\mu_{\mathrm{eff}}C_g(V_s-V_t-V_d)}\frac{k_{t,\mathrm{DTFT}}}{(T_{\mathrm{row}}-T_{\mathrm{delay}})}.$$

Define the lower bound of W/L under this criterion as

$$\left(\frac{W}{L}\right)_{\mathrm{charge,DTFT}} = \frac{C_{\mathrm{px}}}{\mu_{\mathrm{eff}}C_g(V_s-V_t-V_d)}\frac{k_{t,\mathrm{DTFT}}}{(T_{\mathrm{row}}-T_{\mathrm{delay}})}.$$

Since $k_{t,\mathrm{DTFT}} < k_t$, we have

$$\left(\frac{W}{L}\right)_{\mathrm{charge,DTFT}} < \left(\frac{W}{L}\right)_{\mathrm{charge}}.$$

B. Holding Phase

With typical values of $R_{\mathrm{px,DTFT}}=2.7\times10^{12}\ \Omega$ and $R_{\mathrm{px}}=3.75\times10^{12}\ \Omega$, the constraint in the holding phase is modified as

$$\frac{W}{L} < 0.5\left(\frac{C_{\mathrm{px}}}{T_{\mathrm{frame}}2^{N_{\mathrm{bit}}}}-\frac{1}{R_{\mathrm{LC}}}\right)/\sigma_{\mathrm{D}}t_{\mathrm{semi}}.$$

The coefficient 0.5 is due to the use of dual TFTs. Define the lower bound as

$$\left(\frac{W}{L}\right)_{\mathrm{hold,DTFT}} = 0.5\left(\frac{C_{\mathrm{px}}}{T_{\mathrm{frame}}2^{N_{\mathrm{bit}}}}-\frac{1}{R_{\mathrm{LC}}}\right)/\sigma_{\mathrm{D}}t_{\mathrm{semi}}$$

thus we have

$$\left(\frac{W}{L}\right)_{\mathrm{hold,DTFT}} = 0.5\left(\frac{W}{L}\right)_{\mathrm{hold}}.$$

The constraint on W/L in the holding phase with the DTFT LCDs is tighter than that with the STFT LCDs.

C. Asymmetric Kickback

Because all the parameters in (16) for the DTFT LCDs are the same as those for the STFT LCDs, the design constraint based on asymmetric kickback is the same, namely,

$$W_{\mathrm{kb,DTFT}} = W_{\mathrm{kb}}.$$

D. Delay

Since the loads on the data line with the DTFT method and the STFT method are the same, the data-line delays with both methods are identical. On the scan line, the resistive loads are the same, but the capacitive loads are different as $C_{\mathrm{scan,DTFT}} > C_{\mathrm{scan}}$ due to the additional TFT. From (17), the scan-line delay with the DTFT method is longer than that with the STFT method as shown in Fig. 8 under the WXGA specification, where PPI

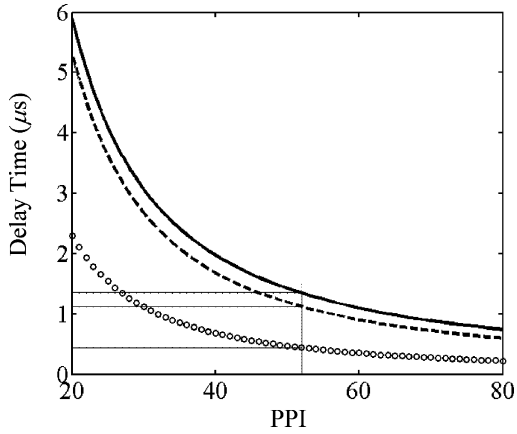

Fig. 8. Delay over signal line, ——: scan-line delay of DTFT, − −: scan-line delay of STFT and ∘: data-line delay of DTFT and STFT, $\mathrm{PPI} = 52$ for 30″ WXGA.

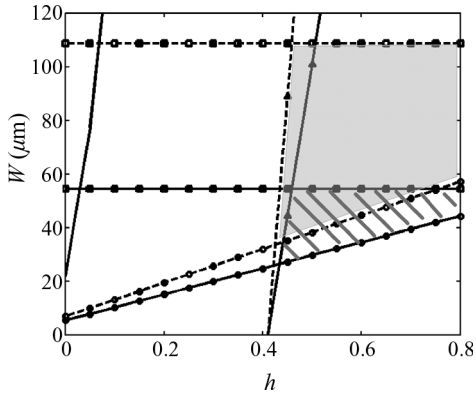

Fig. 9. Operation windows of subpixel design of 30″ WXGA LCDs, slit area with DTFT, grey area with STFT, ——∘——: charging (DTFT), − − ∘ − −: charging (STFT), ——△——: holding (DTFT), − − △ − −: holding (STFT), ——: asymmetric kickbacke (DTFT)(STFT), ——[]——: scan-line delay (DTFT), and − − [] − −: sacn-line delay (STFT).

stands for pixel per inch. A 30″ WXGA LCD is translated to $\mathrm{PPI} = 52$.

Similar to the derivation of (19), the scan-line delay renders the upper bounds for W with both methods

$$W_{\mathrm{delay,s,DTFT}} = \frac{\frac{T_{\mathrm{delay}}}{1.03N_{\mathrm{data}}^2 R_{\mathrm{scan}}} - C_{\mathrm{g0}} - C_{\mathrm{x1}} - C_{\mathrm{pg}} - C_{\mathrm{pg'}}}{4\tilde{C}_{\mathrm{gd}} + 2\epsilon_{\mathrm{insu}}\epsilon_0 L/t_{\mathrm{insu}}}$$

$$W_{\mathrm{delay,s}} = \frac{\frac{T_{\mathrm{delay}}}{1.03N_{\mathrm{data}}^2 R_{\mathrm{scan}}} - C_{\mathrm{g0}} - C_{\mathrm{x1}} - C_{\mathrm{pg}} - C_{\mathrm{pg'}}}{2\tilde{C}_{\mathrm{gd}} + \epsilon_{\mathrm{insu}}\epsilon_0 L/t_{\mathrm{insu}}}$$

where $4\tilde{C}_{\mathrm{gd}}$ and $2\epsilon_{\mathrm{insu}}\epsilon_0 L/t_{\mathrm{insu}}$ in the DTFT method are due to the additional TFT. Due to the difference in the denominator, we have

$$W_{\mathrm{delay,s,DTFT}} = \frac{1}{2} W_{\mathrm{delay,s}}.$$

Typical values are $W_{\mathrm{delay,s,DTFT}} = 54\ \mu\mathrm{m}$ and $W_{\mathrm{delay,s}} = 108.5\ \mu\mathrm{m}$. The constraint on W due to the scan-line delay with the DTFT LCDs is tighter than that with the STFT LCDs.

The constraint on data-line delay is the same as (20) with the STFT method

$$W_{\mathrm{delay,d,DTFT}} = W_{\mathrm{delay,d}}.$$

E. Operation Window

Define the ratio between the size of storage capacitor and that of the subpixel as $h = A_{C_S}/A_{\mathrm{pixel}}$. Fig. 9 shows the operation windows with both methods. Narrower channel width is required for the DTFT LCDs in the charging phase due to charge recycling. Since the charges in the two TFTs are to be preserved in the holding phase instead of one, the maximum channel width is reduced compared with that of the STFT LCDs. Due to the additional TFT, the maximum channel width must be reduced in order not to increase the capacitive load to the scan line. The constraint based on asymmetric kickback remains the same and is not dominant in this case.

The difference between $W_{\mathrm{charge,DTFT}}$ and $W_{\mathrm{charge,STFT}}$ is obvious at $h \simeq 0.4$. In the 30″ LCDs, the upper bound of W is determined by the holding phase as shown in Fig. 9. To achieve higher aperture raio, left border of the operation window is preferred, and the reduction of operation window due to scan-line delay is not significant.

F. Aperture Ratio

The aperture ratio is defined as

$$\mathrm{AR} = \frac{A_{\mathrm{pixel}} - A_{\mathrm{opaque}}}{A_{\mathrm{pixel}}} \tag{25}$$

where A_{opaque} is the opaque area in a subpixel. As shwon in Fig. 1, A_{opaque} is decomposed as

$$A_{\mathrm{opaque}} = A_{\mathrm{data}} + A_{\mathrm{scan}} + A_{\mathrm{ground}} + A_{\mathrm{TFT}} + A_{C_S} - A_{\mathrm{cross}}$$

where $A_{\mathrm{data}} = L_{\mathrm{data}} \times W_{\mathrm{data}}$ is the area of data line n, $A_{\mathrm{scan}} = L_{\mathrm{scan}} \times W_{\mathrm{scan}}$ is the area of scan line m, $A_{\mathrm{ground}} = L_{\mathrm{scan}} \times W_{\mathrm{ground}}$ is the area of the ground line in the (m,n)th subpixel, $A_{\mathrm{TFT}} = W \times L$ is the area of the TFT, $A_{C_S} = hA_{\mathrm{pixel}}$ is the area of the storage capacitor, and $A_{\mathrm{cross}} = W_{\mathrm{data}} \times (W_{\mathrm{scan}} + W_{\mathrm{ground}})$ is the overlapping area between the perpendicular lines. Typical values are $A_{\mathrm{data}} = 4{,}864\ \mu\mathrm{m}^2$, $A_{\mathrm{scan}} = 3{,}241\ \mu\mathrm{m}^2$, $A_{\mathrm{ground}} = 1{,}621\ \mu\mathrm{m}^2$, $A_{\mathrm{TFT}} = 135\ \mu\mathrm{m}^2$, $A_{\mathrm{cross}} = 300\ \mu\mathrm{m}^2$, and $A_{C_S} = 47{,}300\ \mu\mathrm{m}^2$ when $h = 0.6$ and $W = 45\ \mu\mathrm{m}$.

The ratio C_S/C_{px} is related to h as

$$\frac{C_S}{C_{\mathrm{px}}} \simeq \frac{C_S}{C_S + C_{\mathrm{LC}}} = \frac{hd_{\mathrm{LC}}}{hd_{\mathrm{LC}} + t_{\mathrm{insu}}\epsilon_{\mathrm{LC}}/\epsilon_{\mathrm{insu}}}$$

where $d_{\mathrm{LC}} = 4.7\ \mu\mathrm{m}$ and $t_{\mathrm{insu}} = 300$ nm. The DTFT method renders smaller aperture ratio but very close to that with the STFT method. For example, in 30″ WXGA LCDs, the AR with the DTFT method and that with the STFT method are 44.54% and 45.42%, respectively.

The minimum TFT channel width is determined by the charging and holding constraints. As shown in Fig. 9, the minimum TFT channel widths are $W_{\mathrm{DTFT}} = 25\ \mu\mathrm{m}$ and $W = 34\ \mu\mathrm{m}$, respectively. Fig. 9 also shows $h_{\mathrm{DTFT,min}} = 0.433 > h_{\mathrm{STFT,min}} = 0.425$, because a larger storage capacitance is required in the DTFT LCDs to compensate for the double leakage current.

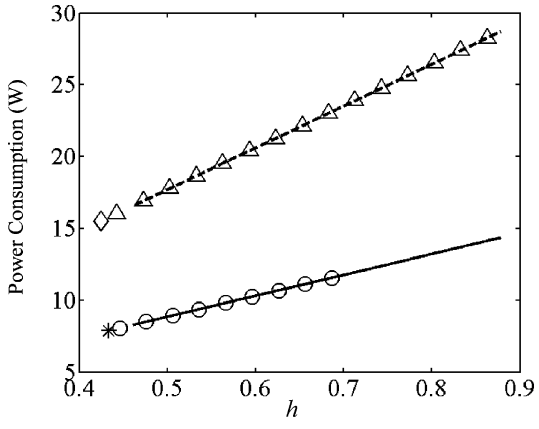

Fig. 10. Power consumption of 30″ WXGA LCDs, *: $W_{30'',\mathrm{DTFT}} = 25\,\mu$m, ∘: $W_{30'',\mathrm{DTFT}} = 40\,\mu$m, ——: $W_{30'',\mathrm{DTFT}} = 54\,\mu$m, ◇: $W_{30'',\mathrm{STFT}} = 34\,\mu$m, △: $W_{30'',\mathrm{STFT}} = 70\,\mu$m, — — —: $W_{30'',\mathrm{STFT}} = 108\,\mu$m.

G. Power Consumption

The power consumption of the data driver can be expressed as [1]

$$P = V_{\mathrm{DD}} \frac{N_{\mathrm{scan}} C_{\mathrm{px}} \Delta V_{\max}}{2T_{\mathrm{row}}} N_{\mathrm{data}}$$

where V_{DD} is the power supply voltage, $\Delta V_{\max}$ is the maximum voltage change on a data line. The ratio of power consumption with both methods becomes

$$\frac{P_{\mathrm{DTFT}}}{P_{\mathrm{STFT}}} = \frac{C_{\mathrm{px,FSC}} \Delta V_{\mathrm{max,DTFT}}}{C_{\mathrm{px,CF}} \Delta V_{\mathrm{max,STFT}}}. \tag{26}$$

The ratio of subpixel capacitances can be expressed as

$$\frac{C_{\mathrm{px,DTFT}}}{C_{\mathrm{px,STFT}}} = \frac{1 + \frac{\epsilon_{\mathrm{insu}} d_{\mathrm{LC}}}{\epsilon_{\mathrm{LC}} t_{\mathrm{insu}}} h_{\mathrm{DTFT}}}{1 + \frac{\epsilon_{\mathrm{insu}} d_{\mathrm{LC}}}{\epsilon_{\mathrm{LC}} t_{\mathrm{insu}}} h_{\mathrm{STFT}}} \simeq \frac{h_{\mathrm{DTFT}}}{h_{\mathrm{STFT}}}. \tag{27}$$

Due to the inversion-mode operation, the voltage at a given subpixel electrode swings from one polarity to the opposite between two consecutive frames. Without loss of generality, consider a still picture so that the voltage at the given subpixel will change from x V in one frame to $-x$ V in the next frame in the STFT LCDs. Because the extra TFT in the DTFT LCDs brings the electrode voltage to zero before charging the next frame, the voltage at the given subpixel will change from 0 to $-x$ V. Thus the maximum voltage change $\Delta V_{\max}$ of the DTFT LCDs is half that of the STFT LCDs. Under the same h, (26) and (27) indicate that the DTFT LCDs consume only about half the power of the STFT LCDs.

Fig. 10 shows the power consumption with both methods. It is observed that

$$P_{\mathrm{DTFT}}/P_{\mathrm{STFT}} \simeq 1/2$$

over the feasible h region.

VI. Conclusion

The inversion characteristic of LCDs is utilized to design a DTFT charge recycling method on the subpixel level. Compared with the conventional STFT method, this method takes shorter charging time. The design constraints of the DTFT method is less stringent in the charging phase, but is tighter in the holding phase and the scan-line delay. The constraints in the asymmetric kickback and data-line delay are similar. The operation window based on the design constraints are dominated by the charging, holding and scan-line delay. The aperture ratio of the DTFT LCDs is similar to that of the STFT LCDs, but the power consumption is about half that of the STFT LCDs.

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