A 30 GHz Active Quasi-Circulator With Current-Reuse Technique in $0.18\ \mu\mathrm{m}$ CMOS Technology

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***Abstract*—An active quasi-circulator at 30 GHz is designed and fabricated in TSMC $0.18\ \mu\mathrm{m}$ RF mixed signal CMOS technology. The current-reuse technique is integrated with a common-source stage to form the quasi-circulator core while reducing the power consumption at the same time. The transmitter-to-receiver leakage is alleviated by the out-of-phase cancellation of signals from two paths. The isolation and insertion loss between other pairs of ports are improved with buffer stages. All the measured isolations are higher than 12 dB, all the insertion losses are lower than 7.9 dB, and the total power consumption is 15 mW.**

***Index Terms*—Active-circulator, circulator, CMOS, current-reuse, monolithic microwave integrated circuit (MMIC), quasi-circulator.**

I. Introduction

THREE-PORT circulators are commonly used in microwave and millimeter-wave systems to decouple the transmitted and received signal paths [1]. For example, it allows the transmitter and the receiver to share a common antenna in FMCW radars [2]. An ideal three-port passive circulator is specified as $|S_{21}| = |S_{32}| = |S_{13}| = 1$ and the other scattering parameters being 0. Circulators can be implemented in integrated circuit, which has the advantages of small size, low cost, and being integratable with RF and baseband modules on a single chip [3].

A quasi-circulator is a special type of circulator with its receiver port isolated from its transmitter port, or $|S_{13}| = 0$. Several active quasi-circulators have been reported in recent years. In [4], transistors with common-source, common-gate, and common-drain topologies are integrated to improve the isolations. In [5], a phase shifter is used to improve the isolation between two specific ports. In [6], an active balun and two transconductance amplifiers (OTAs) are used to design a quasi-circulator without inductors.

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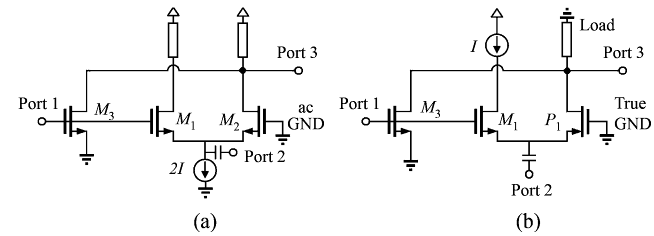

Fig. 1. (a) Core of active circulator and (b) core of active circulator using current-reuse technique.

In this work, an active quasi-circulator is designed to operate at 30 GHz, which is far beyond the operating frequency of CMOS circulators reported in the literatures. The current-reuse technique is integrated with a common-source stage to form the quasi-circulator core. Two common-source buffers are used to compensate for the loss at high frequencies, which also improve the isolation. The out-of-phase cancellation technique is applied to reduce $|S_{31}|$.

II. Circuit Design

Fig. 1(a) shows the core of a three-port quasi-circulator, which consists of a common-drain transistor M_1, a common-gate transistor M_2, and a common-source transistor M_3. In this work, ports 1, 2, and 3 are connected to the transmitter, the antenna and the receiver, respectively.

The source terminals of M_1 and M_2 are connected to form an active balun. The phase difference between the drain terminals of M_1 and M_2 is 180°. The transistor M_3 is connected in parallel to M_1 and M_2. The drain terminals of M_3 and M_1 are in phase, and those of M_3 and M_2 are out of phase. The signals between ports 1 and 3 are canceled by connecting the drain terminals of M_3 and M_2 together. A current source made of an NMOS transistor is typically connected to the source terminals of M_1 and M_2. The signal can be fed either at the drain of the current source to get better input matching, or the gate of the current source to get another transconductance gain.

Fig. 1(b) shows an alternative configuration without the current source, and the original NMOS M_2 is replaced by a PMOS P_1. The signal from/to port 2 (antenna) is coupled to the source terminals of M_2 and P_1 through on-chip capacitors. In this manner, the dc current flowing through M_1 is reused by P_1, hence the dc current is only half of that used in Fig. 1(a). Since the voltage headroom of the current-reuse circulator is slightly higher than that in Fig. 1(a), the power is saved by slightly lower than 50%.

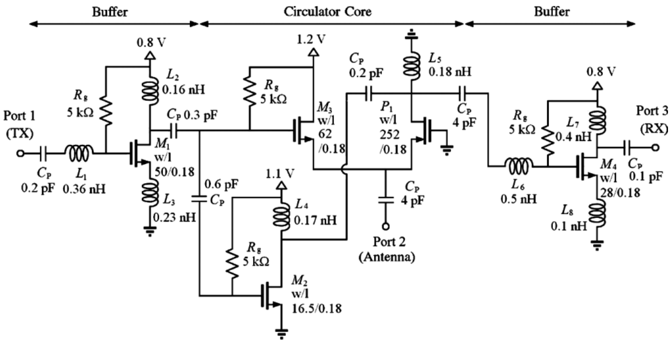

Fig. 2. Proposed active quasi-circulator circuit. Bypass capacitors at dc terminals and body-source connection of all transistors are not shown for simplicity.

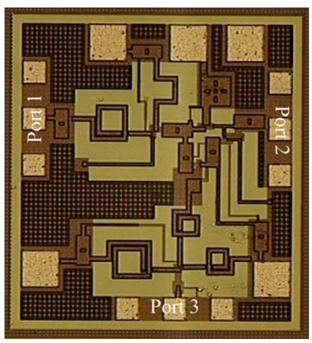

Fig. 3. Chip photo of the proposed active quasi-circulator.

Fig. 2 shows the proposed active quasi-circulator. The core consists of a common-drain transistor M_3, a common-gate transistor P_1, and a common-source transistor M_2. At higher operating frequencies, the parasitic capacitance will degrade the isolation, and the transconductance of transistors will drop, resulting in higher insertion loss. Hence, two buffers are adopted to decrease the insertion losses and increase the isolations. The common-source transistors M_1 and M_4 are used as the output buffer for the transmitter and the input buffer for the receiver, respectively.

Fig. 3 shows the chip photo of the proposed active quasi-circulator, which is implemented with the TSMC 0.18 μm CMOS RF mixed signal technology. The chip size is $0.57\ \mathrm{mm} \times 0.64\ \mathrm{mm}$, including test pads. The RF pads for probing have the size of 50 μm $\times$ 50 μm, and pitches of 100 μm. The dc pads and the ground pads are 80 μm $\times$ 80 μm in size. All the inductors and passive components have been simulated using the EM simulation tool SONNET.

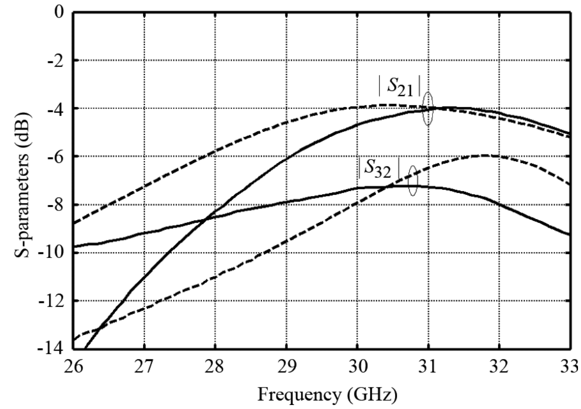

Fig. 4. Insertion losses of the circulator, —: measurement, – – –: simulation.

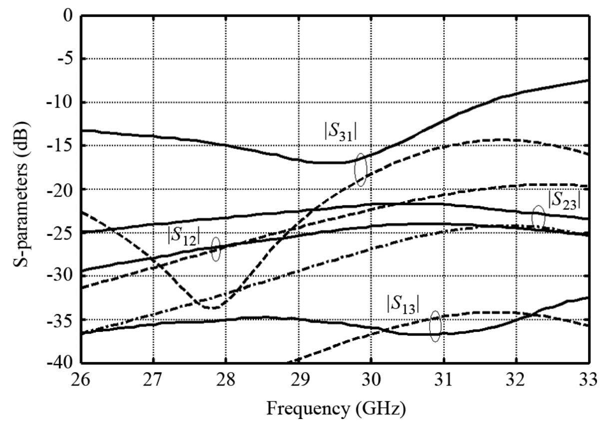

Fig. 5. Isolations of the circulator, —: measurement, – – –: simulation.

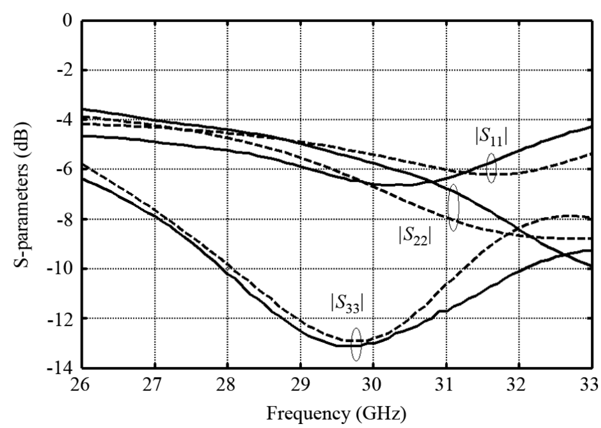

Fig. 6. Return losses of the circulator, —: measurement, – – –: simulation.

III. RESULTSAND DISCUSSIONS

Define the isolation from port n to port m as $\mathrm{IS}_{mn} = -20\log_{10}|S_{mn}|$, with $mn = 12,\ 13,\ 23,\ 31$. Similarly, define the transmission coefficient from port n to port m as $\mathrm{T}_{mn} = 20\log_{10}|S_{mn}|$ with $mn = 21,\ 32$, and the return loss at port n as $\mathrm{RL}_n = -20\log_{10}|S_{nn}|$ with $1 \leq n \leq 4$.

Figs. 4–6 show the simulation and measurement results of insertion losses, isolations, and return losses, respectively, of the circulator. The measured IL_{21} (insertion loss from TX to antenna) lies between 4 and 6 dB from 29 to 31 GHz, and the measured IL_{32} (from antenna to RX) lies between 7.2 and 7.9 dB. The poorest isolation is IS_{31} (TX-RX). In order to increase IS_{31}, the signals via M_3-P_1 path and M_2 path are preferred to have the same magnitude and 180° phase difference. For the configuration of Fig. 1(b), the simulated gain and phase differences between these two paths are 1.2 dB and 174°, respectively, at 30 GHz. The gain difference approaches 0 dB at 28 GHz, with the phase difference of 176.6°. The measured IS_{31} is 16 dB at 30 GHz, and the best isolation is achieved at 28 GHz. The worst isolation appears at 31 GHz, where perfect phase cancellation is difficult to reach due to parasitics at high frequencies.

All the other isolation parameters, IS_{12}, IS_{23} and IS_{13} are higher than 22 dB from 29 to 31 GHz. These isolation parameters and insertion losses can be improved using buffer stages at the input/output ports of the circulator core.

TABLE I
PERFORMANCE COMPARISON OF MMIC QUASI-CIRCULATORS

Parameter		This work	MWCL08[4]	MWCL08[5]	MWCL09[6]	MTT10[7]
Technology		0.18μm CMOS	0.18μm CMOS	GaAs on FR4	0.18μm CMOS	0.25μm pHEMT
Techniques		current reuse+CS	CS+CD+CG	DA+phase-shifter	balun+OTA	active hybrid
Frequency (GHz)		29-31	1.5-9.6	0.8-2.2	1.5-2.7	10.25-12.6
Isolation (dB):	IS_{31}	> 12	> 18	> 15	> 26	> 30
	IS_{12}	> 24	> 55	> 25	> 25	NA
	IS_{23}	> 22	> 26	> 27	> 25	NA
	IS_{13}	> 35	> 60	> 29	> 22	NA
Transmission (dB):	T_{21}	-4 to -6	-4 to -6	1.5	2.4 to 1.5	1.5
	T_{32}	-7.2 to -7.9	-4 to -6	0	0 to -3	-4.7
Return loss (dB):	RL_1	> 6	> 5	> 10	> 12.5	> 11
	RL_2	> 5	> 6	> 15	> 10	> 17
	RL_3	> 11.5	> 3	> 12	> 12.5	> 17
DC Power (mW)		15	31.6	60	86	NA
Chip area (mm^2)		0.36	0.41	NA	0.25	25
$P_{1\mathrm{dB}}$ (dBm)	Port 1-2	-7 @ in	-3.7 @ in	8 @out	-6.4 @ in	34.6 @ out
	Port 2-3	-1.5 @ in	4.3 @ in	NA	NA	34.6 @ out

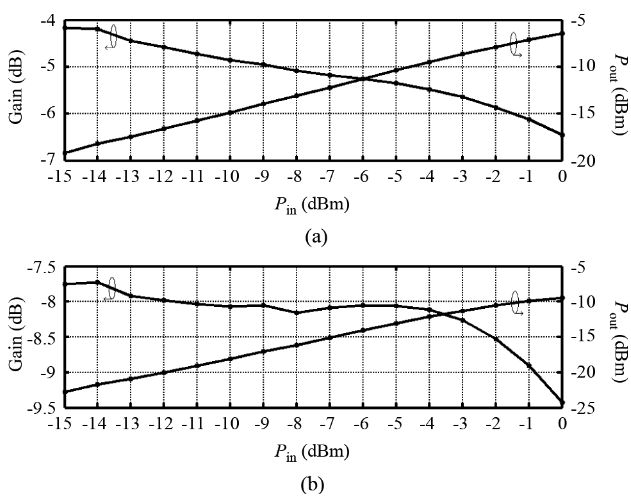

Fig. 7. Measured input $P_{1\ \mathrm{dB}}$ of the circulor: (a) from port 1 to port 2, (b) from port 2 to port 3.

As shown in Fig. 7, the input $P_{1\ \mathrm{dB}}$ measured at 31 GHz is $-7\ \mathrm{dBm}$ from port 1 to port 2 (TX to antenna), and $-1.5\ \mathrm{dBm}$ from port 2 to port 3 (antenna to RX). The power consumptions of the circulator core (M_3, P_1 and M_2) and the buffer stages (M_1 and M_4) are 5.6 and 9.4 mW, respectively.

Table I lists the performance of the proposed design in comparison with literatures. Note that the term "transmission coefficient" is used instead of gain or insertion loss to reduce confusion. This design consumes the least power while maintaining comparative performance. So far as we know, this circulator operates at the highest frequency among those implemented in CMOS technology [7].

IV. CONCLUSION

An active quasi-circulator at 30 GHz is designed and fabricated in TSMC $0.18\ \mu\mathrm{m}$ CMOS technology. The insertion loss is between 4–6 dB from the transmitter to the antenna, and 7.2–7.9 dB from the antenna to the receiver, the worst isolation is 12 dB. By integrating the current-reuse technique, the power consumption in the circulator core is reduced to 5.6 mW. The insertion losses and the isolation parameters (except IS_{31}) can be improved using two buffer stages at the transmitter and the receiver ports. Better performance can be achieved at the cost of more dc power consumption.

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