A 0.18 μm CMOS Self-Mixing Frequency Tripler

Yu-Tsung Lo and Jean-Fu Kiang

***Abstract*—A self-mixing frequency tripler with fundamental frequency between 6–7.3 GHz is built by cascading a doubler and a single-balanced mixer. The doubler and the mixer share a transconducting inductor to reduce the tripler core size when fabricated using the TSMC 0.18 μm RF mixed signal 1P6M process. When the input signal frequency is 6.5 GHz at the power level of 3 dBm, the measured conversion gain is −9.5 dB, the HRR1 is 21.5 dBc, the HRR2 is 29 dBc, and the total dc power consumption is 18.8 mW.**

***Index Terms*—Doubler, frequency tripler, harmonic generation, self-mixing, single-balanced mixer.**

I. Introduction

DESIGN of a frequency tripler is a challenging task since the third-order nonlinearity of a field effect transistor (FET) is usually very small. Frequency triplers based on amplifying this third-order nonlinearity have been addressed in [1], [2]. An alternative design of a frequency tripler is to inject a third-harmonic signal from a harmonic-generation device to the coupled oscillators with free-running frequencies around the injected signal [3]. A third approach, known as the self-mixing technique, uses a doubler to generate signal at $2f_0$, which is up-converted with another mixer to $3f_0$ [4], both the douber and the mixer share the same input. In [5] and [6], the second harmonic and the fundamental tone from the embedded VCO are mixed at the mixer to achieve the third harmonic. A shunt peaking technique is also adopted in [5] to enhance the second-harmonic signal.

In this work, the self-mixing technique is adopted, with a doubler integrated with the mixer, to extract the third-harmonic signal. The input signal at fundamental frequency is sent to both the input port of the doubler and the LO port of the mixer. The transistors of the doubler and the mixer are biased at the same voltage to be near the pinch-off region. The loading inductor of the doubler also serves as a transconducting element of the mixer to reduce the core size. Compared to [4], no cascading element is used in the design, which makes it more feasible under low supply voltage.

Manuscript received August 17, 2011; revised November 09, 2011; accepted December 08, 2011. Date of publication January 24, 2012; date of current version February 15, 2012. This work was supported by the National Science Council of Taiwan under contract NSC 97-2221-E-002-142 and by the National Chip Implementation Center(CIC), Taiwan.

The authors are with the Department of Electrical Engineering and the Graduate Institute of Communication Engineering, National Taiwan University, Taipei, Taiwan (e-mail: jfkiang@cc.ee.ntu.edu.tw).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LMWC.2011.2180370

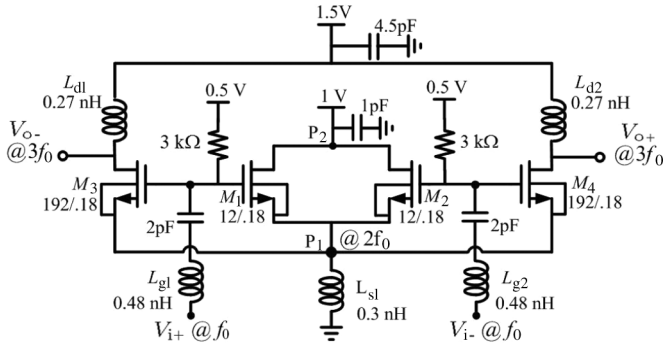

Fig. 1. Core of the proposed frequency tripler.

II. Circuit Design

Fig. 1 shows the core of the proposed frequency tripler. Transistors M_1 and M_2 are in the common-drain configuration, with the differential signals input at the fundamental frequency f_0 via the gates. The second-harmonic current signals at $2f_0$ appear at point P_1, which is transconducted to a voltage by the inductor L_{s1}. This voltage signal is fed to the source terminals of M_3 and M_4, which form the switching pair of a single-balanced mixer. The switching pair are modulated by the same input signal at f_0, hence the output signal from the mixer contains a component at f_0 and the third harmonic at $3f_0$. A pair of buffers are then used to filter out the fundamental tone.

The doubler and the mixer are biased at the same dc level of 0.5 V. The supply voltages of the doubler and the mixer are 1 and 1.5 V, respectively, and the associated currents are 0.5 and 7.1 mA, respectively, with the input power of 3 dBm. Since transistors M_1 to M_4 share the same input signal and their sources are connected together, transistors M_3 and M_4 also take part in the doubler function, hence their effect must be considered in designing the doubler.

In the single-blanced mixer, transistors M_3 and M_4 are biased near the pinch-off region, and the transistor sizes are selected to achieve the maximum up-conversion gain around 6.5 GHz. By simulation, the overall conversion gain appears more sensitive to the size of M_3 and M_4 than that of M_1 and M_2. Thus, the size of M_3 and M_4 in the mixer is adjusted first, then the size of M_1 and M_2 are tuned to maxmize the conversion gain of the doubler.

The inductor L_{s1} serves as the load of the doubler as well as the tranconducting element of the mixer. Fig. 2 shows the simulated conversion gain of the doubler and the mixer at different values of L_{s1}. At $L_{s1} = 0.3\,\mathrm{nH}$, maximum gain of the doubler and moderate gain of the mixer are achieved, and the conversion gain of the tripler core is about -16.5 dB.

Fig. 3 shows one of the output buffer pair, which is a two-stage common-source amplifier. It enhances the conversion gain of the tripler as well as the out-of-band isolation. The buffer

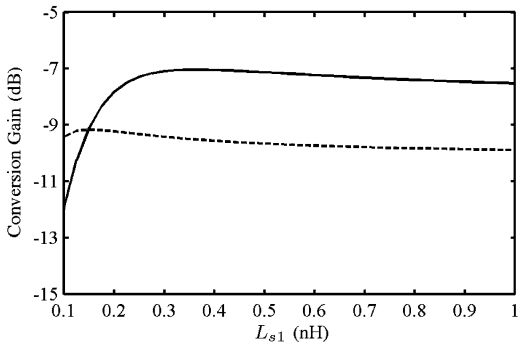

Fig. 2. Effect of L_{s1} on the conversion gain by simulation, —: doubler, $\cdots$: mixer.

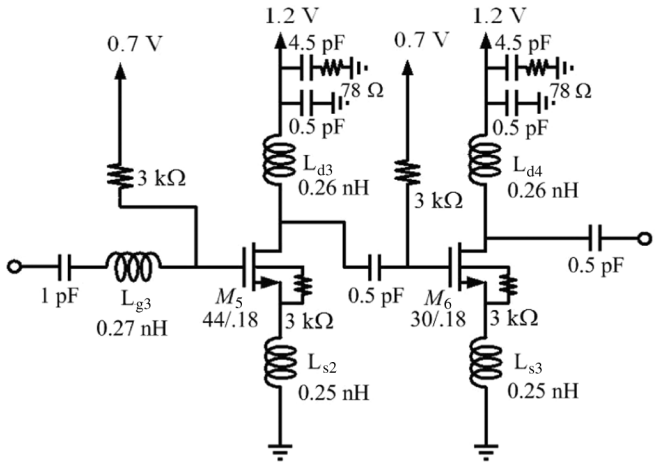

Fig. 3. Buffer after the tripler core.

provides about 7 dB of power gain at 20 GHz, and each buffer consumes 3.8 mW of dc power. The input 1 dB compression point ($P_{1\,\mathrm{dB}}$) is designed at −7 dBm. When the input power is 3 dBm, the power level at the buffer input is about −13.5 dBm, well below $P_{1\,\mathrm{dB}}$ of the buffer.

III. Measurement Results

Fig. 4 shows the photo of the chip, which is fabricated using the TSMC 0.18 μm RF mixed signal 1P6M process. The chip size is 1.21 mm × 1.11 mm, including on-chip buffers and testing pads. On-wafer probing is used to feed the RF signal and dc power. A 1–12.4 GHz balun and a 10–40 GHz balun are used to provide and combine differential signals at the input and output port, respectively. The input power at f_0 is 3 dBm during the measurement of conversion gain.

Figs. 5 and 6 show the measured output spectra at f_0 = 4.5 and 7 GHz, respectively. Fig. 7 shows the measured and simulated conversion gain of the tripler, which is defined as $G_3 = P_{3f,\mathrm{out}} - P_{f,\mathrm{in}}$, with all the power levels in dBm. The conversion gain lies between −14.2 and −9.5 dB when the input signal sweeps from 6 to 7.3 GHz. The conversion gain of the second harmonic is defined as $G_2 = P_{2f,\mathrm{out}} - P_{f,\mathrm{in}}$. The measured G_2 lies between −36 to −39.2 dB when the input signal sweeps from 6 to 7.3 GHz. The measured fundamental gain $G_1 = P_{f,\mathrm{out}} - P_{f,\mathrm{in}}$ lies between −27.9 to −33.8 dB in the same frequency range. The measured and simulated conversion

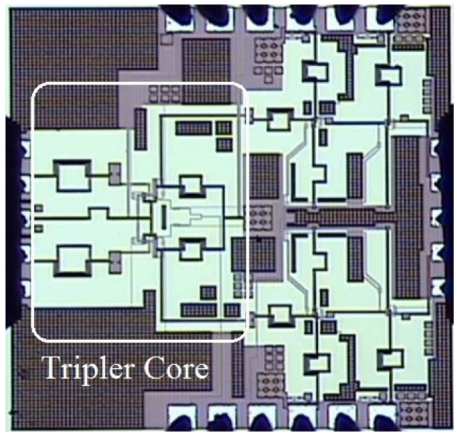

Fig. 4. Chip photo of the proposed frequency tripler, with RF and dc probes attached.

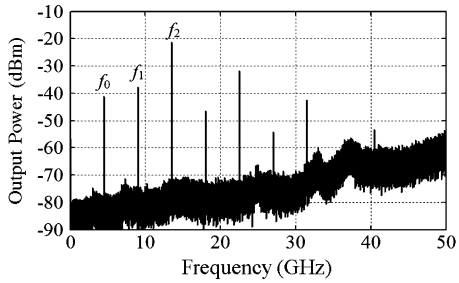

Fig. 5. Measured spectrum of the tripler output, $f_0 = 4.5$ GHz, $f_1 = 9$ GHz, and $f_2 = 13.5$ GHz.

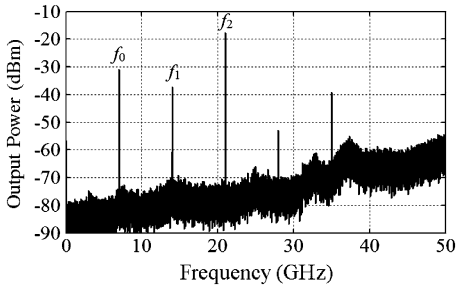

Fig. 6. Measured spectrum of the tripler output, $f_0 = 7$ GHz, $f_1 = 14$ GHz, and $f_2 = 21$ GHz.

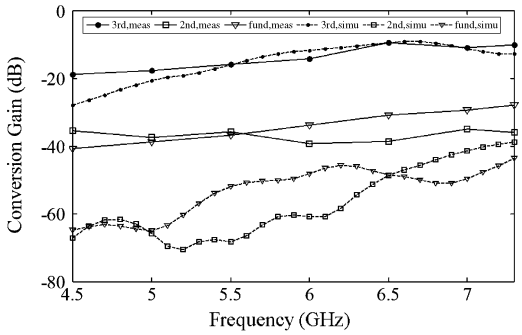

Fig. 7. Conversion gain of the harmonics.

gains are similar. The difference between measured and simulated results of G_2 and G_3 is mainly caused by device mismatch.

Fig. 8 shows the measured and simulated harmonic rejection ratios of the tripler, which are defined as $\mathrm{HRR1} = P_{3f,\mathrm{out}} - P_{f,\mathrm{out}}$ and $\mathrm{HRR2} = P_{3f,\mathrm{out}} - P_{2f,\mathrm{out}}$, with all the power levels in dBm. The measured HRR1 lies between 16.9 and 21.5 dBc,

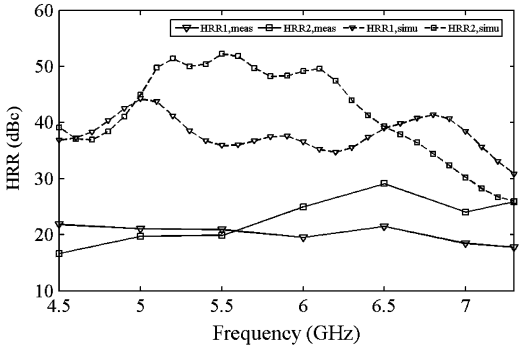

Fig. 8. Harmonic rejection ratios of the proposed tripler.

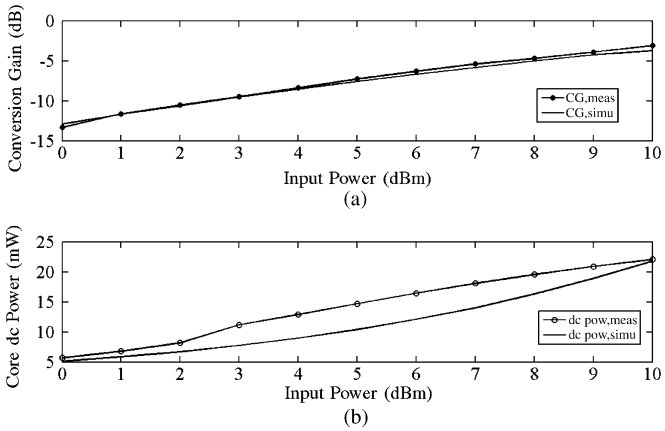

Fig. 9. Effect of input power on (a) conversion gain and (b) dc power consumption of the tripler core at input frequency of 6.5 GHz.

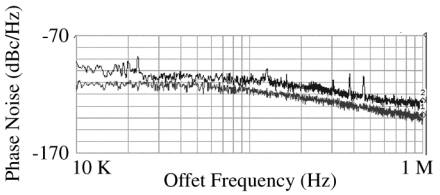

Fig. 10. Measure phase noise of the proposed tripler and the injection source, upper: tripler output, lower: injection source.

and HRR2 lies between 24 and 29 dBc, when f_0 sweeps from 6 to 7.3 GHz.

Fig. 9 shows the effect of the input power level on the conversion gain and the dc power consumption of the core. The power level of 3 dBm seems a reasonable trade-off, at which the tripler core consumes 11.2 mW of dc power and the two buffers consume 7.6 mW.

Fig. 10 shows the measured phase noise of the input signal at f_0 from the signal generator Agilent E8257D and the output signal at $3f_0$ from the tripler. The input phase noise of the former is -138 dBc/Hz @ 1 MHz offset, and that of the the third-harmonic output is -128.06 dBc/Hz @ 1 MHz offset. The minimum degradation due to frequency multiplication is $20\log_{10} N$, with N being the harmonic order [7]. The phase noise degradation of the proposed design is 9.94 dB, which is 0.4 dB worse than the minimum value of 9.54 dB, due to the noise of the active nonlinear elements and the conversion loss [7]. The spikes on the measured data may be due to dc probing and measurement set-up. Usually, the spikes are more obvious when measured with the spectrum analyzer than with the signal source analyzer (SSA).

TABLE I
MEASURED PERFORMANCE OF THE 6–7.3 GHz TRIPLER AND COMPARISON WITH LITERATURES

Parameters	This work	MWCL 09 [8]	TMTT 09 [9]	RFIC 10 [4]	SIRF 10 [10]
input signal (GHz)	6 to 7.3	6-8	1	12-16	1.5
conversion gain (dB)	-14.2 to -9.5	-19 to -5.7	3	-20 to -11.4	-4.2
HRR1 (dBc)	16.9 to 21.5	9.5 to 22.44	30	> 40	35
HRR2 (dBc)	24 to 29	4 to 19.5	26	> 10	-
input power (dBm)	3	10	-10	0	14
dc Power (mW)	18.8	39.6	68	21.8	43.1
output signals	differential	IQ#	single-ended	single-ended	IQ#
chip area (mm^2)	1.21 × 1.11	1 × 1.05	1 × 0.8	0.6 × 0.44	1.4 × 1.1
process	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.13 μm CMOS	0.18 μm CMOS

with I and Q channels, each with single-ended output.

Table I lists the comparison of the propsoed tripler with recent publications in similar frequency ranges. This design achieves moderate conversion gain, acceptable input power level of 3 dBm and good harmonic rejection with the dc power consumption of 18.8 mW, including the buffers. Note that the tripler core occupies only about one third of the overall chip size.

IV. CONCLUSION

A tripler core composed of a doubler and a single-balanced mixer has been designed and implemented. At the input power level of 3 dBm, the measured conversion gain is -9.5 dB, HRR1 is 21.5 dBc, HRR2 is 29 dBc, and the total dc power consumption is 18.8 mW at the input frequency of 6.5 GHz.

REFERENCES

[1] A. Boudiaf, D. Bachelet, and C. Rumelhard, "A high-effciency and low-phase-noise 38-GHz pHEMT MMIC tripler," *IEEE Trans. Microw. Theory Tech.*, vol. 48, no. 12, pp. 2546–2553, Dec. 2000.

[2] N. C. Kuo, J. C. Kao, Z. M. Tsai, K. Y. Lin, and H. Wang, "A 60-GHz frequency tripler with gain and dynamic-range enhancement," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 3, pp. 660–671, Mar. 2011.

[3] W. L. Chan, J. R. Long, and J. J. Pekarik, "A 56-to-65 GHz injection-locked frequency tripler with quadrature outputs in 90 nm CMOS," in *ISSCC Dig.*, Feb. 2008, pp. 480–481.

[4] S. S. Ghouchani and J. Paramesh, "A wideband millimeter-wave frequency doubler-tripler in 0.13- μm CMOS," in *IEEE RFIC Symp. Dig.*, 2010, pp. 65–68.

[5] G. Huang and V. Fusco, "A 94 GHz wide tuning range SiGe bipolar VCO using a self-mixing technique," *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 2, pp. 86–88, Feb. 2011.

[6] P. K. Tsai, C. Y. Liu, and T. H. Huang, "A CMOS voltage controlled oscillator and frequency tripler for 22–27 GHz local oscillator generation," *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 9, pp. 492–494, Sep. 2011.

[7] K. V. Puglia, "Phase noise analysis of component cascades," *IEEE Microw. Mag.*, vol. 3, no. 4, pp. 71–75, Dec. 2002.

[8] C. N. Kuo, H. S. Chen, and T. C. Yan, "A K-band CMOS quadrature frequency tripler using sub-harmonic mixer," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 12, pp. 822–824, Dec. 2009.

[9] B. R. Jackson, F. Mazzilli, and C. E. Saavedra, "A frequency tripler using a subharmonic mixer and fundamental cancellation," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 5, pp. 1083–1090, May 2009.

[10] C. C. Tsai, D. Chang, H. S. Chen, and C. N. Kuo, "A 11-mW quadrature frequency tripler with fundamental cancellation," in *Proc. IEEE Silicon Monolith. ICs RF Syst. Meeting*, Jan. 2010, pp. 100–103.