A 5-GHz CMOS Frequency Synthesizer With an Injection-Locked Frequency Divider and Differential Switched Capacitors

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***Abstract*—A phase-locked loop (PLL)-based frequency synthesizer at 5 GHz is designed and fabricated in 0.18-μm CMOS technology. The power consumption of the synthesizer is significantly reduced by using an injection-locked frequency divider (ILFD) as the first frequency divider in the PLL feedback loop. The synthesizer chip consumes 18 mW of power, of which only 3.93 mW is consumed by the voltage-controlled oscillator (VCO) and the ILFD at 1.8-V supply voltage. The VCO has the phase noise of −104 dBc/Hz at 1-MHz offset and an output tuning range of 740 MHz. The chip size is 1.1 mm × 0.95 mm.**

***Index Terms*—Frequency divider, injection-locked frequency divider (ILFD), integer-N, low power, oscillator, phase-locked loop (PLL), receiver, synthesizer, voltage-controlled oscillator (VCO), wireless local area network (WLAN).**

I. Introduction

THE IEEE 802.11a wireless local area network (WLAN) is allocated 300-MHz bandwidth at 5 GHz, which can support a data throughput of 54 Mb/s or higher. The lower 200 MHz (5.15–5.35 GHz) is shared with the European high-performance radio LAN band. The upper 100 MHz (5.725–5.825 GHz) falls in the industrial, scientific, and medical band.

In this paper, we focus on the lower 200-MHz band, which is divided into eight channels and at a channel spacing of 20 MHz [1]. A low-power frequency synthesizer is designed in CMOS technology. The design issues and frequency planning of the frequency synthesizer will be presented in Section II. Building blocks of the phase-locked loop (PLL) will be presented in Section III. Simulation and measurement results will be discussed in Section IV, followed by the conclusions.

II. Architecture of Synthesizer

Typical architectures of RF frequency synthesizer include integer-N, fractional-N, and dual loop. Among them, the integer-N architecture is the most popular one, but its loop bandwidth is limited because the reference frequency must be equal to the channel spacing. Thus, low reference frequency and high division ratio must be used in the feedback loop of an integer-N architecture. However, the channel spacing of IEEE 802.11a is 20 MHz, which is wide enough to relax the earlier constraint [2]. Hence, the integer-N architecture will be adopted in this paper. In order to reduce power consumption, high-frequency building blocks such as voltage-controlled oscillators (VCOs) and dividers will impose design challenges.

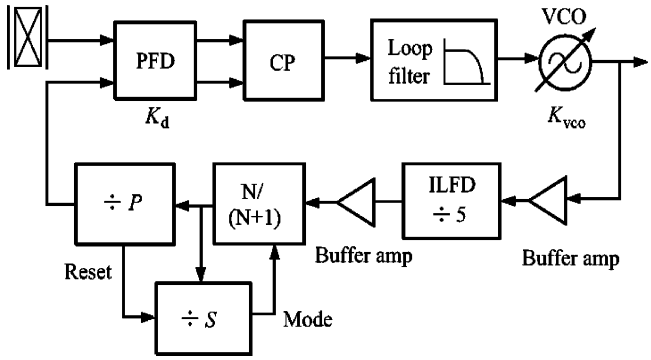

Fig. 1. Architecture of PLL-based integer-N frequency synthesizer.

TABLE I
Division Ratio and Frequency of All Channels, $N = 16$, $P = 16$

Parameter	f_{out} (MHz)	M	S
Channel 1	5,180	1,295	3
Channel 2	5,200	1,300	4
Channel 3	5,220	1,305	5
Channel 4	5,240	1,310	6
Channel 5	5,260	1,315	7
Channel 6	5,280	1,320	8
Channel 7	5,300	1,325	9
Channel 8	5,320	1,330	10

Fig. 1 shows the architecture of this paper, which includes phase frequency detector (PFD), charge pump (CP), third-order loop filter, VCO, injection-locked frequency divider (ILFD) with modulus 5, and pulse swallow divider. The reference frequency is $f_{\text{ref}} = 4$ MHz, and the loop bandwidth is 200 kHz, which is less than $f_{\text{ref}}/10$.

Table I lists the division ratios $M = 5 \times (NP + S)$ of all channels. The dual-modulus prescaler is $N/(N+1) = 16/17$, the P counter is fixed as 16, and the S counter changes from three to ten. Thus, the division ratio M of the feedback loop

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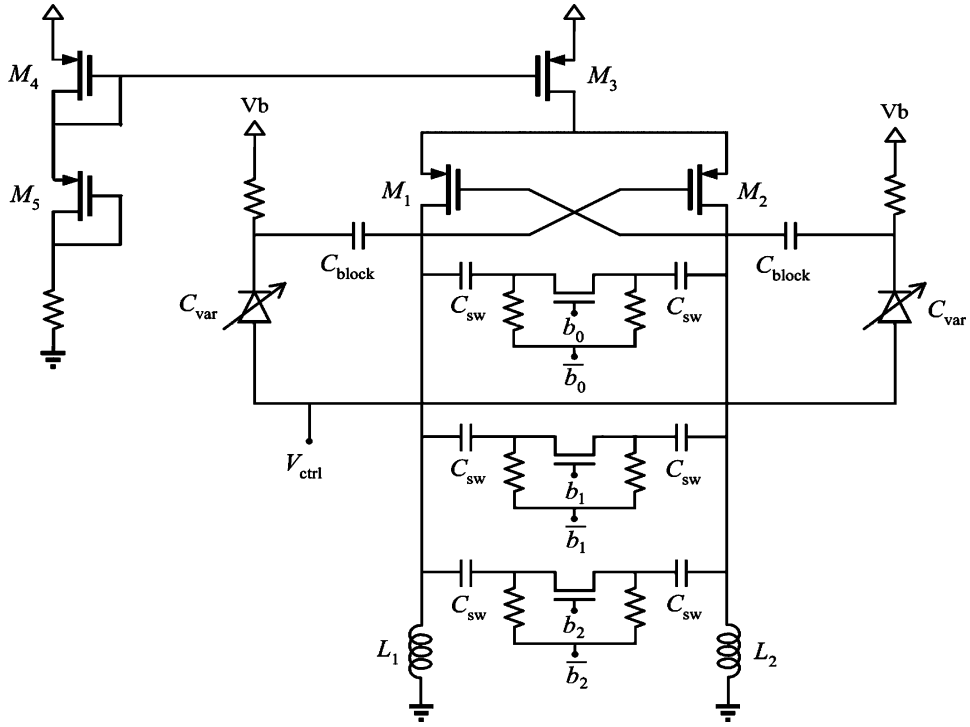

Fig. 2. Wide-band VCO using DSCA.

will change from 1295 to 1330 in steps of 5, complying with the frequency step of 20 MHz specified in the IEEE 802.11a lower band (5.15–5.25 GHz) and middle band (5.25–5.35 GHz).

III. Circuit Implementation

A. VCO

Fig. 2 shows the wideband VCO using differential switched-capacitor array (DSCA) [3]. The cross-coupled negative-transconductance cells (M_1, M_2) are used to compensate for the losses in the LC tanks, MOS varactor $(C_{\rm var})$, and DSCA. The pMOS cross-coupled pair is used because it has lower noise than the nMOS pair.

Fig. 3 shows the DSCA which has low phase noise [4]. When the switched circuit is embedded into the differential oscillator, the LC tank is loaded by two identical switches as shown in Fig. 3(a). Each on-resistance will degrade the tank over one half period due to the differential design. Fig. 3(b) shows the equivalent circuit in which the sources of the two switches are tied together. Due to symmetry of the circuit, the source of the switches becomes a virtual ground. The total resistance load of the resonator is equal to $2r_{\rm ds}$, which suggests that the two switches may be merged into one switch with an effective length of $2L$, as shown in Fig. 3(c). In order to secure symmetry, the drain and source terminals of the switch shown in Fig. 3(c) are connected to the inverse gate voltage via a large resistance as shown in Fig. 3(d).

The Q factor of DSCA is given by [4]

$$Q = \frac{\mu_n C_{\rm ox} W (V_{\rm GS} - V_t)}{\omega_0 \cdot 2L \cdot C}.$$

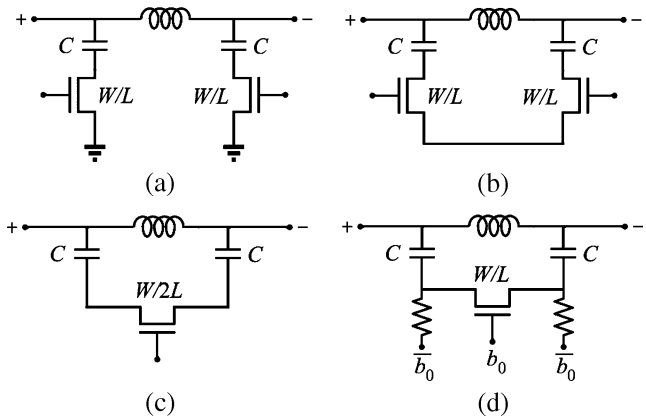

Fig. 3. Switch capacitor element. (a) Two single-ended switches connected to two VCO nodes. (b) Removal of ground. (c) Merged switch. (d) Differential switch [4].

Note that if the gate length is L instead of $2L$, the quality factor of the differential switch will be doubled and the maximum achievable frequency could be increased.

In this design, the frequency tuning is achieved by using the accumulation-mode MOS varactor [5]. The capacitor $C_{\rm block}$ is used to isolate the dc levels of the VCO core and the varactor. The use of $C_{\rm block}$ and an additional control voltage V_b provides an effective way to increase the tuning range across $C_{\rm var}$ from $0 - V_{\rm dd}/2$ to $-V_{\rm dd}/2 - V_{\rm dd}/2$. The $C_{\rm block}$ has a magnitude of about 300 fF, it also helps to stabilize the dc voltage level at the drains of M_1 and M_2.

The control voltage can be varied from 0 to 1.8 V to extend the tuning range. Fig. 4 shows the tuning characteristics of the free-running VCO. The four curves are measured at different combinations of the tuning bits b_0 to b_2 in Fig. 2. The tunable

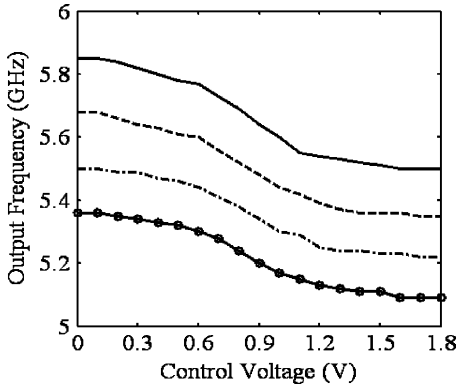

Fig. 4. Measured tuning characteristics of the VCO. (—) $(b_0, b_1, b_2) = (0, 0, 0)$. $(- - -)$ $(b_0, b_1, b_2) = (1, 0, 0)$. $(- \cdot -)$: $(b_0, b_1, b_2) = (1, 1, 0)$. $(- \circ -)$: $(b_0, b_1, b_2) = (1, 1, 1)$.

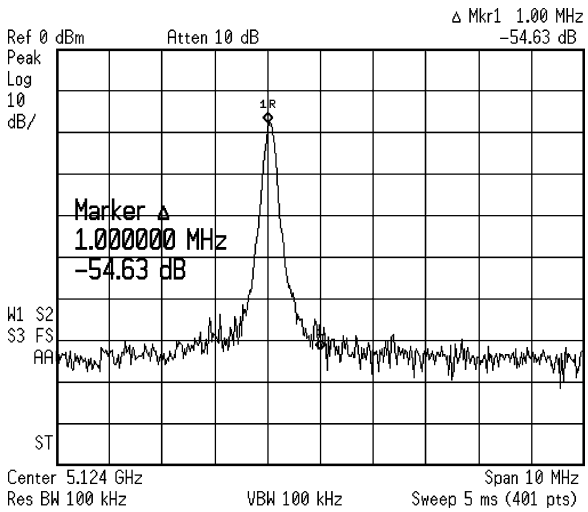

Fig. 5. Measured phase noise of the free-running VCO with the tuning voltage of 1.2 V.

frequency range is between 5.09 and 5.83 GHz, covering the three IEEE 802.11a bands.

Fig. 5 shows the measurement result of the free-running VCO at the supply voltage of 1.8 V and the bias current of 1.6 mA. The buffer consumes 4 mW. When the control voltage is set to 1.2 V and bits b_0 to b_2 are set high to turn on the three switches, the oscillation frequency is 5.12 GHz, and the output power is about -18 dBm. The noise power measured in a 100-kHz bandwidth at an offset of 1 MHz is -72.6 dBm; hence, the phase noise is $-72.6\ \text{dBm} + 18\ \text{dBm} - 10\log 100\ \text{k} = -104.6$ dBc/Hz. The VCO gain is $K_{\text{vco}} = 200$MHz/v, which is relatively small to ensure low phase noise and low spur.

B. ILFD

In order to reduce the power consumption in the digital circuit, an ILFD is used as the first divider of the feedback loop. The ILFD based on ring oscillator can reduce the chip size. From our frequency planning, the use of a divide-by-five frequency divider at the first stage of the feedback loop can also reduce power consumption. Hence, the adoption of ILFD is an effective and simple solution.

Fig. 6 shows the functional diagram of an ILFD, which consists of a mixer and a frequency-selective module, usually a

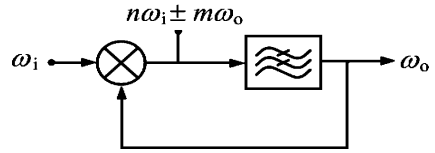

Fig. 6. Functional diagram of ILFD.

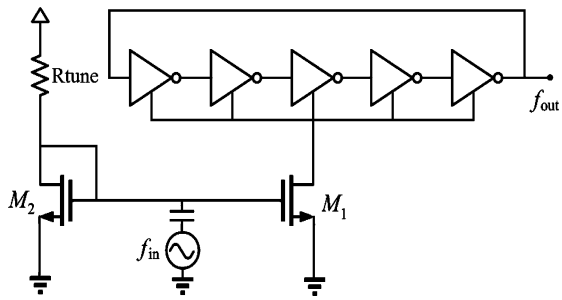

Fig. 7. Schematic of inverter-based ILFD with modulus 5.

low-pass or bandpass filter. The input signal ω_{i} and the output signal ω_{o} are mixed to generate multiple harmonics of $n\omega_{\text{i}} \pm m\omega_{\text{o}}$. The frequency-selective module passes the intended tone, $n\omega_{\text{i}}/N$, which is a fraction of the input frequency, and suppresses all the other harmonics [6].

Fig. 7 shows the schematic of the ILFD with modulus 5. An inverter-based amplifier is used to insert enough delay. The signal from the VCO output is injected into the gate of M_1 which also forms a current-reuse structure to reduce power consumption. The dimensions of inverter are chosen to provide low-pass filtering and keep the close-loop gain greater than unity. The upper bound of operating frequency is mainly limited by the loading capacitance due to the output buffers. The locking range of the ILFD can be increased by injecting stronger signal and adopting a ring oscillator with lower Q factor.

As shown in Fig. 7, based on the basic theorem of injection locking, only the desired tone is sustained in the feedback loop when the loop is locked. When there is no injection signal, the five-stage ring oscillator will resonate at frequency f_0. Only when the injection signal from the drain of M_1 is at 5 f_0 will the loop be locked. Hence, M_1 serves as an injector as well as an amplifier. The locking range is related to the bias current of M_1, the input signal amplitude, and the number of stages used in the ring oscillator. The more stages are used, the more parasitic capacitance between the drain of M_1 to ground will appear and, thus, reduce the locking range. The off-chip resistor R_{tune} is used to adjust the bias current of M_1. The proposed ILFD has a locking range of 400 MHz (5.035–5.435 GHz) and consumes 1.5 mW of power.

Based on the symbols in [11], let $v_{\text{in}} = V_{\text{dc}} + V_1 \cos(M\omega_0 t + \alpha)$ and $v_{\text{out}} = V_2 \cos(\omega_0 t + \varphi)$ be the input and output signals, respectively. The output phase of the ILFD can be perturbed by the phase noise of the input signal and the internal phase noise of ILFD. In the steady state, there is a fixed phase relationship between α and φ. If α is fixed while φ deviates slightly from its steady-state value due to internal noise, it will eventually return to its steady-state value. If α jumps to a different value, then φ will eventually stabilize to a new steady-state value in the

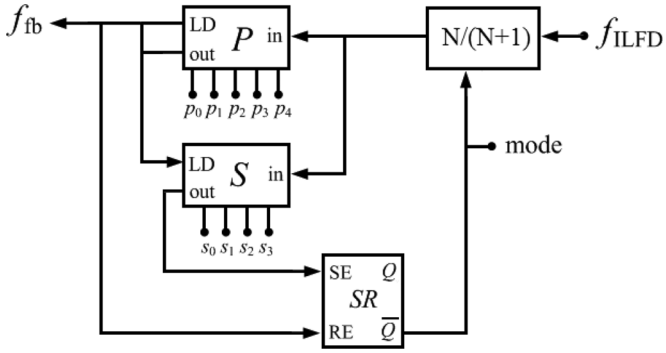

Fig. 8. Block diagram of pulse swallow frequency divider. Mode 1: ÷17. Mode 0: ÷16.

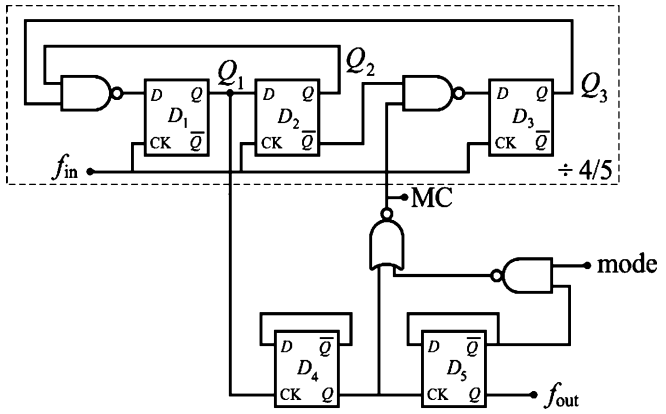

Fig. 9. ÷16/17 dual-modulus prescaler in pulse swallow frequency divider. $f_{\rm in}$ is the output frequency of ILFD. $f_{\rm out}$ is connected to P and S counters.

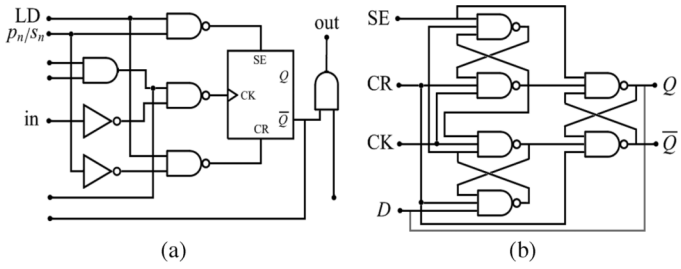

Fig. 10. (a) One-bit counter cell in the P counter (n: 0–4) and the S counter (n: 0–3). (b) D flip-flop in (a).

absence of noise. In [12], an ILFD consisting of a ring oscillator is proposed, which has the injection frequency of 1 GHz, phase noise at 100 kHz of −110 dBc/Hz, and core power consumption of 350 μW.

C. Pulse Swallow Frequency Divider

Fig. 8 shows the pulse swallow frequency divider which is composed of a $\div N/(N+1)$ prescaler, a programmable counter, and a swallow counter. If the prescaler is set at mode 1, the divisor $N+1$ will be selected. The P and the S counters divide the output signal frequency of the prescaler simultaneously. Note that the content of P must be greater than that of S. The S counter will reach the full state before the P counter then generates an output signal to reset the SR latch. By this time, the input port has received $(N+1)S$ cycles, and the mode is switched to zero, and the prescaler will divide the input frequency by N. The P counter takes $P-S$ cycles at its input to reach the full state, hence $(P-S)N$ pulses will be received at the input port before then, and an output signal is generated. Then, the P and the S counters will be reset by the output signal; the SR latch will also be reset and switch to mode 1, back to the initial status.

As a consequence, the total number of input pulses required to generate one output pulse is $(N+1)S+(P-S)N = NP+S$, implying

$$f_{\rm fb} = \frac{1}{NP+S} f_{\rm ILFD}$$

where $f_{\rm ILFD}$ is the output frequency of ILFD and $f_{\rm fb}$ is the feedback frequency of the PLL. In this design, $N = 16$, and the P and S counters have 5 and 4 bit, respectively. Thus, the division ratio ranges from 259 to 266.

Fig. 9 shows the ÷16/17 dual-modulus prescaler, which consists of a ÷4/5 counter, two D flip-flops, and two NAND gates. When mode is set to low, D_3 will be disabled, and the ÷4/5 counter will work in the ÷4 mode. The output Q_1 is divided by the asynchronous ÷4 circuit, and the input clock $f_{\rm in}$ is divided by 16. When mode is set to high, the ÷4/5 counter will work in the ÷4 mode in the first three cycles, and in the ÷5 mode, in the last cycle when $\rm MC = 1$. Thus, the modulus becomes $4 \times 3 + 5 \times (4-3) = 17$.

The pulse counter and the swallow counter can be implemented using programmable down counter. Fig. 10(a) shows the schematic of 1-bit counter cell in the programmable down counter. Note that $\overline{Q}$ and D in the D flip-flop of the counter cell are connected together as shown in Fig. 10(b). When $\rm LD = 1$, the counter is programmed by presetting the flip-flops according to the input. When $\rm LD = 0$, the counter starts to count down. If the output signal $f_{\rm out}$ is connected to LD, an output pulse of $f_{\rm out}$ will reset the input, and the counter starts counting down from the preset value. Another output pulse will appear when the counter counts down to zero and a new cycle begins. Thus, the down counter works as a frequency divider.

D. PFD

Fig. 11 shows a dynamic PFD. The PFD compares the phase and frequency between the reference signal and the feedback signal to generate an up or down signal to the CP. In order to operate at high speed with a small dead zone, the dynamic PFD in [7] is chosen. The dynamic PFD generates glitch at both output nodes in every period of the reference signal after the PLL is locked. Thus, additional logic gates are used to remove the glitch.

E. CP

Fig. 12 shows the circuit diagram of the CP and loop filter. The signal at node X is sent to the loop filter. The loop filter converts the digital signal to an analog signal to tune the output frequency of the VCO. Possible mismatch between pMOS and nMOS is avoided by using only nMOS switches [8]. The current sources are always turned on, and the nMOS switches are used to steer the current from one branch of the CP to the other.

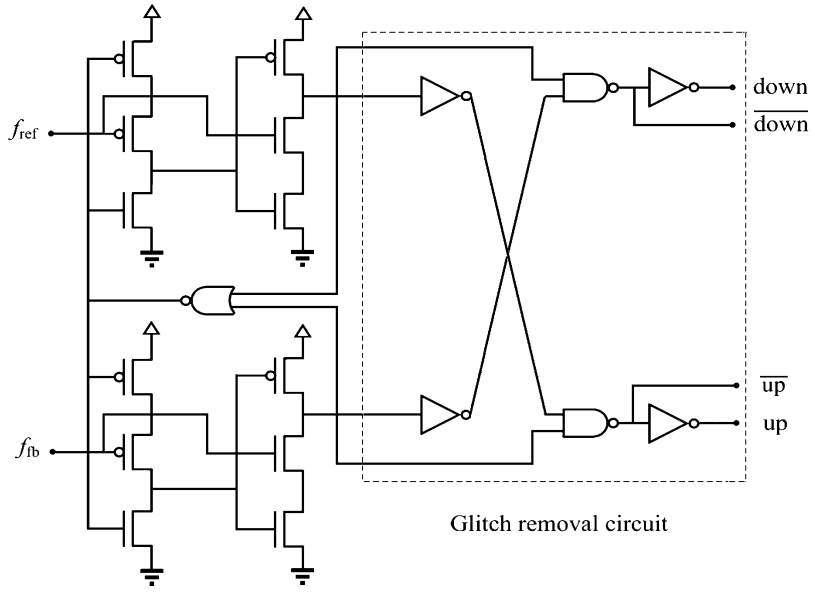

Fig. 11. Dynamic PFD with glitch removal circuit.

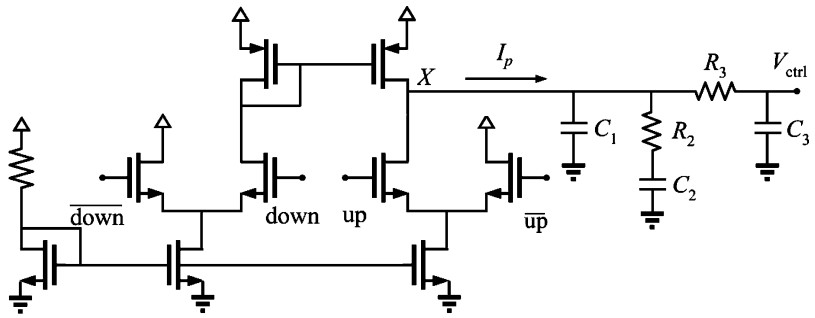

Fig. 12. Schematic of nMOS CP and loop filter.

F. Loop Filter

A third-order loop filter follows the CP as shown in Fig. 12. Resistor R_2 and capacitor C_2 in the loop filter generate a pole at the origin and a zero at $1/(R_2C_2)$. The current switching noise at the reference frequency in the CP circuit may cause unwanted FM sidebands at the output of VCO to interfere the adjacent channels. Capacitor C_1 and the combination of R_3 and C_3 are used to insert extra poles at frequencies higher than the PLL bandwidth to reduce the feedthrough at the reference frequency and decrease spurious sidebands at harmonics of the reference frequency.

The thermal noise at R_2 and R_3 will directly modulate the VCO control voltage and can incur substantial phase noise in the VCO. The capacitances and resistances of the loop filter are designed to perform the required filtering while keeping the loop stable and creating as little noise as possible [9].

In this paper, an off-chip third-order loop filter is designed with [10]

$$C_1 = \frac{T_1}{T_2}\frac{2\pi K_{\rm d}K_{\rm vco}}{M\omega_c^2}\sqrt{\frac{1+\omega_c^2T_2^2}{(1+\omega_c^2T_1^2)(1+\omega_c^2T_3^2)}}$$
$$C_2 = C_1\left(\frac{T_2}{T_1}-1\right) \quad R_2 = \frac{T_2}{C_2}$$
$$C_3 = \frac{C_1}{10} \quad R_3 = \frac{T_3}{C_3}$$

where M is the ratio of $f_{\rm out}/f_{\rm ref}$. The time constants T_1, T_2, and T_3 of the third-order filter are

$$T_1 = \frac{\sec\phi_p - \tan\phi_p}{\omega_p}$$
$$T_2 = \frac{1}{(T_1+T_3)\omega_c^2}$$
$$T_3 = \frac{\sqrt{10^{\alpha/10}-1}}{2\pi f_{\rm ref}}$$

where

$$\omega_c = \frac{(T_1+T_3)\tan\phi_p}{(T_1+T_3)^2+T_1T_3}\left[\sqrt{1+\frac{(T_1+T_3)^2+T_1T_3}{[(T_1+T_3)\tan\phi_p]^2}}-1\right]$$

is the third-order open-loop unity-gain frequency (loop bandwidth), ω_p and ϕ_p are the loop bandwidth and phase margin, respectively, of the second-order loop filter, and α is the spurs attenuation. In this paper, we choose $K_{\rm vco} = 200$ MHz/v, $I_p = 200\,\mu$A, $\phi_p = 65^\circ$, $C_1 = 38$ pF, $C_2 = 0.387$ nF, $R_2 = 8.3\,\text{k}\Omega$, $C_3 = 3.8$ pF, and $R_3 = 31.3\,\text{k}\Omega$.

G. Preamplifier

Fig. 13 shows the preamplifier used to amplify the signal after VCO and ILFD, respectively. It is composed of a three-stage high-gain inverter-based amplifier and a dc-level shift. In order

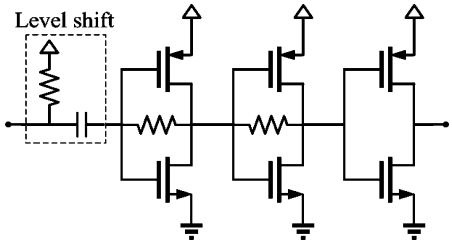

Fig. 13. Schematic of preamplifier used at the output of VCO and ILFD, respectively.

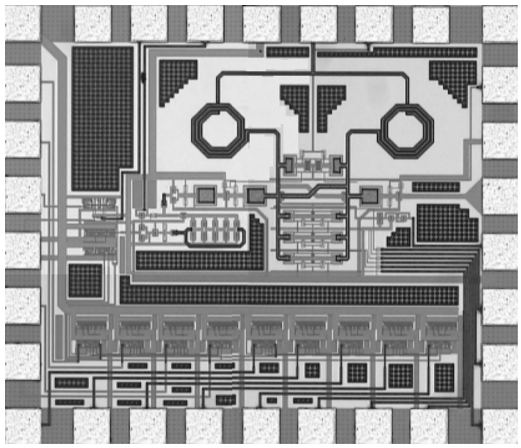

Fig. 14. Die micrograph of the proposed synthesizer. Chip size is 0.95 mm × 1.1 mm.

to generate a full-swing square wave at the output of ILFD, the dc-level shift is biased at $V_{\rm DD}/2$.

IV. Results and Discussions

The frequency synthesizer is designed and fabricated in the 0.18-μm CMOS technology. Fig. 14 shows the die micrograph of the synthesizer; its size is 1.1 mm × 0.95 mm, including the pads. The pads of dc supply, ground, and digital control lines are wire-bonded to the test board. An Agilent E4408B spectrum analyzer and an Amrel FG-506 function generator are used to measure the synthesizer parameters.

To compensate for the process tolerance, a 3-bit DSCA is designed to fine tune the free-running VCO. The synthesizer is tested with a reference signal of 4 MHz under closed-loop measurements. If the P counter is set to 16, $(p_0, p_1, p_2, p_3, p_4) = (0, 0, 0, 0, 1)$, and the S counter is set to to 6, $(s_0, s_1, s_2, s_3) = (0, 1, 1, 0)$, channel 4 will be selected. Fig. 15 shows the output spectrum of the PLL in the locked state. The output frequency is 5.24 GHz, verifying that the division ratio is 1310. The prescaler works properly without any glitch phenomenon. The spur at 4-MHz offset is lower than the intended carrier by 40 dB. The parameters of the proposed synthesizer are summarized in Table II.

V. Conclusion

A 5-GHz synthesizer has been designed and fabricated in a 0.18-μm CMOS technology. The ILFD is used as the first divider in the PLL feedback loop to reduce the power consumption in the digital circuits. The synthesizer chip consumes 18 mW of power at 1.8-V supply voltage, of which only 3.93 mW is consumed by the VCO and the ILFD. The VCO has a phase noise of −104 dBc/Hz at the frequency offset of 1 MHz and has an output tuning range of 740 MHz. The spurious tone at 4-MHz offset is lower than the intended carrier by 40 dB. The chip size is 0.95 mm × 1.1 mm.

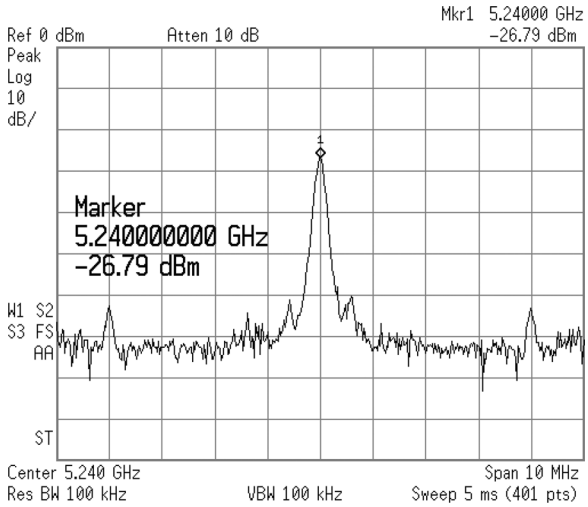

Fig. 15. Measured output spectrum of the synthesizer.

TABLE II
Measured Synthesizer Parameters

Parameter	Result
Technology	0.18 μm CMOS
Synthesizer frequency	5.15-5.35 GHz
Reference frequency	4 MHz
Channel spacing	20 MHz
Number of channels	7
Reference spurs	−40 dBc
VCO phase noise	−104 dBc/Hz @ 1MHz
Loop bandwidth	200 kHz
Supply voltage	1.8 V
Power dissipation	18 mW
Die area	0.95 mm × 1.1 mm

Acknowledgment

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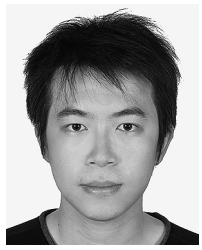

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