RFID Regulator Design Insensitive to Supply Voltage Ripple and Temperature Variation

Chi-En Liu, Yi-Jhan Hsieh, and Jean-Fu Kiang, *Member, IEEE*

***Abstract*—A regulator is designed for radio-frequency identification tags in the ultrahigh-frequency band using the Taiwan Semiconductor Manufacturing Company 0.18-μm CMOS process. A stable reference voltage with short calibration time is designed by integrating a ripple stabilizer and a temperature stabilizer. The regulator output exhibits a line regulation and load regulation of 12 mV/V and 0.34 mV/mA, respectively, and its power supply rejection ratio is 35.1 dB at 1 MHz.**

***Index Terms*—Regulator, ripple stabilizer, temperature stabilizer.**

I. Introduction

RADIO-FREQUENCY identification (RFID) technology has found immense applications in recent years, for example, to retrieve information from a large number of items quickly, easily, and correctly. The RFID tags can roughly be categorized into active and passive ones. An active tag requires a battery to power its circuitry. A passive tag, on the other hand, converts electromagnetic radiation into electricity, usually via a rectifier and a regulator.

In [1], a regulator is proposed, which has a low quiescent current of 110 nA, and its output ripple is less than 0.3 V. In [2], a regulator is designed with the power supply rejection ratio (PSRR) of about -60 dB at 100 kHz; however, its operation is sensitive to temperature variation. In [3], a regulator with an output voltage of 3.3 V and a current of 2 mA is proposed; however, its bias circuit is unregulated and demands a high PSRR. In [4], four series diodes are used to constrain the large output swing of a regulator. A multistage cascode current mirror with the NMOS operating in the subthreshold region tends to consume less power, but its operation is sensitive to temperature variation.

In [5], a limiter is proposed to protect the main circuit from breakdown by a large voltage swing. However, a relatively large ripple after the limiter may still disable the main circuit. In [6], a passive RFID transponder integrated circuit is designed with a voltage multiplier to drain its dc power from the incident wave. However, no voltage regulator is accompanied to stabilize the voltage level. In [7], a mirror voltage line is proposed to release excess charges into two capacitors, but it is sensitive to temperature variation, and an offset bias current is required for proper operation.

In [8], a transponder for long-range telemetry is proposed, in which a voltage multiplier consisting of 16 cascaded stages is integrated to provide a 3-V dc supply from a -12.3-dBm incident RF signal. However, no regulator is designed to reduce the possible voltage variation. In [9], an operational amplifier (OPA) is used to design a regulator that controls a bypass element to release the overcurrent. However, the OPA consumes too much power and requires a high PSRR to reject supply voltage ripples. In [10], a bandgap reference circuit and an operational transconductance amplifier (OTA) are integrated to supply 2 mA of current at the output voltage of 3 V. However, the OTA consumes a quiescent power of $5I_{\rm bias}$ in order to maintain a high slew rate. A high-PSRR regulator is proposed in [11], but the voltage gain of the OPA is not high enough to work beyond 1 MHz.

In [12], the relation between load current and the frequency response of a gain stage is utilized to reduce the quiescent current. However, the noise rejection function of the OPA is degraded because the current mirror is directly connected to the supply voltage. In [13], a regulator is designed by cascading two wideband OTAs to replace the Miller capacitor for frequency compensation, hence improving the performance of both frequency and transient responses. However, the consumed power is doubled because two OTAs are used. In [14], an internal circuit is designed to replace an effective series resistor otherwise used to create a zero for frequency compensation. However, the circuit has relatively low immunity to voltage ripple. In [15], damping factor control is adopted for frequency compensation in a regulator; hence, the regulator has low line and load regulations even without the feedback capacitor.

In this brief, we propose a regulator that can effectively reject voltage ripples at 1 MHz. A brief overview on the associated tag system is given in Section II. Design issues of the regulator are presented in Section III, and simulation and measurement results are presented in Section IV, followed by the conclusion.

II. Overview of Tag System

RFID tags in the UHF band can respond to a reader with RF pulses. As shown in Fig. 1, the reader emits a continuous wave without modulation. A bit 0 is echoed by the tag via adjusting its impedance to match with the antenna impedance, thus scattering very little power back to the reader. On the other hand, a bit 1 is echoed by the tag via adjusting its input impedance to a lower value, thus scattering more RF power back to the reader. The RF power available to the tag chip will

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The authors are with the Department of Electrical Engineering and the Graduate Institute of Communication Engineering, National Taiwan University, Taipei 106, Taiwan (e-mail: jfkiang@cc.ee.ntu.edu.tw).

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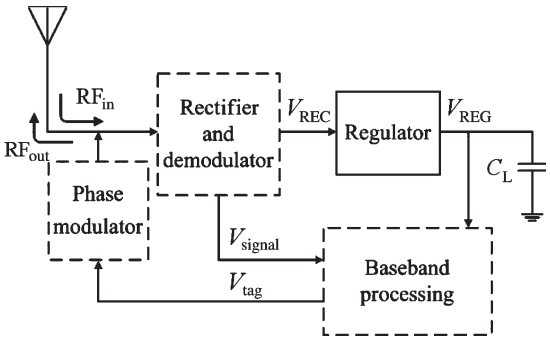

Fig. 1. Voltage regulator for RFID tag.

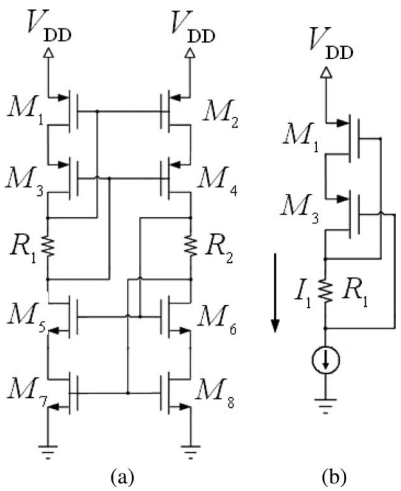

Fig. 2. Schematic of the ripple stabilizer. (a) Cascode current mirror. (b) Diodelike pair with self-bias.

drive a voltage regulator to charge an on-chip capacitor C_L for storage.

An ideal voltage regulator is expected to maintain a constant dc voltage level independent of the amount of power received by the antenna or consumed by the tag circuitry. It is required to consume power less than a few tens of microwatts, and its temperature coefficient (TC) is preferred to be zero at room temperature.

III. Design Issues

A. Ripple Stabilizer

Fig. 2 shows the ripple stabilizer used in this design. A cascode current mirror is adopted to maintain a reference current insensitive to supply voltage variation. The first current mirror consists of four PMOSs M_1, M_2, M_3, and M_4. The current I_2 closely matches I_1 if M_1 and M_3 match M_2 and M_4, respectively. The second current mirror consisting of NMOSs M_5–M_8 makes I_1 follow I_2 if M_5 and M_7 match M_6 and M_8, respectively. Since each diodelike pair (M_1 and M_3 as well as M_6 and M_8) is fed by a constant-current source, I_1 and I_2 are relatively independent of $V_{\rm DD}$ variation. The cascode of M_5 and M_7 increases the output impedance looking from the diodelike pair M_1 and M_3; hence, the reference current becomes less sensitive to voltage ripple at $V_{\rm DD}$.

Resistances R_1 and R_2 are properly adjusted so that all the MOSFETs are biased in the saturation region. Referring to Fig. 2(b), $v_{\rm SD1} > v_{\rm SG1} - |V_{\rm th1}|$ and $v_{\rm SD3} > v_{\rm SG3} - |V_{\rm th3}|$ if M_1 and M_3 operate in the saturation region, where $V_{\rm th1}$ and $V_{\rm th3}$ are the threshold voltages of M_1 and M_3, respectively. The voltage drop across R_2 can be expressed as

$$I_1 R_2 = v_{\rm SG3} - v_{\rm SD3} < v_{\rm SG3} - v_{\rm SG3} + |V_{\rm th3}| = |V_{\rm th3}|$$

hence

$$I_1 < \frac{|V_{\rm th3}|}{R_2}. \tag{1}$$

Furthermore, since

$$v_{\rm SD3} + I_1 R_2 = v_{\rm SG3} > |V_{\rm th3}|$$
$$v_{\rm SD3} = v_{\rm DG1} = v_{\rm SG1} - v_{\rm SD1} < |V_{\rm th1}|$$

we have

$$I_1 > \frac{|V_{\rm th3}| - |V_{\rm th1}|}{R_2}. \tag{2}$$

A similar analysis can be applied to M_6 and M_8 to derive the condition that

$$\frac{V_{\rm th6} - V_{\rm th8}}{R_1} < I_2 < \frac{V_{\rm th6}}{R_1}. \tag{3}$$

Equations (1) and (2) are used to determine the range of the reference current I_1 and resistance R_2.

A systematic approach is taken to adjust the proper W/L value for each MOS as follows: 1) Choose R_1 and R_2 around several kΩ. 2) Simulate the circuit in Fig. 2(b) with constant-current source based on (1) and (2). The constant current I_2 via M_6 and M_8 is required to satisfy (7). 3) Adjust the W/L value of M_1, M_3, M_6, and M_8 such that they all operate far away from the edge of the triode region. If $I_1 = I_2$, the size of M_2, M_4, M_5, and M_7 must be the same as that of M_1, M_3, M_6, and M_8, respectively. 4) Stack the two cascode current mirrors, run simulation to check whether the currents I_1 and I_2 are continuous at both cascodes. If the currents do not match, adjust I_1 and I_2 and then go back to step 1.

B. Temperature Stabilizer

The threshold voltage across the p-n junction of either a diode or a bipolar junction transistor (BJT) exhibits a negative TC. The collector current of a BJT is related to its emitter–base voltage as

$$I_C = I_S \exp(v_{\rm EB}/V_T) \quad \text{or} \quad v_{\rm EB} = V_T \ln(I_C/I_S) \tag{4}$$

where V_T is the thermal voltage, I_C and $I_S = A\mu\kappa T n_i^2$ are the collector current and saturation current, respectively, μ is the mobility of minority carriers, n_i is the intrinsic minority carrier concentraion in the silicon, $\kappa \simeq 1.38 \times 10^{-23}$ J/K is Boltzmann's constant, and A is a proportional constant. These parameters depend on the temperature as $\mu \propto \mu_0 T^m$, with $m \simeq -1.4$, and $n_i^2 \propto T^3 \exp[-E_g/(\kappa T)]$, where the bandgap

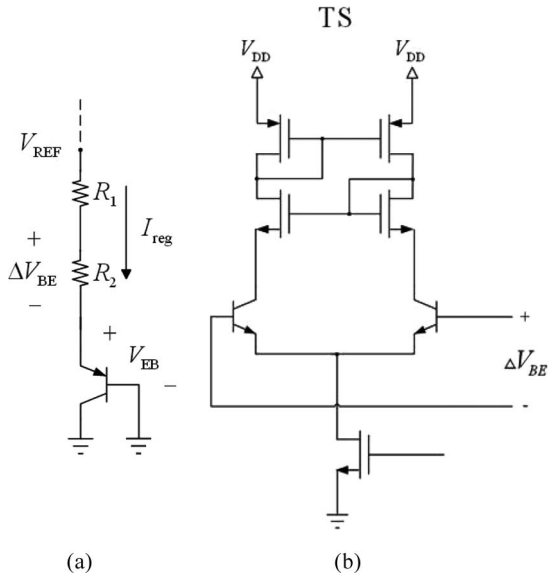

Fig. 3. Schematic of bandgap reference generator. (a) Zero-TC voltage reference. (b) $\Delta V_{\rm BE}$ generation circuit, TS stands for temperature stabilizer.

energy of silicon is $E_g \simeq 1.12$ eV. With these parameters, I_S can be expressed as

$$I_S = BT^{4+m} \exp\left(\frac{-E_g}{\kappa T}\right) \tag{5}$$

where B is another proportional constant. Thus, we have

$$\begin{aligned}\frac{\partial I_S}{\partial T} &= B(4+m)T^{3+m} \exp\left(\frac{-E_g}{\kappa T}\right) \\ &\quad + BT^{4+m} \exp\left(\frac{-E_g}{\kappa T}\right)\left(\frac{E_g}{\kappa T^2}\right) \\ \frac{V_T}{I_S}\frac{\partial I_S}{\partial T} &= (4+m)\frac{V_T}{T} + \frac{E_g}{\kappa T^2}V_T. \end{aligned} \tag{6}$$

Next, take the derivative of $v_{\rm EB}$ in (4) with respect to T to have

$$\begin{aligned}\frac{\partial v_{\rm EB}}{\partial T} &= \frac{\partial V_T}{\partial T}\ln\left(\frac{I_C}{I_S}\right) - \frac{V_T}{I_S}\frac{\partial I_S}{\partial T} + \frac{V_T}{I_C}\frac{\partial I_C}{\partial T} \\ &= \frac{v_{\rm EB} - (4+m)V_T - E_g/q}{T} + \frac{V_T}{I_C}\frac{\partial I_C}{\partial T} \end{aligned} \tag{7}$$

where $q = 1.6 \times 10^{-19}$ C.

Figs. 3(a) and (b) show the bandgap reference generator and the $\Delta V_{\rm BE}$ generation circuit, respectively. In Fig. 3(a), substitute $I_C \simeq I_{\rm reg} = V_T \ln n/R_2$ and $\partial I_{\rm reg}/\partial T = V_T \ln n/R_2 T = I_{\rm reg}/T$ into (7) to have

$$\begin{aligned}\frac{\partial v_{\rm EB}}{\partial T} &= \frac{v_{\rm EB} - (4+m)V_T - E_g/q}{T} + \frac{V_T}{I_{\rm reg}}\frac{\partial I_{\rm reg}}{\partial T} \\ &= \frac{v_{\rm EB} - (3+m)V_T - E_g/q}{T}. \end{aligned} \tag{8}$$

Let $v_{\rm EB} \simeq 750$ mV and $T = 300$ K, we obtain $\partial V_{\rm EB}/\partial T \simeq -1.417$ mV/K.

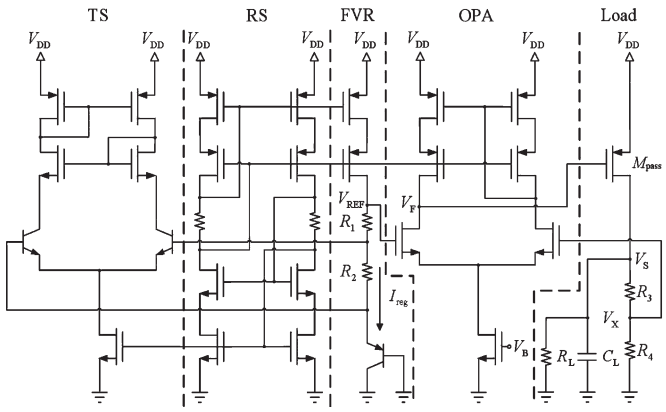

Fig. 4. Schematic of proposed regulator: TS: temperature stabilizer; RS: ripple stabilizer; FVR: fixed voltage reference; OPA: operational amplifier.

If the currents through two identical bipolar transistors are different by a ratio n, the difference between their base–emitter voltages is directly proportional to the absolute temperature as [16]

$$\Delta V_{\rm BE} = V_T \ln n$$

which implies that

$$\frac{\partial \Delta V_{\rm BE}}{\partial T} = \frac{\kappa}{q}\ln n. \tag{9}$$

Apply (9) to the two identical BJTs Q_1 and Q_2 in Fig. 3(b) where the current through Q_2 is n times that through Q_1. As shown in Fig. 3(a), $\Delta V_{\rm BE}$ with a positive TC is superimposed on $V_{\rm EB}$ with a negative TC to have

$$\begin{aligned} V_{\rm REF} &= \left(1 + \frac{R_1}{R_2}\right)\Delta V_{\rm BE} + V_{\rm EB} \\ \frac{\partial V_{\rm REF}}{\partial T} &= \left(1 + \frac{R_1}{R_2}\right)\frac{\kappa}{q}\ln n + \frac{V_{\rm BE} - (4+m)V_T - E_g/q}{T}. \end{aligned}$$

Let $R_1/R_2 = 24$ and $n = 2$; the derivative of $V_{\rm REF}$ with respect to T is close to zero around $T = 300$ K. Here, a smaller derivative means the reference voltage $V_{\rm REF}$ is less sensitive to temperature variation.

C. Complete Circuit

Fig. 4 shows the schematic of the complete regulator, in which $I_{\rm reg}$ is insensitive to voltage ripples. The voltage $V_{\rm REF}$ is insensitive to either ripple voltage or temperature variation, making it a stable reference for the OPA.

The ripple stabilizer, temperature stabilizer, and OPA are all designed with a cascode current mirror so that voltage ripples in $V_{\rm DD}$ induce only negligible current variation. R_L and C_L represent the load from the subsequent stage, and V_S is the regulated supply voltage. The ratio R_3/R_4 is adjusted to make $V_X \simeq V_{\rm REF}$; a large W/L ratio of $M_{\rm pass}$ is required to provide sufficient load current.

If a sinusoidal ripple waveform $V_{\rm ripple}$ appears on $V_{\rm DD}$, the current via $M_{\rm pass}$ will increase during the postive half period of $V_{\rm ripple}$, hence pulling V_S and V_X up. The increase of V_X will

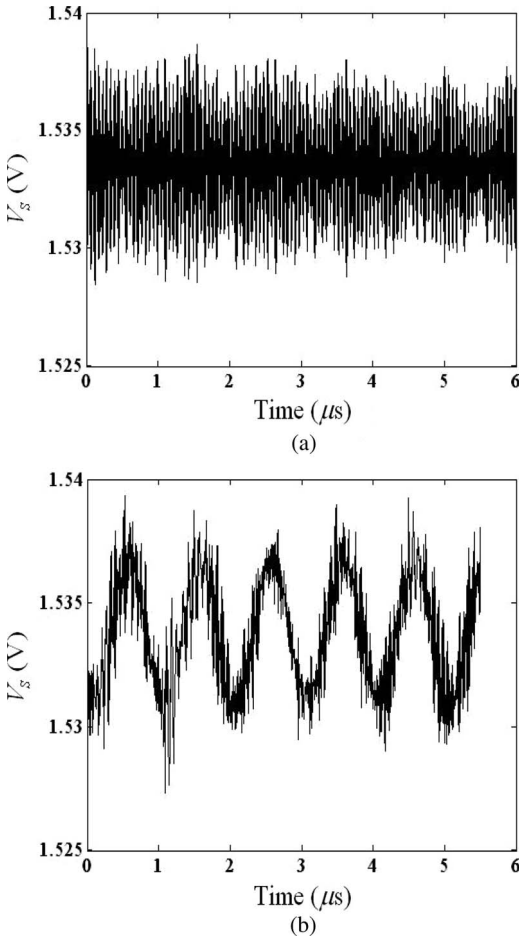

Fig. 5. Variation of V_S with a perturbation of $A_r \times \sin(2\pi \times 10^6 t)$ mV superimposed on $V_{\rm DD}$. (a) $A_r = 50$ mV. (b) $A_r = 200$ mV.

activate the OPA to increase the voltage V_F, hence decreasing the conducting current via $M_{\rm pass}$. Thus, V_S will be brought back to its original dc level. On the other hand, the negative half period of $V_{\rm ripple}$ causes a voltage drop at V_S and V_X. The decrease of V_X will activate the OPA to decrease the voltage V_F, hence increasing the conducting current via $M_{\rm pass}$. Since $V_{\rm REF}$ is insensitive to ripple voltage and temperature variation, so is the regulated voltage V_S.

IV. Results and Discussions

The quality of a regulator is conventionally measured in terms of line regulation (LIR), load regulation (LOR), and power supply ripple rejection (PSRR), defined as

$$\text{LIR} = \frac{\Delta V_o}{\Delta V_{\rm DD}} \qquad \text{LOR} = \frac{\Delta V_o}{\Delta I_L}$$

$$\text{PSRR} = 20\log_{10}\frac{\Delta V_{\rm DD}}{\Delta V_o}$$

where V_o is the reference voltage of concern.

Fig. 5(a) shows the simulated variation of V_S, given a ripple voltage at $V_{\rm DD}$ of $A_r \times \sin(2\pi f_r t)$ mV, with $A_r = 50$ mV and $f_r = 1$ MHz. The output voltage of V_S is about 1.5 V, the LIR is about 12 mV/V, the voltage swing of V_S is about 0.68 mV, and the LOR is about 0.34 mV/mA. Fig. 5(b) shows the simulated variation of V_S with $A_r = 200$ mV. The LIR, LOR, and voltage swing of V_S are almost the same as those with $A_r = 50$ mV. The peak-to-peak variation is 400 mV, and the output voltage swing is about 7 mV; hence, PSRR $= 20\log_{10}(400/7) \simeq 35.1$ dB.

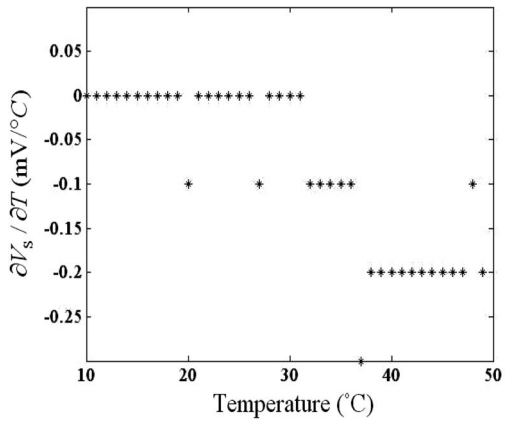

Fig. 6. TC at V_S, with $V_o = 1.316$ V.

These two cases have also been measured. Variation around the unperturbed voltage level is hardly observable because the ripple at V_S is smaller than the dc noise.

Fig. 6 shows the TC at V_s over the temperature range from 10 °C to 50 °C. The magnitude of the TC is less than 0.2 mV/°C and is close to zero below 37 °C.

V. Conclusion

A regulator for RFID tags in the UHF band has been designed and implemented using the Taiwan Semiconductor Manufacturing Company 0.18-μm CMOS process. A ripple stabilizer and a temperature stabilizer have been integrated to maintain a stable reference voltage that is insensitive to temperature variation and voltage ripple. This regulator has an LIR and LOR of 12 mV/V and 0.34 mV/mA, respectively, and its PSRR is 35.1 dB at 1-MHz sinusoidal ripple.

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