Design Constraints on FSC LCD

I-Yin Li, *Member, IEEE*, and Jean-Fu Kiang, *Member, IEEE*

***Abstract*—Design constraints on field-sequential color liquid crystal displays (LCDs) are proposed and compared with those of conventional color filter LCDs. Application of these constraints to the design of LCD screens is demonstrated.**

***Index Terms*—High-definition television (HDTV), liquid crystal display (LCD), power demand, thin-film transistor (TFT), TV display.**

I. Introduction

COMPARED with color filter (CF) liquid crystal displays (LCDs) of the same screen size, the field-sequential color (FSC) LCDs consume less power and can support a finer resolution. Under the same resolution, the pixel size of the FSC LCDs is three times that of the CF LCDs, while its charging time is one-third of the latter [1]. The FSC LCDs display a color image using the technique of temporal color mixture instead of the spatial color mixture; hence, the response of liquid crystal molecules and circuits must be three times faster than those of the CF LCDs.

In 1989, Kaneko developed a pixel model based on an equivalent circuit [2]; however, no design constraints were mentioned. In 1996, a dynamic analysis of an a-Si thin-film transistor LCD (TFT-LCD) pixel was presented by embedding an a-Si TFT model and a liquid cyrstal capacitance model in the simulation program with integrated circuit emphasis (SPICE) simulator [3], but no design constraints were discussed. Tsukada proposed a theory to analyze LCD subpixels [4], [5], but no systematic design procedure was proposed. In 1998, Tsukada proposed a scaling theory to analyze the gate delay and offset voltage in TFT-LCDs with narrow bus-line width and small pixel capacitance [6].

In 2001, Zhu presented the simulation results of kickback voltage on a-Si TFT-LCDs, with the orientation of liquid crystal molecules controlled by an imposed voltage [7]. Higuchi developed poly-Si TFT-LCDs using a dual-drive technique [8]. In 2006, Tai proposed the concept of operation window based on the mechanisms of charging, holding, coupling, and delay [9], which can be used to determine the pixel storage capacitance and the TFT channel width.

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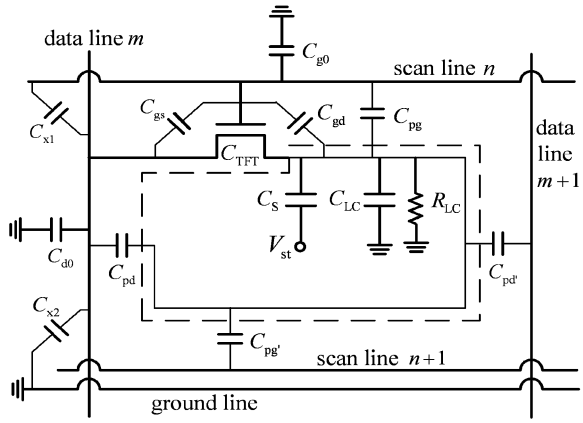

Fig. 1. Equivalent circuit of a pixel.

In this paper, an equivalent circuit of a supbixel is used to derive a set of design constraints for FSC LCDs. An operation window is, thus, built to analyze the difference between FSC LCDs and CF LCDs at various screen sizes. The models of pixel and signal line will be described in Section II. The constraints on pixel design will be presented in Section III. The pixel design for FSC LCDs will be proposed in Section IV. The assessment of different screen sizes based on these constraints will be discussed in Section V, which will be followed by the conclusions.

II. Models of Pixel and Signal Line

Fig. 1 shows the equivalent circuit of a pixel, where C_{LC} and R_{LC} are the capacitance and resistance, respectively, between the indium-tin-oxide (ITO) and the common electrode of a pixel. The pixel capacitance can be decomposed as [4]

$$\begin{aligned} C_{\rm px} &= C_S + C_{LC} + C_{\rm gd} + C_{\rm pd'} + C_{\rm pd} + C_{\rm pg'} + C_{\rm pg} \\ &\simeq C_S + C_{LC} \end{aligned}$$

where we assume that the parasitic capacitances $C_{\rm gd}$, $C_{\rm pd'}$, $C_{\rm pd}$, $C_{\rm pg'}$, and $C_{\rm pg}$ are much smaller than C_{LC} and the storage capacitance C_S.

To estimate the loading effect of a pixel on a scan line [9], [10], first calculate the equivalent resistance $R_{\rm scan}$ as

$$R_{\rm scan} = \rho_{\rm scan} \frac{L_{\rm scan}}{A_{\rm scan}}$$

where $A_{\rm scan} = t_{\rm scan} \times W_{\rm scan}$ is the cross-sectional area of the scan line, $\rho_{\rm scan}$, $W_{\rm sacn}$, and $t_{\rm scan}$ are the resistivity, width, and thickness, respectively, of the scan line, and $L_{\rm scan}$ is the length of the scan line across a pixel. The load capacitance $C_{\rm scan}$ can

be approximated as

$$C_{\rm scan} \simeq C_{\rm gs} + C_{\rm TFT} + C_{g0} + C_{x1} + C_{\rm gd} + C_{\rm pg} + C_{\rm pg'}. \quad (1)$$

Next, consider the loading effect of a pixel on a data line. The equivalent resistance $R_{\rm data}$ can be calculated as

$$R_{\rm data} = \rho_{\rm data} \frac{L_{\rm data}}{A_{\rm data}}$$

where $A_{\rm data} = t_{\rm data} \times W_{\rm data}$ is the cross-sectional area of the data line; $\rho_{\rm data}$, $W_{\rm data}$, and $t_{\rm data}$ are the resistivity, width, and thickness, respectively, of the data line; and $L_{\rm data}$ is the length of the data line across a pixel. The load capacitance $C_{\rm data}$ can be approximated as

$$C_{\rm data} \simeq C_{x1} + C_{x2} + C_{d0} + C_{\rm gs} + C_{\rm pd'} + C_{\rm pd}.$$

A scan line or a data line can be modeled as a lossy transmission line with the per-unit-length resistance and capacitance of R and C, respectively. Assume that the signal line has a finite length ℓ and is open circuited at $z = \ell$, and the driving voltage at $z = 0$ is a step function of time, then the waveform at $z = \ell$ will be [4]

$$\frac{v(\ell,t)}{V_g} = 1 + \frac{4}{\pi} \sum_{n=1}^{\infty} \frac{(-1)^n}{2n-1} \exp\left[-\frac{(2n-1)^2\pi^2}{4RC\ell^2}t\right]. \quad (2)$$

When $t > RC\ell^2$, (2) can be approximated as

$$\frac{v(\ell,t)}{V_g} \simeq 1 - \frac{4}{\pi}\exp\left(-\frac{\pi^2 t}{4RC\ell^2}\right).$$

Thus, it takes the delay time of $1.03RC\ell^2$, $1.96RC\ell^2$, and $2.25RC\ell^2$ for the voltage at the load to reach $v(\ell,t)/V_g = 90\%$, 99%, and 99.5%, respectively.

III. Constraints on Pixel Design

As shown in Fig. 1, the voltage V_e at the display electrode is a function of the data line voltage V_d as [5], [6]

$$V_e = \frac{1 - ae^{-t/\tau}}{1 - be^{-t/\tau}} V_d$$

with

$$a = \frac{V_d - V_{e0}}{V_d} \frac{2(V_s - V_t - V_d) + V_d}{2(V_s - V_t - V_d) + V_d - V_{e0}}$$

$$b = \frac{V_d - V_{e0}}{2(V_s - V_t - V_d) + V_d - V_{e0}}$$

$$\tau = \frac{C_{\rm px}}{\beta_0 (V_s - V_t - V_d)}$$

where V_s is the voltage on the scan line, V_t is the threshold voltage of the TFT, $V_{e0} = V_e(t=0)$, and $\beta_0 = \mu_{\rm eff} C_g W/L$ is a parameter determined by the TFT geometry and material [4]. The channel width W and length L of the TFT are the design parameters to be optimized.

A. Charging Phase

First, express the rise time t_r in units of τ as $t_r = k_t\tau$, and define the voltage ratio $r_c = V_e/V_d$, then k_t can be expressed as

$$k_t = \ln\frac{a - br_c}{1 - r_c}.$$

The rise time must be shorter than the period $T_{\rm row}$ allocated for displaying one row of pixels, deducting the delay over the scan line, namely

$$t_r < T_{\rm row} - T_{\rm delay}$$

where $T_{\rm delay}$ is the maximum allowable delay time over a scan line. Thus, we obtain the first constraint

$$\frac{W}{L} > \frac{C_{\rm px}}{\mu_{\rm eff} C_g (V_s - V_t - V_d)} \frac{k_t}{(T_{\rm row} - T_{\rm delay})}. \quad (3)$$

Note that the delay time along a sacn line depends on the TFT parameters. Hence, the maximum allowable delay time must be estimated iteratively, incorporating the other constraints that will be discussed later.

B. Holding Phase

In the holding phase, the charge leaks through the equivalent RC circuit formed by R_{LC}, $R_{\rm OFF}$, and $C_{\rm px}$, where $R_{\rm OFF} = V_{ed}/I_{\rm OFF}$ is the off-resistance of the TFT with $V_{ed} = V_e - V_d$ [10]. The time constant of the pixel during the holding phase is

$$\tau_{\rm px} = \frac{R_{LC} R_{\rm OFF}}{R_{LC} + R_{\rm OFF}} C_{\rm px}. \quad (4)$$

The leakage current $I_{\rm OFF}$ can be expressed as [10]

$$I_{\rm OFF} \simeq \frac{\sigma_D t_{\rm semi} V_{ed} W}{L}$$

where σ_D and $t_{\rm semi}$ are the dark conductivity and thickness, respectively, of the semicoductor layer.

Define the retention ratio in the holding phase as

$$r = e^{-T_{\rm frame}/\tau_{\rm px}}.$$

To display a distortion-free image, the voltage deviation due to leakage must be less than one gray level, which leads to

$$r > 1 - \frac{1}{2^{N_{\rm bit}}} \quad (5)$$

where $N_{\rm bit}$ is the number of bits. Substituting (4) into (5), we obtain the second constraint

$$\frac{W}{L} < \frac{C_{\rm px}}{T_{\rm frame} 2^{N_{\rm bit}} \sigma_D t_{\rm semi}}. \quad (6)$$

C. Asymmetric Kickback

At the end of the charging phase, the TFT is turned off and the pixel is switched to the holding phase, the voltage at the gate terminal of $C_{\rm gd}$ is pulled low, and the display electrode at the other terminal of $C_{\rm gd}$ is pulled low too. By imposing the law of charge conservation and assuming that the scan pulse is a square pulse, a kickback voltage of magnitude [4]

$$\Delta V_{\rm kb} = (v_{s,\rm ON} - v_{s,\rm OFF}) \frac{C_{\rm gd} + C_{\rm pg}}{C_{\rm gd} + C_{\rm pg} + C_{LC}(V) + C_S}$$

will appear at the display electrode of the pixel, where $v_{s,\mathrm{ON}}$ and $v_{s,\mathrm{OFF}}$ are the voltages on the scan line at the ON and OFF states, respectively, C_{gd} is the parasitic capacitatance between the gate and the drain electrodes of TFT, and $C_{LC}(V)$ is the voltage across the pixel.

Define the deviation of ΔV_{kb} as

$$\begin{aligned}\Delta\left(\Delta V_{\mathrm{kb}}\right) &= \frac{\Delta V_{\mathrm{kb,max}} - \Delta V_{\mathrm{kb,min}}}{2} \\ &= \frac{\left(v_{s,\mathrm{ON}} - v_{s,\mathrm{OFF}}\right)\left(C_{\mathrm{gd}} + C_{\mathrm{pg}}\right)}{2\left(C_{\mathrm{gd}} + C_{\mathrm{pg}} + C_{LC,\mathrm{min}} + C_S\right)} \\ &\quad \frac{C_{LC,\mathrm{max}} - C_{LC,\mathrm{min}}}{C_{\mathrm{gd}} + C_{\mathrm{pg}} + C_{LC,\mathrm{max}} + C_S}. \end{aligned} \tag{7}$$

The average of ΔV_{kb} can be compensated by tuning the voltage level of the common electrode on the color filter substrate, but the voltage deviation $\Delta(\Delta V_{\mathrm{kb}})$ tends to induce a residual direct current with a preferred polarity, which will degrade the quality of the liquid crystal. Hence, $\Delta\left(\Delta V_{\mathrm{kb}}\right)$ must be constrained by an acceptable residual voltage threshold F_{kb} as [9]

$$\Delta\left(\Delta V_{\mathrm{kb}}\right) < F_{\mathrm{kb}}. \tag{8}$$

The capacitance C_{gd} can be expressed in terms of $\tilde{C}_{\mathrm{gd}}$, the gate-to-drain capacitance per unit channel width, as

$$C_{\mathrm{gd}} = \tilde{C}_{\mathrm{gd}} W. \tag{9}$$

Substituting (7) and (9) into (8), and assuming $C_{\mathrm{gd}} \ll C_{LC} + C_S$, a third design constraint is derived as (10) shown at the bottom of the page

D. Delay

To estimate the delay along a scan line using the lossy transmission line model, first approximate the per-unit-length resistance and capacitance along the scan line as $R = R_{\mathrm{scan}}/L_{\mathrm{scan}}$ and $C = C_{\mathrm{scan}}/L_{\mathrm{scan}}$, respectively. If there are N_{data} pixels along one scan line, the total length of the scan line will be $N_{\mathrm{data}} L_{\mathrm{scan}}$. The delay $t_{\mathrm{d,scan}}$ for the voltage to reach 90% of its intended level can, thus, be calculated as

$$t_{\mathrm{d,scan}} = 1.03 N_{\mathrm{data}}^2 R_{\mathrm{scan}} C_{\mathrm{scan}}. \tag{11}$$

This delay must be shorter than the specified T_{delay}, namely,

$$t_{\mathrm{d,scan}} < T_{\mathrm{delay}}. \tag{12}$$

Substituting (1) and (11) into (12), we obtain the fourth constraint on the channel width W as

$$W < \frac{\left(T_{\mathrm{delay}}/1.03 N_{\mathrm{data}}^2 R_{\mathrm{scan}}\right) - \left(C_{g0} + C_{x1} + C_{\mathrm{pg}} + C_{\mathrm{pg}'}\right)}{2\tilde{C}_{\mathrm{gd}} + \epsilon_{\mathrm{insu}}\epsilon_0 L/t_{\mathrm{insu}}}$$

where $C_{\mathrm{gs}} \simeq C_{\mathrm{gd}} = \tilde{C}_{\mathrm{gd}} W$, $C_{\mathrm{TFT}} = \epsilon_{\mathrm{insu}}\epsilon_0 WL/t_{\mathrm{insu}}$, and ϵ_{insu} and t_{insu} are the relative dielectric constant and thickness, respectively, of the insulator layer.

Similarly, one may substitute $R = R_{\mathrm{data}}/L_{\mathrm{data}}$ and $C = C_{\mathrm{data}}/L_{\mathrm{data}}$ into the lossy transmission line model to estimate the delay along a data line. Since a data line runs across N_{scan} rows of pixels, the total length of a data line is $N_{\mathrm{scan}} L_{\mathrm{data}}$; thus, we derive another constraint

$$W < \frac{\left(T_{\mathrm{delay}}/1.03 N_{\mathrm{scan}}^2 R_{\mathrm{data}}\right) - \left(C_{x1} + C_{x2} + C_{d0} + C_{\mathrm{pd}} + C_{\mathrm{pd}'}\right)}{\tilde{C}_{\mathrm{gd}}}.$$

IV. Pixel Design For FSC LCD

Under the same resolution and screen size, the frame period T_{frame} and the pixel size A_{pixel} of the FSC LCDs and the CF LCDs are related as

$$\begin{aligned} T_{\mathrm{frame,FSC}} &= \frac{1}{3} T_{\mathrm{frame,CF}} \\ A_{\mathrm{pixel,FSC}} &= 3 A_{\mathrm{subpixel,CF}}. \end{aligned}$$

As a consequence, $T_{\mathrm{row,FSC}} = 1/3 T_{\mathrm{row,CF}}$, $C_{LC,\mathrm{FSC}} = 3C_{LC,\mathrm{CF}}$, and $R_{LC,\mathrm{FSC}} = 1/3 R_{LC,\mathrm{CF}}$. Define the ratio between the size of storage capacitor and that of the pixel as $h = A_{C_S}/A_{\mathrm{pixel}}$, then $C_{\mathrm{px,FSC}}$ can be rephrased as

$$C_{\mathrm{px,FSC}} \simeq C_{LC,\mathrm{FSC}} \left(1 + \frac{\epsilon_{\mathrm{insu}} d_{LC}}{t_{\mathrm{insu}} \epsilon_{LC}} h_{\mathrm{FSC}}\right)$$

where ϵ_{LC} and d_{LC} are the relative dielectric constant and thickness, respectively, of the liquid crystal layer.

Similar to the derivation leading to (3), the lower bound $(W/L)_{\mathrm{charge,FSC}}$ for FSC LCDs can be derived as

$$\frac{C_{\mathrm{px,FSC}}}{\mu_{\mathrm{eff}} C_g \left(V_s - V_t - V_d\right)} \frac{k_t}{\left(T_{\mathrm{row,FSC}} - T_{\mathrm{delay}}\right)}.$$

As a comparison, the lower bound $(W/L)_{\mathrm{charge,CF}}$ for CF LCDs is

$$\frac{C_{\mathrm{px,CF}}}{\mu_{\mathrm{eff}} C_g \left(V_s - V_t - V_d\right)} \frac{k_t}{\left(T_{\mathrm{row,CF}} - T_{\mathrm{delay}}\right)}.$$

Since $T_{\mathrm{row,FSC}} = 1/3 T_{\mathrm{row,CF}}$ and $C_{LC,\mathrm{FSC}} = 3C_{LC,\mathrm{CF}}$, the two lower bounds are related as

$$\begin{aligned}&\left(\frac{W}{L}\right)_{\mathrm{charge,FSC}} \\ &\quad \simeq 9 \left(\frac{1 + \left(\epsilon_{\mathrm{insu}} d_{LC}/t_{\mathrm{insu}} \epsilon_{LC}\right) h_{\mathrm{FSC}}}{1 + \left(\epsilon_{\mathrm{insu}} d_{LC}/t_{\mathrm{insu}} \epsilon_{LC}\right) h_{\mathrm{CF}}}\right) \left(\frac{W}{L}\right)_{\mathrm{charge,CF}}.\end{aligned}$$

Following the derivation leading to (6), the upper bounds of W/L derived from the holding phase constraint are, respectively

$$\begin{aligned}\left(\frac{W}{L}\right)_{\mathrm{hold,FSC}} &= \frac{C_{\mathrm{px,FSC}}}{T_{\mathrm{frame,FSC}} 2^{N_{\mathrm{bit}}} \sigma_D t_{\mathrm{semi}}} \\ \left(\frac{W}{L}\right)_{\mathrm{hold,CF}} &= \frac{C_{\mathrm{px,CF}}}{T_{\mathrm{frame,CF}} 2^{N_{\mathrm{bit}}} \sigma_D t_{\mathrm{semi}}}.\end{aligned}$$

$$W < \frac{\left[2\left(C_{LC,\mathrm{min}} + C_S\right)\left(C_{LC,\mathrm{max}} + C_S\right) F_{\mathrm{kb}}\right] / \left[\left(v_{s,\mathrm{ON}} - v_{s,\mathrm{OFF}}\right)\left(C_{LC,\mathrm{max}} - C_{LC,\mathrm{min}}\right)\right] - C_{\mathrm{pg}}}{\tilde{C}_{\mathrm{gd}}} \tag{10}$$

They are related by

$$\left(\frac{W}{L}\right)_{\mathrm{hold,FSC}} \simeq 9\left(\frac{1+(\epsilon_{\mathrm{insu}}d_{LC}/t_{\mathrm{insu}}\epsilon_{LC})h_{\mathrm{FSC}}}{1+(\epsilon_{\mathrm{insu}}d_{LC}/t_{\mathrm{insu}}\epsilon_{LC})h_{\mathrm{CF}}}\right)\left(\frac{W}{L}\right)_{\mathrm{hold,CF}}.$$

Similar to the derivation of (10), another upper bound of W based on the asymmetric kickback voltage constraint $W_{\mathrm{kb,FSC}}$ is derived as (*) shown at the bottom of next page for the FSC LCDs, and the counterpart $W_{\mathrm{kb,CF}}$ for the CF LCDs is (**) shown at the bottom of the next page

The kickback voltage is a function of the falling slope of the scan pulse, a steeper slope induces a larger kickback voltage. In this analysis, an infinite slope is assumed to derive the largest possible kickback voltage.

Similar to (11), the scan-line delay $t_{\mathrm{d,scan,FSC}}$ for the voltage to reach 90% of its intended level can be expressed as

$$t_{d,\mathrm{scan,FSC}} = 1.03N^2_{\mathrm{data,FSC}}R_{\mathrm{scan,FSC}}C_{\mathrm{scan,FSC}}.$$

Under the same resolution, screen size, and process condition, and assuming that the R, G and B subpixels on the CF screen are aligned horizontally, the scan-line length passing through an FSC pixel will be three times that passing through a CF subpixel; hence, $N_{\mathrm{data,FSC}} = 1/3N_{\mathrm{data,CF}}$, $R_{\mathrm{scan,FSC}} \simeq 3R_{\mathrm{scan,CF}}$, $C_{\mathrm{scan,FSC}} \simeq 3C_{\mathrm{scan,CF}}$, and $t_{d,\mathrm{scan,FSC}} \simeq t_{d,\mathrm{scan,CF}}$.

The data line delay $t_{d,\mathrm{data,FSC}}$ for the voltage to reach 90% of its intended level can be expressed as

$$t_{d,\mathrm{data,FSC}} = 1.03N^2_{\mathrm{scan,FSC}}R_{\mathrm{data,FSC}}C_{\mathrm{data,FSC}}.$$

Since $N_{\mathrm{scan,FSC}} = N_{\mathrm{scan,CF}}$, we have $R_{\mathrm{data,FSC}} \simeq R_{\mathrm{data,CF}}$, $C_{\mathrm{data,FSC}} \simeq C_{\mathrm{data,CF}}$, and $t_{d,\mathrm{data,FSC}} \simeq t_{d,\mathrm{data,CF}}$.

Since a scan line drives more pixels than does a data line, $t_{d,\mathrm{scan}} > t_{d,\mathrm{data}}$; thus, the delay time T_{delay} during the charging phase is dominated by the scan-line delay; hence, $T_{\mathrm{delay,FSC}} \simeq T_{\mathrm{delay,CF}}$, namely, both FSC LCDs and CF LCDs have similar delay-time budget.

In summary, the major constraint on the FSC pixel design is the short charging time. On the other hand, the FSC pixel design is less restricted in the holding, asymmetric kickback, and delay mechanisms. Since $C_{LC,\mathrm{FSC}} = 3C_{LC,\mathrm{CF}}$ and $C_{\mathrm{px}} \simeq C_{LC} + C_S$, the storage capacitance required in the FSC LCDs can be decreased. Since the storage capacitor and the TFT are opaque, smaller h and W are preferred. A higher aperture ratio can be realized in the FSC LCDs, which requires lower backlight intensity, and hence, lower power consumption.

V. Assessment of Different Screen Sizes

In this section, the performances of a 30 in wide extended graphics array (WXGA) and a 2.4 in quarter video graphics array (QVGA) LSD will be analyzed. The FSC LCDs and the CF LCDs will be compared in terms of operation window, aperture ratio, and power consumption.

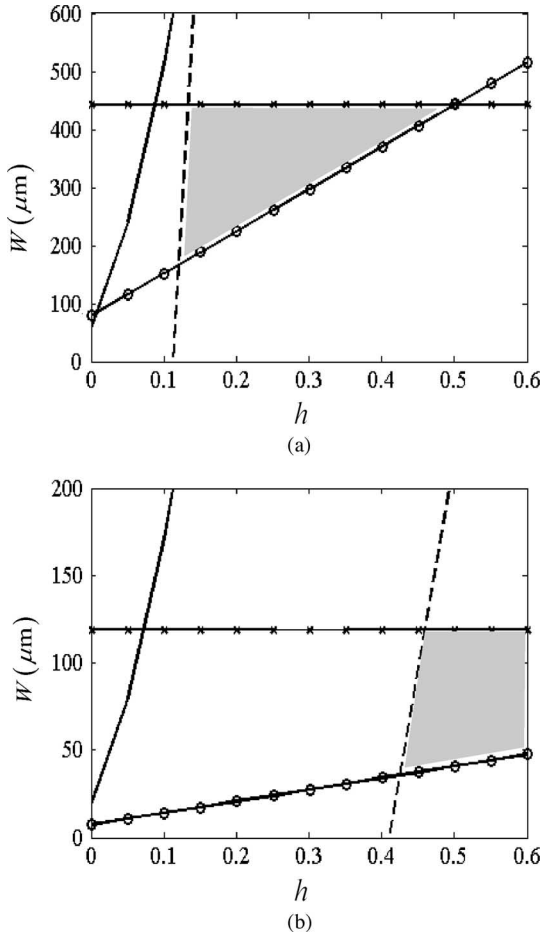

Fig. 2. Operationwindow of 30 in WXGA LCD. (a) FSC LCD. (b) CF LCD. $(-\circ-)$ charging constraint; $(---)$ holding constraint; (—) asymmetric kickback constraint; $(-*-)$ scan-line delay constraint; cell gap is $d_{LC} = 4.7$ μm, line widths are $W_{\mathrm{scan}} = 20\mu$m and $W_{\mathrm{data}} = 10$ μm, sheet resistance is 16.8 nΩm, dielectric constant and thickness of insulator are $\epsilon_{\mathrm{insu}} = 6.9$ and $t_{\mathrm{insu}} = 300$ nm, parameters of TFT are $\mu_{\mathrm{eff}} = 0.15 \times 10^{-4}$ m^2/V $\cdot$ s and $V_t = 0.7$ V.

A. Operation Window

Fig. 2 shows the operation windows of 30 in WXGA LCDs based on the design constraints, where W is the TFT channel width and $h = A_{C_S}/A_{\mathrm{pixel}}$ is the ratio between the size of the storage capacitor and that of the pixel. The operation window of the FSC LCD has relatively low h and high W compared with that of the CF LCD, with $h_{30\,\mathrm{in,FSC}} > 0.121$ and $h_{30\,\mathrm{in,CF}} > 0.423$.

If the minimum channel widths, $W_{30\,\mathrm{in,FSC}} = 157$ μm at $h_{30\,\mathrm{in,FSC}} = 0.121$ and $W_{30\,\mathrm{in,CF}} = 34$ μm at $h_{30\,\mathrm{in,CF}} = 0.423$, respectively, are chosen, the maximum aperture ratios (ARs) will be $\mathrm{AR}_{30\,\mathrm{in,FSC}} = 79\%$ and $\mathrm{AR}_{30\,\mathrm{in,CF}} = 45\%$. The available AR at different channel widths and area ratios are marked in Fig. 3. The maximm AR of the FSC LCDs is about twice that of the CF LCDs.

The performance parameters of two different LCD screen sizes are summarized in Table I. The lower bound of W is determined by the charging phase constraint for both screen sizes, but the dominant factors for the upper bound of W are different.

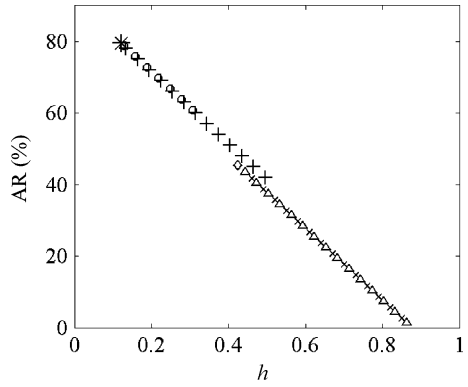

Fig. 3. AR of 30 in WXGA LCD. (*) $W_{30\,\mathrm{in,FSC}} = 157\mu$m; ($\circ$) $W_{30\,\mathrm{in,FSC}} = 284\ \mu$m; (+) $W_{30\,\mathrm{in,FSC}} = 411\ \mu$m; ($\diamondsuit$) $W_{30\,\mathrm{in,CF}} = 34\ \mu$m; ($\triangle$) $W_{30\,\mathrm{in,CF}} = 70\ \mu$m; ($\times$) $W_{30\,\mathrm{in,CF}} = 108\ \mu$m.

TABLE I
GENERAL PERFORMACES OF 30 IN AND 2.4 IN LCD PIXEL (*AR=0)

parameter	30" HDTV	2.4" portable
resolution	WXGA (1,366×768)	QVGA (320×240)
aspect ratio	16:9	4:3
T_{delay}	1.7 μs	17 ns
$A_{\mathrm{px,FSC}}(\mu\mathrm{m}^2)$	236,500	23,226
$A_{\mathrm{subpx,CF}}(\mu\mathrm{m}^2)$	78,833	7,742
h_{FSC}	(0.120, 0.496)	(0.116, 0.941*)
h_{CF}	(0.430, 0.876*)	(0.416, 0.903*)
$W_{\mathrm{FSC}}(\mu\mathrm{m})$	(157, 284)	(3.59, 223.8)
$W_{\mathrm{CF}}(\mu\mathrm{m})$	(34, 70)	((0.93, 73.33)
$\mathrm{AR}_{\mathrm{FSC}}(\%)$	(42, 79)	(0, 82)
$\mathrm{AR}_{\mathrm{CF}}(\%)$	(0, 45)	(0, 48)
$\frac{\mathrm{AR}_{\mathrm{FSC,max}}}{\mathrm{AR}_{\mathrm{CF,max}}}$	1.76	1.7

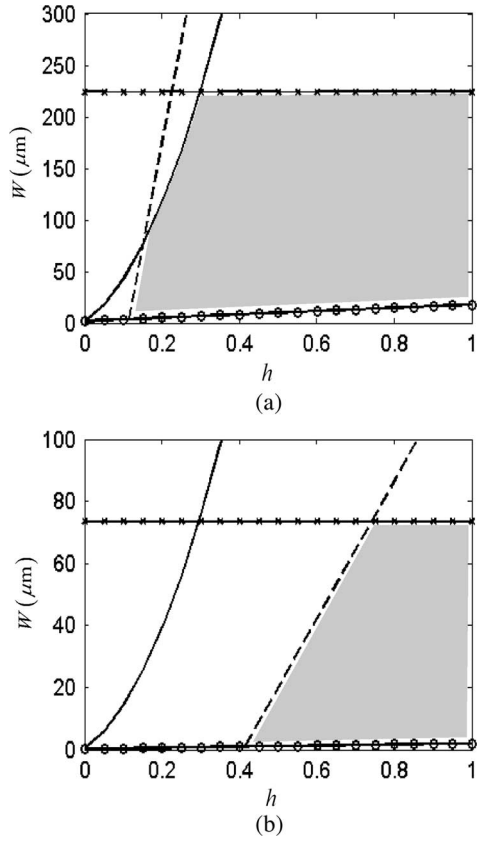

Fig. 4. Operation window of 2.4 in QVGA LCD. (a) FSC LCD. (b) CF LCD. ($-\circ-$) charging constraint; ($---$) holding constraint; (—) asymmetric kickback constraint; ($-*-$) scan-line delay constraint; parameters are the same as in Fig. 3, except $W_{\mathrm{scan}} = W_{\mathrm{data}} = W_{\mathrm{ground}} = 3\ \mu$m.

For the large-size LCDs, the upper bound of W is determined by the holding phase and the scan-line delay constraints. For the small-size LCDs, the asymmetric kickback constraint affects the operation window and cannot be neglected, as shown in Fig. 4.

For 2.4 in QVGA LCDs, the minimum TFT channel widths of the FSC LCD and the CF LCD are 3.59 and 0.93 μm, respectively. At a given h, larger L implies larger W based on the holding and charging constraints, and the intercept point of the charging and holding bounds will be moved toward smaller h and larger W. In this case, the asymmetric kickback constraint, instead of the holding constraint, will dominate the upper bound of the operation window in the FSC LCDs.

Note that the scan driver can be used to drive the scan line at both ends simultaneously, and the longest delay will occur at the center of the scan line. When using this double-driver technique, T_{delay} can be reduced to about one quarter that of using conventional single driver.

The pixel area A_{pixel} is proportional to C_{px}. In the charging phase, larger current is required to charge a larger C_{px}, and the charging current of TFT is determined by the channel width W. Thus, there is a positive correlation between the channel width W and the pixel area A_{pixel}.

The capacitive load on a scan line can be reexpressed as

$$C_{\mathrm{scan}} = \left(2\tilde{C}_{\mathrm{gd}} + \epsilon_{\mathrm{insu}}\epsilon_0 \frac{L}{t_{\mathrm{insu}}}\right) W + 2\epsilon_{\mathrm{insu}}\epsilon_0 \frac{t_{\mathrm{insu}} L_{\mathrm{scan}}}{s_{\mathrm{pg}}} + \epsilon_0 \left(\epsilon_{LC} \frac{L_{\mathrm{scan}}}{d_{LC}} + \epsilon_{\mathrm{insu}} \frac{W_{\mathrm{data}}}{t_{\mathrm{insu}}}\right) W_{\mathrm{scan}}.$$

$$\frac{\left[2\left(C_{LC,\mathrm{min,FSC}} + C_{S,\mathrm{FSC}}\right)\left(C_{LC,\mathrm{max,FSC}} + C_{S,\mathrm{FSC}}\right) F_{\mathrm{kb}}/(v_{s,\mathrm{ON}} - v_{s,\mathrm{OFF}})\left(C_{LC,\mathrm{max,FSC}} - C_{LC,\mathrm{min,FSC}}\right)\right] - C_{\mathrm{pg}}}{\tilde{C}_{\mathrm{gd}}} \quad (*)$$

$$\frac{\left[2\left(C_{LC,\mathrm{min,CF}} + C_{S,\mathrm{CF}}\right)\left(C_{LC,\mathrm{max,CF}} + C_{S,\mathrm{CF}}\right) F_{\mathrm{kb}}/(v_{s,\mathrm{ON}} - v_{s,\mathrm{OFF}})\left(C_{LC,\mathrm{max,CF}} - C_{LC,\mathrm{min,CF}}\right)\right] - C_{\mathrm{pg}}}{\tilde{C}_{\mathrm{gd}}} \quad (**)$$

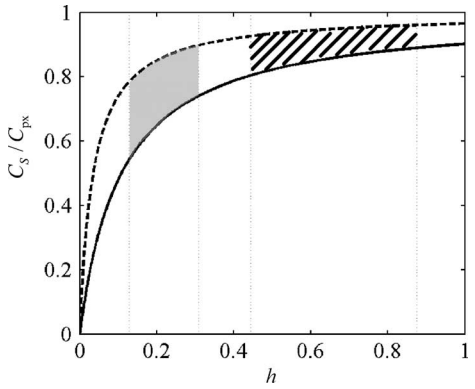

Fig. 5. Relation between capacitance ratio and area ratio, gray area for FSC with $W = 284\ \mu$m, slit area for CF with $W = 70\ \mu$m, $(--)\ \epsilon_{LC} = 3.8$; $(—)$ $\epsilon_{LC} = 11.7$; parameters are the same as in Fig.3.

Thus, the delay time $T_{\rm delay}$ can be rephrased as

$$1.03N_{\rm data}^2\rho_{\rm scan}\frac{L_{\rm scan}}{t_{\rm scan}}\left(\frac{B}{W_{\rm scan}}+D\right)$$

where

$$B=\left(2\tilde{C}_{\rm gd}+\epsilon_0\epsilon_{\rm insu}\frac{L}{t_{\rm insu}}\right)W+\epsilon_0\epsilon_{\rm insu}\frac{t_{\rm insu}L_{\rm scan}}{s_{\rm pg}}$$

$$D=\epsilon_0\left(\epsilon_{LC}\frac{L_{\rm scan}}{d_{LC}}+\epsilon_{\rm insu}\frac{W_{\rm data}}{t_{\rm insu}}\right).$$

For 30 in LCDs, signal delays cannot be neglected, and wider scan lines are needed to reduce the delay along the scan lines. For example, if choosing $W_{\rm scan,30\,in} = 20\ \mu$m and $W_{\rm scan,2.4\,in} = 3\ \mu$m, the delay times will be 1.7 μs and 17 ns, respectively.

B. Aperture Ratio

The AR is defined as

$$\mathrm{AR}=\frac{A_{\rm pixel}-A_{\rm opaque}}{A_{\rm pixel}}$$

where $A_{\rm opaque}$ is the opaque area in a pixel. As shown in Fig. 1, $A_{\rm opaque}$ is decomposed as

$$A_{\rm opaque}=A_{\rm data}+A_{\rm scan}+A_{\rm ground}+A_{\rm TFT}+A_{C_S}-A_{\rm cross}$$

where $A_{\rm data}=L_{\rm data}\times W_{\rm data}$, $A_{\rm scan}=L_{\rm scan}\times W_{\rm scan}$, and $A_{\rm ground}=L_{\rm scan}\times W_{\rm ground}$ are the areas of data line, scan line, and ground line, respectively, in the (m,n)th pixel, $A_{\rm TFT}=W\times L$ is the area of the TFT, $A_{C_S}=hA_{\rm pixel}$ is the area of the storage capacitor, and $A_{\rm cross}=W_{\rm data}\times(W_{\rm scan}+W_{\rm ground})$ is the overlapping area between a scan line and a data line. The relation between $C_S/C_{\rm px}$ and h is

$$\frac{C_S}{C_{\rm px}}\simeq\frac{C_S}{C_S+C_{LC}}=\frac{hd_{LC}}{hd_{LC}+t_{\rm insu}\epsilon_{LC}/\epsilon_{\rm insu}}.$$

Fig. 5 shows the capacitance ratio $C_S/C_{\rm px}$ as a function of h, with $d_{LC}=4.67\ \mu$m, $t_{\rm insu}=0.3\ \mu$m, $\epsilon_{\rm insu}=6.9$, and $3.8\le\epsilon_{LC}\le 11.7$. Take $W_{\rm FSC}=284\ \mu$m, $0.128<h_{\rm FSC}<0.309$ and $W_{\rm CF}=70\ \mu$m, $0.443<h_{\rm CF}<0.876$, respectively, as deduced from the operation windows shown in Fig. 2. Note that $0.55\le C_S/C_{\rm px}\le 0.9$ for the FSC LCDs and $0.80\le C_S/C_{\rm px}\le 0.96$ for the CF LCDs. Smaller $C_S/C_{\rm px}$ ratio implies that smaller storage capacitance is needed to satisfy the holding constraint. Because the storage capacitor is opaque, larger $C_S/C_{\rm px}$ ratio implies smaller AR. Note that $\mathrm{AR}_{\rm FSC}>\mathrm{AR}_{\rm CF}$, and the ratio $\mathrm{AR}_{\rm FSC,max}/\mathrm{AR}_{\rm CF,max}$ is about 1.7.

The backlight consumes the most power in the LCDs. Higher AR implies higher backlight efficiency or less power consumption. In the FSC LCDs, the backlight efficiency is three times that of the CF LCDs since no color filters are used. If $\mathrm{AR}_{\rm FSC,max}/\mathrm{AR}_{\rm CF,max}$ is about 2, then the total backlight power consumption of the FSC LCDs will be only one-sixth that of the CF LCDs. For example, if the 30 in CF LCDs require 130 W of backlight, then the 30 in FSC LCDs will require only 24 W to provide the same luminance. Similarly, for 2.4 in LCDs, if the CF LCDs require 500 mW of backlight, the FSC ones will require only 90 mW.

C. Power Consumption

The power consumption of the data driver can be estimated as [11]

$$P=V_{\rm DD}\frac{N_{\rm scan}C_{\rm data}\Delta V_{d,\max}}{2T_{\rm row}}N_{\rm data}$$

where $V_{\rm DD}$ is the power supply voltage and $\Delta V_{d,\max}$ is the maximum voltage swing on the data lines. Thus, the power consumption ratio between the FSC LCDs and the CF LCDs is close to 1.

VI. Conclusion

Design constraints on the FSC LCDs have been derived and demonstrated with two different screen sizes. The FSC pixel design is less constrained in the holding, asymmetric kickback, and delay mechanisms, but is more strictly constrained in the charging phase. Higher AR and less power consumption can be achieved for the FSC LCDs due to the smaller storage capacitance needed. The line width and channel width are critical in large-size LCDs, especially in the FSC LCDs. Although the frame rate of the FSC LCDs is three times that of the CF LCDs, the power consumption in pixel-related circuitries of the FSC LCDs is close to that of the CF LCDs.

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