# Curriculum Vitae

## Jie-Hong Roland Jiang

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**Research interests**

Formal verification, logic synthesis, computation models

**Education**

| | |
|---|---|
| December 2004 | Ph.D., EECS, University of California, Berkeley, USA |
| June 1998 | M.S., Electronics Engineering, National Chiao Tung University, Taiwan |
| June 1996 | B.S., Electronics Engineering, National Chiao Tung University, Taiwan |

**Experience**

| | |
|---|---|
| August 2013 – present | Professor<br>Department of Electrical Engineering<br>Graduate Institute of Electronics Engineering<br>National Taiwan University |
| August 2017 – present | Division Director<br>Information Management Division<br>Computer and Information Network Center<br>National Taiwan University |
| November 2013 – July 2016 | Deputy Director<br>Graduate Institute of Electronics Engineering<br>National Taiwan University |
| August 2009 – July 2013 | Associate Professor<br>Department of Electrical Engineering<br>Graduate Institute of Electronics Engineering<br>National Taiwan University |
| August 2005 – July 2009 | Assistant Professor<br>Department of Electrical Engineering<br>Graduate Institute of Electronics Engineering<br>National Taiwan University |
| January 2005 – August 2005 | Postdoctoral Researcher<br>Department of Electrical Engineering and Computer Sciences<br>University of California, Berkeley<br>(research on formal verification, hardware synthesis,<br>quantum computation) |

**Experience (cont'd)**

| | |
|---|---|
| June 2001 – December 2004 | Research Assistant<br>Department of Electrical Engineering and Computer Sciences<br>University of California, Berkeley<br>(research and development of verification and synthesis<br>techniques for electronic design automation) |
| August 2004 – December 2004 | Teaching Assistant<br>Department of Electrical Engineering and Computer Sciences<br>University of California, Berkeley<br>(EE42 Introduction to Digital Electronics) |
| June 2003 – September 2003 | Graduate Intern<br>Verplex Systems, Inc./Cadence Design Systems, Inc.<br>(research and development of sequential equivalence checking<br>algorithms) |
| January 2003 – May 2003 | Teaching Assistant<br>Department of Electrical Engineering and Computer Sciences<br>University of California, Berkeley<br>(EE219B Logic Synthesis) |
| June 2000 – August 2000 | Research Assistant<br>Department of Electrical Engineering and Computer Sciences<br>University of California, Berkeley<br>(MVSIS project) |
| July 1998 – April 2000 | Second Lieutenant<br>Air Force, Taiwan, R.O.C.<br>(compulsory military service) |

**Honors and awards**

| | |
|---|---|
| 2017 | Humboldt Research Fellowship, Alexander von Humboldt Foundation |
| 2013, 2014, 2016 | Teaching Excellence Award, National Taiwan University |
| 2012 | Distinguished Young Scholar Award, Taiwan IC Design Society |
| 2011, 2013 | Academic Excellence Award, College of EECS, National Taiwan University |
| 2000 – 2001 | UC Regent's Fellowship |
| 1998 | Dragon Thesis Award<br>(Acer Foundation) |
| 1998 | Member of Phi Tau Phi |
| 1997 – 1998 | Fellowship of the Ministry of Education, Taiwan |
| 1997 | Memorial Scholarship of Dr. Sun Yat-Sen's Centennial |
| 1996 | Gold Prize, NCTU Undergraduate Research and Development Award |
| 1995 – 1996 | Academic Achievement Award<br>(Department of Electronics Engineering, National Chiao Tung University) |

**Professional societies**

Association of Computing Machinery (ACM)
Institute of Electrical and Electronics Engineers (IEEE)

**Professional activities**

Steering Committee Member of
     International Workshop on Logic & Synthesis (IWLS) 2017 - present

Technical Program Committee Chair of
>International Workshop on Logic & Synthesis (IWLS) 2018

General Chair of
>International Workshop on Logic & Synthesis (IWLS) 2017

Special Session Chair of
>International Workshop on Logic & Synthesis (IWLS) 2016

Session Chair of
>ACM/IEEE Design Automation Conference 2009, IEEE/ACM International Conference on Computer-Aided Design 2013-2014

Invited Lecturer of
>TAROT Summer School on Software Testing, Verification and Validation 2011, Formosan Summer School on Logic, Language, and Computation (FLOLAC) 2009, 2011, 2013, 2015, 2017

Local Arrangement Chair of
>International Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI) 2015

Technical Program Committee Member of
>Asian Symposium on Programming Languages and Systems (APLAS) 2013, Asia and South Pacific Design Automation Conference (ASPDAC) 2012, 2018, International Symposium on Automated Technology for Verification and Analysis (ATVA) 2011-2012, 2014-2015, 2017, International Workshop on Constraints in Formal Verification (CFV) 2013, 2015, International Conference on Formal Methods in Computer Aided Design (FMCAD) 2010, International Symposium on Games, Automata, Logics, and Formal Verification (GandALF) 2018, International Conference on Computer-Aided Design (ICCAD) 2012-2014, International Conference on Testing Software and Systems (ICTSS) 2017, 2018, International Joint Conference on Artificial Intelligence (IJCAI) 2018, International Workshop on Logic and Synthesis (IWLS) 2010-2018, International Workshop on Quantified Boolean Formula (QBF) 2016, International Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI) 2012-2013, International Conference on Theory and Applications of Satisfiability Testing (SAT) 2015, 2013-2015, IEEE International Symposium on Theoretical Aspects of Software Engineering (TASE) 2010, IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC) 2011

Referee of
>ACM Transactions on Design Automation of Electronic Systems, Asia and South Pacific Design Automation Conference, Asian Symposium on Programming Languages and Systems, Design Automation Conference, Design Automation and Test in Europe, Discrete Applied Mathematics, EURASIP Journal on Embedded Systems, Formal Methods in Computer Aided Design, Formal Methods in System Design, IEEE Design & Test Magazine, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on Computers, IEEE Transactions on VLSI Systems, Integration, the VLSI Journal, International Conference on Computer-Aided Design, International Conference on Computer Design, International Conference on Computer Aided Verification, International Conference on Embedded Software and Systems, International Conference on Very Large Scale Integration, International SOC Conference, International Symposium on Automated Technology for Verification and Analysis, International Symposium on Circuits and Systems, International Workshop on Constraints in Formal Verification, International Workshop on Logic & Synthesis, Journal of

Automated Reasoning, Journal of Computer and System Sciences, Microprocessors and Microsystems, Proceedings of the IEEE, Software Quality Journal, Symmetry

## Publications

Nian-Ze Lee, Jie-Hong R. Jiang. Towards Formal Evaluation and Verification of Probabilistic Design. *IEEE Transactions on Computers*, 67(8): 1202-1216, 2018.

Nian-Ze Lee, Yen-Shi Wang, Jie-Hong R. Jiang. Solving Exist-Random Quantied Stochastic Boolean Satisability via Clause Selection. In *Proc. International Joint Conference on Artificial Intelligence* (IJCAI), 2018.

Ai Quoc Dao, Nian-Ze Lee, Li-Cheng Chen, Mark Po-Hung Lin, Jie-Hong R. Jiang, Alan Mishchenko, Robert K. Brayton. Efficient computation of ECO patch functions. In *Proc. Design Automation Conference* (DAC), 2018.

He-Teng Zhang, Jie-Hong R. Jiang. Cost-aware patch generation for multi-target function rectification of engineering change orders. In *Proc. Design Automation Conference* (DAC), 2018.

Run-Yi Wang, Chia-Cheng Pai, Jun-Jie Wang, Hsiang-Ting Wen, Yu-Cheng Pai, Yao-Wen Chang, James Chien-Mo Li, Jie-Hong R. Jiang. Efficient multi-layer obstacle-avoiding region-to-region rectilinear Steiner tree construction. In *Proc. Design Automation Conference* (DAC), 2018.

Chun-Han Lin, Fang Yu, Jie-Hong Roland Jiang, Tevfik Bultan. Static detection of API call vulnerabilities in iOS executables. In *Proc. International Conference on Software Engineering* (ICSE), 2018.

Nian-Ze Lee, Victor Kravets, Jie-Hong R. Jiang. Sequential Engineering Change Order under Retiming and Resynthesis. In *Proc. International Conference on Computer-Aided Design* (ICCAD), 2017.

Chun-Ning Lai, Jie-Hong Jiang, Francois Fages. RecombinaseBased Genetic Circuit Optimization. In *Proc. IEEE Biomedical Circuits and Systems Conference* (BioCAS), 2017.

Hung-En Wang, Kuan-Hua Tu, Jie-Hong R. Jiang, Natalia Kushik. Homing Sequence Derivation with Quantified Boolean Satisfiability. In *Proc. IFIP International Conference on Testing of Software and Systems* (ICTSS), 2017.

Tai-Yin Chiu, Jie-Hong R. Jiang. Logic Synthesis of RecombinaseBased Genetic Circuits. *Scientific Reports*, 7, Article No. 12873, doi:10.1038/s41598-017-07386-3, 2017.

Hsiao-Lei Chien, Mei-Yen Chiu, Jie-Hong R. Jiang. A Gridless Approach to the Satisfiability of Self-Aligned Triple Patterning. *IEEE Trans. on CAD of Integrated Circuits and Systems*, 36(8): 1251-1264, 2017.

Nian-Ze Lee, Yen-Shi Wang, Jie-Hong R. Jiang. Solving Stochastic Boolean Satisfiability under Random-Exist Quantification. In *Proc. International Joint Conferences on Artificial Intelligence* (IJCAI), 2017.

Chun-Ning Lai and Jie-Hong R. Jiang. Path-Specific Functional Timing Verification under Floating and Transition Modes of Operation. In *Proc. ACM/IEEE Design Automation Conf.* (DAC), pp. 38:1-38:6, 2017.

Cheng-Yu Shih, Chun-Hong Shih, and Jie-Hong R. Jiang. Closing the Accuracy Gap of Static Performance Analysis of Asynchronous Circuits. In *Proc. ACM/IEEE Design Automation Conf.* (DAC), pp. 73:1-73:6, 2017.

Nian-Ze Lee, Yen-Shi Wang, and Jie-Hong R. Jiang. Solving Stochastic Boolean Satisfiability under Random-Exist Quantification. In *Proc. Int'l Joint Conf. on Artificial Intelligence* (IJCAI), 2017.

Hui-Ju Katherine Chiang, Chi-Yuan Liu, Jie-Hong R. Jiang, and Yao-Wen Chang. Simultaneous EUV Flare Variation Minimization and CMP Control by Coupling-Aware Dummification. *IEEE Trans. on CAD of Integrated Circuits and Systems*, 35(4): 598-610, 2016.

Valeriy Balabanov, Shuo-Ren Lin, and Jie-Hong R. Jiang. Flexibility and Optimization of QBF Skolem-Herbrand Certificates. *IEEE Trans. on CAD of Integrated Circuits and Systems*, 35(9): 1557-1568, 2016.

Yi-Hsiang Lai, Chi-Chuan Chuang, and Jie-Hong R. Jiang. Scalable Synthesis of PCHB-WCHB Hybrid Quasi-Delay Insensitive Circuits. *IEEE Trans. on CAD of Integrated Circuits and Systems*, 35(11): 1797-1810, 2016.

Nian-Ze Lee, Hao-Yuan Kuo, Yi-Hsiang Lai, and Jie-Hong R. Jiang. Analytic Approaches to the Collapse Operation and Equivalence Verification of Threshold Logic Circuits. In *Proc. IEEE/ACM Int'l Conf. on Computer-Aided Design* (ICCAD), 2016.

Tai-Yin Chiu, Cheng-Han Hsieh and Jie-Hong R. Jiang. Realization of Large Logic Circuits with Long-Term Memory Using CRISPR/Cas9 Systems. In *Proc. Int'l Workshop on Bio-Design Automation* (IWBDA), Newcastle upon Tyne, UK, Aug. 2016.

Hung-En Wang, Tzung-Lin Tsai, Chun-Han Lin, Fang Yu, and Jie-Hong R. Jiang. String Analysis via Automata Manipulation with Logic Circuit Representation. In *Proc. Int'l Conf. on Computer Aided Verification* (CAV), (1): 241-260, 2016.

Valeriy Balabanov, Jie-Hong Roland Jiang, Christoph Scholl, Alan Mishchenko, and Robert K. Brayton. 2QBF: Challenges and Solutions. In *Proc. Int'l Conf. on Theory and Applications of Satisfiability Testing* (SAT), pp. 453-469, 2016.

Grace Wu, Yi-Tin Sun, and Jie-Hong R. Jiang. Design Partitioning for Large-Scale Equivalence Checking and Functional Correction. In *Proc. ACM/IEEE Design Automation Conf.* (DAC), pp. 23:1-23:6, 2016.

Valeriy Balabanov, Jie-Hong Roland Jiang, Alan Mishchenko, and Christoph Scholl. Clauses Versus Gates in CEGAR-Based 2QBF Solving. In *Proc. AAAI Workshop: Beyond NP*, 2016

Nina Yevtushenko, Khaled El-Fakih, Tiziano Villa, and Jie-Hong R. Jiang. Deriving Compositionally Deadlock-free Componenets over Synchronous Automata Compositions. *The Computer Journal*, Oxford University Press, 58(11):2793-2803, 2015.

Yi-Hsiang Lai, Chi-Chuan Chuang, and Jie-Hong R. Jiang. A General Framework for Efficient Performance Analysis of Acyclic Asynchronous Pipelines. In *Proc. IEEE/ACM Int'l Conf. on Computer-Aided Design* (ICCAD), Nov. 2015.

Chun-Hong Shih, Yi-Hsiang Lai and Jie-Hong R. Jiang. SPOCK: Static Performance analysis and deadlOCK verification for efficient asynchronous circuit synthesis. In *Proc. IEEE/ACM Int'l Conf. on Computer-Aided Design* (ICCAD), Nov. 2015.

Bo-Yuan Huang, Yi-Hsiang Lai, and Jie-Hong R. Jiang. Asynchronous QDI Circuit Synthesis from Signal Transition Protocols. In *Proc. IEEE/ACM Int'l Conf. on Computer-Aided Design* (ICCAD), Nov. 2015.

Ting-Wei Chiang and Jie-Hong R. Jiang. Property-Directed Synthesis of Reactive Systems from Safety Specifications. In *Proc. IEEE/ACM Int'l Conf. on Computer-Aided Design* (ICCAD), Nov. 2015.

Kuan-Hua Tu, Tzu-Chen Hsu, and Jie-Hong R. Jiang. QELL: QBF Reasoning with Extended Clause Learning and Levelized SAT Solving. In *Proc. Int'l Conf. on Theory and Applications of Satisfiability Testing* (SAT), Sep. 2015.

Hui-Ju Katherine Chiang, Jie-Hong R. Jiang, and Francois Fages. Reconfigurable Neuromorphic Computation in Biochemical Systems. In *Proc. 37th Int'l Conf. of the IEEE Engineering in Medicine and Biology Society* (EMBC), Aug. 2015.

Ting-Wei Chiang, Kai-Hui Chang, Yen-Ting Liu, Jie-Hong R. Jiang. Scalable Sequence-Constrained Retention Register Minimization in Power Gating Design. In *Proc. ACM/IEEE Design Automation Conf.* (DAC), June 2015.

Hui-Ju Katherine Chiang, Francois Fages, Jie-Hong Roland Jiang, and Sylvain Soliman. Hybrid Simulations of Heterogeneous Biochemical Models in SBML. *ACM Trans. Model. Comput. Simul.* 25(2):14, 2015.

Valeriy Balabanov, Jie-Hong R. Jiang, Mikolas Janota, and Magdalena Widl. Efficient Extraction of QBF (Counter)models from Long-Distance Resolution Proofs. In *Proc. AAAI Conf. on Artificial Intelligence* (AAAI), Jan. 2015.

Nian-Ze Lee and Jie-Hong R. Jiang. Towards Formal Evaluation and Verification of Probabilistic Design. In *Proc. IEEE/ACM Int'l Conf. on Computer-Aided Design* (ICCAD), Nov. 2014.

Hui-Ju Katherine Chiang, Jie-Hong R. Jiang, and Francois Fages. Building Recofigurable Circuitry in a Biochemical World. In *Proc. IEEE Biomedical Circuits and Systems Conf.* (BioCAS), Oct. 2014.

Valeriy Balabanov, Magdalena Widl, and Jie-Hong R. Jiang. QBF Resolution Systems and their Proof Complexities. In *Proc. Int'l Conf. on Theory and Applications of Satisfiability Testing* (SAT), Vienna, Austria, Jul. 2014.

Chi-Chuan Chuang, Yi-Hsiang Lai, and Jie-Hong R. Jiang. Synthesis of PCHB-WCHB Hybrid Quasi-Delay Insensitive Circuits. In *Proc. ACM/IEEE Design Automation Conf.* (DAC), San Francisco, USA, Jun. 2014.

Chi-Yuan Liu, Hui-Ju K. Chiang, Yao-Wen Chang, and Jie-Hong R. Jiang. Simultaneous EUV Flare Variation Minimization and CMP Control with Coupling-Aware Dummification. In *Proc. ACM/IEEE Design Automation Conf.* (DAC), San Francisco, USA, Jun. 2014.

Tai-Yin Chiu, Ruei-Yang Huang, Hui-Ju K. Chiang, Jie-Hong R. Jiang, and Francois Fages. Configurable Linear Control of Biochemical Systems. In *Proc. Int'l Workshop on Bio-Design Automation* (IWBDA), Boston, MA, Jun. 2014.

Yi-Hsiang Lai, Chi-Chuan Chuang, and Jie-Hong R. Jiang. Efficient Static Performance Analysis of Acyclic Asynchronous Pipelines. In *Proc. Int'l Workshop on Logic & Synthesis* (IWLS), San Francisco, USA, Jun. 2014.

Valeriy Balabanov, Hui-Ju Katherine Chiang, and Jie-Hong R. Jiang. Henkin Quantifiers and Boolean Formulae: A Certification Perspective of DQBF. *Theoretical Computer Science* (TCS), 523: 86-100, Feb. 2014.

Tsung-Po Liu, Shuo-Ren Lin, Jie-Hong R. Jiang. Software Workarounds for Hardware Errors: Instruction Patch Synthesis. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (TCAD), 32(12): 1992-2003, Dec. 2013.

Ko-Lung Yuan, Chien-Yen Kuo, Jie-Hong R. Jiang, Meng-Yen Li. Encoding Multi-Valued Functions for Symmetry. In *Proc. IEEE/ACM Int'l Conf. on Computer-Aided Design* (ICCAD), San Jose, USA, Nov. 2013.

Shin-Yann Ho, Shuo-Ren Lin, Ko-Lung Yuan, Chien-Yen Kuo, Kuan-Yu Liao, Jie-Hong R. Jiang, Chien-Mo Li. Automatic Test Pattern Generation for Delay Defects Using Timed Characteristic Functions. In *Proc. IEEE/ACM Int'l Conf. on Computer-Aided Design* (ICCAD), San Jose, USA, Nov. 2013.

Hui-Ju K. Chiang, Francois Fages, Jie-Hong R. Jiang, and Sylvain Soliman. On the Hybrid Composition and Simulation of Heterogeneous Biochemical Models. In *Proc. Int'l Conf. on Computational Methods in Systems Biology* (CMSB), Klosterneuburg, Austria, Sep. 2013.

Yi-Ting Chung and Jie-Hong R. Jiang. Functional Timing Analysis Made Fast and General. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (TCAD), 32(9): 1421-1434, Sep. 2013

Ruei-Yang Huang, De-An Huang, Hui-Ju K. Chiang, Jie-Hong R. Jiang, and Francois Fages. Species Minimization in Computation with Biochemical Reactions. In *Proc. Int'l Workshop on Bio-Design Automation* (IWBDA), London, UK, Jul. 2013.

Kuan-Hua Tu and Jie-Hong R. Jiang. Synthesis of Feedback Decoders for Initialized Encoders. In *Proc. ACM/IEEE Design Automation Conf.* (DAC), Austin, TX, Jun. 2013.

De-An Huang, Jie-Hong R. Jiang, Ruei-Yang Huang, and Chi-Yun Cheng. Compiling Program Control Flows into Biochemical Reactions. In *Proc. IEEE/ACM Int'l Conf. on Computer-Aided Design* (ICCAD), San Jose, USA, Nov. 2012.

Kuan-Hsien Ho, Jie-Hong R. Jiang, and Yao-Wen Chang. TRECO: Dynamic Technology Remapping for Timing Engineering Change Orders. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (TCAD), 31(11): 1723-1733, Nov. 2012.

Hsiou-Yuan Liu, Yen-Cheng Chou, Chen-Hsuan Lin, and Jie-Hong R. Jiang. Automatic Decoder Synthesis: Methods and Case Studies. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (TCAD), 31(9): 1319-1331, Sep. 2012.

Kai-Hui Chang, Chia-Wei Chang, Jie-Hong R. Jiang, and Chien-Nan J. Liu. Reducing Test Point Overhead with Don't-Cares. In *Proc. IEEE Int'l Midwest Symposium on Circuits and Systems* (MWSCAS), Boise, ID, Aug. 2012.

Valeriy Balabanov and Jie-Hong R. Jiang. Unified QBF Certification and its Applications. *Formal Methods in System Design* (FMSD), 41(1): 45-65, Aug. 2012.

Cheng-Shen Han and Jie-Hong R. Jiang. When Boolean Satisfiability Meets Gaussian Elimination in a Simplex Way. In *Proc. Int'l Conf. on Computer Aided Verification* (CAV), Berkeley, USA, Jul. 2012.

Kai-Hui Chang, Chia-Wei Chang, Jie-Hong R. Jiang, and Chien-Nan J. Liu. Improving Design Verifiability by Early RTL Coverability Analysis. In *Proc. ACM/IEEE Int'l Conf. on Formal Methods and Models for Codesign* (MEMOCODE), Arlington, VA, Jul. 2012.

Valeriy Balabanov, Hui-Ju K. Chiang, and Jie-Hong R. Jiang. Henkin Quantifiers and Boolean Formulae. In *Proc. Int'l Conf. on Theory and Applications of Satisfiability Testing* (SAT), Trento, Italy, Jun. 2012.

Yi-Ting Chung and Jie-Hong R. Jiang. Functional Timing Analysis Made Fast and General. In *Proc. ACM/IEEE Design Automation Conf.* (DAC), San Francisco, USA, Jun. 2012.

K.-H. Ho, X.-W. Shih, and J.-H. R. Jiang. Clock Rescheduling for Timing Engineering Change Orders. In *Proc. Asia and South Pacific Design Automation Conf.* (ASP-DAC), Sydney, Australia, January 2012.

A. Mishchenko, R. K. Brayton, J.-H. R. Jiang, and S. Jang. Scalable don't-care-based logic optimization and resynthesis. *ACM Trans. on Reconfigurable Technology and Systems* (TRETS), 4(4):34, 2011.

H.-Y. Liu, Y.-C. Chou, C.-H. Lin, and J.-H. R. Jiang. Towards Completely Automatic Decoder Synthesis. In *Proc. IEEE/ACM Int'l Conf. on Computer Aided Design* (ICCAD), San Jose, USA, November 2011.

V. Balabanov and J.-H. R. Jiang. Resolution Proofs and Skolem Functions in QBF Evaluation and Applications. In *Proc. Int'l Conf. on Computer Aided Verification* (CAV), Salt Lake City, USA, July 2011.

C.-W. Chang, H.-Z. Chou, K.-H. Chang, J.-H. R. Jiang, C.-N. Liu, and S.-Y. Kuo. Constraint Generation for Software-Based Post-Silicon Bug Repair with Scalable Resynthesis Technique for Constraint Optimization. In *Proc. IEEE Int'l Symp. on Quality Electronic Design* (ISQED), Santa Clara, USA, March 2011.

H.-P. Lin, J.-H. R. Jiang, and R.-R. Lee. "Ashenhurst Decomposition Using SAT and Interpolation. In *Advanced Techniques in Logic Synthesis, Optimizations and Applications*, Sunil Khatri and Kanupriya Gulati (Editors), pages 67-85, Springer, 2011. (book chapter)

R.-R. Lee, J.-H. R. Jiang, and W.-L. Hung. "Bi-decomposition Using SAT and Interpolation. In *Advanced Techniques in Logic Synthesis, Optimizations and Applications*, Sunil Khatri and Kanupriya Gulati (Editors), pages 87-105, Springer, 2011. (book chapter)

J.-H. R. Jiang, H.-P. Lin, and W.-L. Hung. "Extracting Functions from Boolean Relations Using SAT and Interpolation. In *Advanced Techniques in Logic Synthesis, Optimizations and Applications*, Sunil Khatri and Kanupriya Gulati (Editors), pages 287-307, Springer, 2011. (book chapter)

C.-F. Lai, J.-H. R. Jiang, and Kuo-Hua Wang. Boolean Matching of Function Vectors with Strengthened Learning. In *Proc. IEEE/ACM Int'l Conf. on Computer-Aided Design* (ICCAD), San Jose, USA, November 2010.

B.-H. Wu, C.-J. Yang, C.-Y. Huang, and J.-H. R. Jiang. A Robust Functional ECO Engine by SAT Proof Minimization and Interpolation Techniques. In *Proc. IEEE/ACM Int'l Conf. on Computer-Aided Design* (ICCAD), San Jose, USA, November 2010.

C.-F. Lai, J.-H. R. Jiang, and K.-H. Wang. BooM: A Decision Procedure for Boolean Matching with Abstraction and Dynamic Learning. In *Proc. ACM/IEEE Design Automation Conf.* (DAC), pages 499-504, Anaheim, USA, June 2010. (best paper nominee)

J.-H. R. Jiang and T. Villa. Hardware Equivalence and Property Verification. In *Boolean Methods and Models in Mathematics, Computer Science and Engineering*, Yves Crama and Peter L. Hammer, editors, Cambridge University Press, 2010. (book chapter)

J.-H. R. Jiang, C.-C. Lee, A. Mishchenko, and C.-Y. Huang. To SAT or Not to SAT: Scalable Exploration of Functional Dependency. *IEEE Transactions on Computers*, 59(4): 457-467, April 2010.

K.-H. Ho, J.-H. R. Jiang, and Y.-W. Chang. TRECO: Dynamic Technology Remapping for Timing Engineering Change Orders. In *Proc. Asia and South Pacific Design Automation Conf.* (ASP-DAC), Taipei, Taiwan, January 2010.

J.-H. R. Jiang, H.-P. Lin, and W.-L. Hung. Interpolating Functions from Large Boolean Relations. In *Proc. IEEE/ACM Int'l Conf. on Computer-Aided Design* (ICCAD), San Jose, USA, November 2009.

N. Eliseeva, J.-H. R. Jiang, N. Kushik, and N. Yevtushenko. Symmetrization in Digital Circuit Optimization. In *Proc. IEEE East-West Design & Test Symposium* (EWDTS), Moscow, Russia, September 2009.

J.-H. R. Jiang. Quantifier Elimination via Functional Composition. In *Proc. Int'l Conf. on Computer Aided Verification* (CAV), pp. 383–397, Grenoble, France, June 2009.

J.-H. R. Jiang and T. Villa. Hardware Equivalence and Property Verification. In *Boolean Methods and Models in Mathematics, Computer Science and Engineering*, Peter L. Hammer and Yves Crama, editors, to be published by Cambridge University Press.

J.-H. R. Jiang and S. Devadas. Logic Synthesis in a Nutshell. In *Electronic Deisng Automation: Synthesis, Verification, and Test*, Laung-Terng Wang, Kwang-Ting (Tim) Cheng, and Yao-Wen Chang, editors, pp. 299–404, Morgan Kaufmann Publishers, 2009.

A. Mishchenko, R. K. Brayton, J.-H. R. Jiang, and S. Jang. Scalable Don't Care based Logic Optimization and Resynthesis. In *Proc. ACM International Symposium on Field Programmable Gate Arrays* (FPGA), pp. 151–160, Monterey, California, USA, February 2009.

H.-P. Lin, J.-H. R. Jiang, and R.-R. Lee. To SAT or Not to SAT: Ashenhurst Decomposition in a Large Scale. In *Proc. IEEE/ACM Int'l Conf. on Computer-Aided Design* (ICCAD), pp. 32–37, San Jose, USA, November 2008.

S.-C. Huang and J.-H. R. Jiang. A Dynamic Accuracy-Refinement Approach to Timing-Driven Technology Mapping. In *Proc. IEEE Int'l Conf. on Computer Design* (ICCD), pp. 538–543, Lake Tahoe, USA, October 2008.

R.-R. Lee, J.-H. R. Jiang, and W.-L. Hung. Bi-Decomposing Large Boolean Functions via Interpolation and Satisfiability Solving. In *Proc. ACM/IEEE Design Automation Conf.* (DAC), pp. 636–641, Anaheim, USA, June 2008.

J.-H. R. Jiang, D.-W. Chiou, and C.-E. Wu. Quantum Mechanical Search and Harmonic Perturbation. *Quantum Information Processing*, 6(5): 349–362, October 2007.

J.-H. R. Jiang and W.-L. Hung. Inductive Equivalence Checking under Retiming and Resynthesis. In *Proc. IEEE/ACM Int'l Conf. on Computer-Aided Design* (ICCAD), pp. 326–333, San Jose, USA, November 2007.

C.-C. Lee, J.-H. R. Jiang, C.-Y. Huang, and A. Mishchenko. Scalable Exploration of Functional Dependency by Interpolation and Incremental SAT Solving. In *Proc. IEEE/ACM Int'l Conf. on Computer-Aided Design* (ICCAD), pp. 227–233, San Jose, USA, November 2007. (best paper nominee)

C.-H. Hsu, S.-J. Chou, J.-H. R. Jiang, and Y.-W. Chang. A Statistical Approach to the Timing-Yield Optimization of Pipeline Circuits. In *Proc. Int'l Workshop on Power and Timing Modeling, Optimization and Simulation* (PATMOS), pp. 148–159, Goteborg, Sweden, September 2007.

A. Mishchenko, R. K. Brayton, J.-H. R. Jiang, and S. Jang. SAT-based Logic Optimization and Resynthesis. In *Proc. Int'l Workshop on Logic Synthesis* (IWLS), pages 358–364, San Diego, USA, May 2007.

J.-H. R. Jiang, D.-W. Chiou, and C.-E. Wu. Quantum Mechanical Search and Harmonic Perturbation. In quant-ph/0702007, February 2007.

J.-H. R. Jiang and R. K. Brayton. Retiming and Resynthesis: A Complexity Perspective. *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, December, 2006.

A. Mishchenko, S. Chatterjee, J.-H. R. Jiang, and R. K. Brayton. Integrating Logic Synthesis, Technology Mapping, and Retiming. In *Proc. Int'l Workshop on Logic and Synthesis*, pp. 177–181, 2005.

J.-H. R. Jiang. On Some Transformation Invariants under Retiming and Resynthesis. In *Proc. Int'l Conf. on Tools and Algorithms for the Construction and Analysis of Systems* (TACAS), pp.413–428, Edinburgh, UK, April 2005.

A. Mishchenko, S. Chatterjee, J.-H. R. Jiang, and R. K. Brayton. FRAIGs: A Unifying Representation for Logic Synthesis and Verification. ERL Technical Report, EECS Dept., UC Berkeley, March 2005.

A. Mishchenko, R. K. Brayton, J.-H. R. Jiang, T. Villa, N. Yevtushenko. Efficient Solution of Language Equations Using Partitioned Representations. In *Proc. Design Automation and Test in Europe* (DATE), pp.418–423, Munich, Germany, March 2005.

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**Patents**

Yi-Ting Chung and Jie-Hong R. Jiang. Functional Timing Analysis Method for Circuit Timing Verification. U.S. Patent (Patent No 8671375 B1).