Curriculum Vitae

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Research interests

Formal verification, logic synthesis, quantum computation, gene regulatory network analysis

Education

December 2004	Ph.D., EECS, University of California, Berkeley, USA
June 1998	M.S., Electronics Engineering, National Chiao Tung University, Taiwan
June 1996	B.S., Electronics Engineering, National Chiao Tung University, Taiwan

Experience

August 2009 –	Associate Professor Dept. of Electrical Engineering / Grad. Inst. of Electronics Engineering National Taiwan University
August 2005 – July 2009	Assistant Professor Dept. of Electrical Engineering / Grad. Inst. of Electronics Engineering National Taiwan University
January 2005 – August 2005	Postdoctoral Researcher Department of Electrical Engineering and Computer Sciences University of California, Berkeley (research on formal verification, hardware synthesis, quantum computation)
June 2001 – December 2004	Research Assistant Department of Electrical Engineering and Computer Sciences University of California, Berkeley (research and development of verification and synthesis techniques for electronic design automation)
August 2004 – December 2004	Teaching Assistant Department of Electrical Engineering and Computer Sciences University of California, Berkeley (EE42 Introduction to Digital Electronics)
June 2003 – September 2003	Graduate Intern Verplex Systems, Inc./Cadence Design Systems, Inc. (research and development of sequential equivalence checking algorithms)

Experience (cont'd)

January 2003 – May 2003	Teaching Assistant Department of Electrical Engineering and Computer Sciences University of California, Berkeley (EE219B Logic Synthesis)
June 2000 – August 2000	Research Assistant Department of Electrical Engineering and Computer Sciences University of California, Berkeley (MVSIS project)
July 1998 – April 2000	Second Lieutenant Air Force, Taiwan, R.O.C. (compulsory military service)

Honors and awards

2000 – 2001	UC Regent's Fellowship
1998	Dragon Thesis Award (Acer Foundation)
1998	Member of Phi Tau Phi
1997 – 1998	Fellowship of the Ministry of Education, Taiwan
1997	Memorial Scholarship of Dr. Sun Yat-Sen's Centennial
1996	Gold Prize, NCTU Undergraduate Research and Development Award
1995 – 1996	Academic Achievement Award (Department of Electronics Engineering, National Chiao Tung University)

Professional societies

Association of Computing Machinery (ACM)
Institute of Electrical and Electronics Engineers (IEEE)

Professional activities

Referee of ACM Transactions on Design Automation of Electronic Systems, ACM/IEEE Design Automation Conference, IEEE Asia and South Pacific Design Automation Conference, IEEE Design Automation and Test in Europe, IEEE/ACM International Conference on Computer-Aided Design

Session Chair of ACM/IEEE Design Automation Conference 2009

Program Committee Member of International Workshop on Logic and Synthesis 2010, IEEE International Symposium on Theoretical Aspects of Software Engineering 2010, International Conference on Formal Methods in Computer Aided Design 2010

Teaching

Fall 2010	Computer-Aided VLSI System Design (NTU)
Fall 2010	Logic Synthesis and Verification (NTU)
Spring 2010	Logic Synthesis and Verification (NTU)
Fall 2009	Switching Circuits and Logic Design (NTU)
Fall 2009	Computer-Aided VLSI System Design (NTU)
Summer 2009	Formosan Summer School on Logic, Language, and Computation (Academia Sinica, NTU)
Spring 2009	Special Topics on Applied Mathematical Logic (NTU)
Fall 2008	Introduction to Electronic Design Automation (NTU)
Fall 2008	Logic Synthesis and Verification (NTU)
Spring 2008	Special Topics on Applied Mathematical Logic (NTU)

Teaching (cont'd)

Fall 2007	Introduction to Electronic Design Automation (NTU)
Fall 2007	Logic Synthesis and Verification (NTU)
Spring 2007	Nonlinear Programming (NTU)
Fall 2006	Introduction to Electronics Design Automation (NTU)
Fall 2006	Logic Synthesis and Verification (NTU)
Spring 2006	Nonlinear Programming (NTU)
Fall 2005	Logic Synthesis and Verification (NTU)
Spring 2005	EE290A - Sequential Logic Synthesis and Verification (UCB)
Fall 2004	EE42 - Introduction to Digital Electronics (UCB)
Spring 2003	EE219B - Logic Synthesis (UCB)

Publications

A. Mishchenko, R. K. Brayton, J.-H. R. Jiang, and S. Jang, "Scalable don't-care-based logic optimization and resynthesis," *ACM Trans. on Reconfigurable Technology and Systems* (TRETS), to appear.

J.-H. R. Jiang, H.-P. Lin, and W.-L. Hung, "Extracting Functions from Boolean Relations Using SAT and Interpolation," in *Advanced Techniques in Logic Synthesis, Optimizations and Applications*, Sunil P. Khatri and Kanupriya Gulati, editors, Springer, 2010. (book chapter)

H.-P. Lin, J.-H. R. Jiang, and R.-R. Lee, "Ashenhurst Decomposition Using SAT and Interpolation," in *Advanced Techniques in Logic Synthesis, Optimizations and Applications*, Sunil P. Khatri and Kanupriya Gulati, editors, Springer, 2010. (book chapter)

R.-R. Lee, J.-H. R. Jiang, and W.-L. Hung, "Bi-Decomposition Using SAT and Interpolation," in *Advanced Techniques in Logic Synthesis, Optimizations and Applications*, Sunil P. Khatri and Kanupriya Gulati, editors, Springer, 2010. (book chapter)

C.-F. Lai, J.-H. R. Jiang, and Kuo-Hua Wang, "Boolean Matching of Function Vectors with Strengthened Learning," in *Proc. Int'l Conf. on Computer-Aided Design* (ICCAD'10), San Jose, USA, November 2010.

B.-H. Wu, C.-J. Yang, C.-Y. Huang, and J.-H. R. Jiang, "A Robust Functional ECO Engine by SAT Proof Minimization and Interpolation Techniques," in *Proc. Int'l Conf. on Computer-Aided Design* (ICCAD'10), San Jose, USA, November 2010.

C.-F. Lai, J.-H. R. Jiang, and K.-H. Wang, "BooM: A Decision Procedure for Boolean Matching with Abstraction and Dynamic Learning," in *Proc. ACM/IEEE Design Automation Conference* (DAC'10), pages 499-504, Anaheim, USA, June 2010. (best paper nominee)

J.-H. R. Jiang and T. Villa, "Hardware Equivalence and Property Verification," in *Boolean Methods and Models in Mathematics, Computer Science and Engineering*, Yves Crama and Peter L. Hammer, editors, Cambridge University Press, 2010. (book chapter)

J.-H. R. Jiang, C.-C. Lee, A. Mishchenko, and C.-Y. Huang. To SAT or Not to SAT: Scalable Exploration of Functional Dependency. *IEEE Transactions on Computers*, vol. 59, no. 4, pages 457-467, April 2010.

K.-H. Ho, J.-H. R. Jiang, and Y.-W. Chang, "TRECO: Dynamic Technology Remapping for Timing Engineering Change Orders," in *Proc. Asia and South Pacific Design Automation Conference* (ASP-DAC'10), Taipei, Taiwan, January 2010.

J.-H. R. Jiang, H.-P. Lin, and W.-L. Hung, "Interpolating Functions from Large Boolean Relations," in *Proc. Int'l Conf. on Computer-Aided Design* (ICCAD'09), San Jose, USA, November 2009.

N. Eliseeva, J.-H. R. Jiang, N. Kushik, and N. Yevtushenko, "Symmetrization in Digital Circuit Optimization," in *Proc. IEEE East-West Design & Test Symposium* (EWDTS'09), Moscow, Russia, September 2009.

J.-H. R. Jiang, "Quantifier Elimination via Functional Composition," in *Proc. Int'l Conf. on Computer Aided Verification* (CAV'09), pp. 383–397, Grenoble, France, June 2009.

J.-H. R. Jiang and T. Villa, "Hardware Equivalence and Property Verification," in *Boolean Methods and Models in Mathematics, Computer Science and Engineering*, Peter L. Hammer and Yves Crama, editors, to be published by Cambridge University Press.

J.-H. R. Jiang and S. Devadas, "Logic Synthesis in a Nutshell," in *Electronic Deisng Automation: Synthesis, Verification, and Test*, Laung-Terng Wang, Kwang-Ting (Tim) Cheng, and Yao-Wen Chang, editors, pp. 299–404, Morgan Kaufmann Publishers, 2009.

A. Mishchenko, R. K. Brayton, J.-H. R. Jiang, and S. Jang, "Scalable Don't Care based Logic Optimization and Resynthesis," in *Proc. ACM International Symposium on Field Programmable Gate Arrays* (FPGA'09), pp. 151–160, Monterey, California, USA, February 2009.

H.-P. Lin, J.-H. R. Jiang, and R.-R. Lee, "To SAT or Not to SAT: Ashenhurst Decomposition in a Large Scale," in *Proc. IEEE/ACM Int'l Conf. on Computer-Aided Design* (ICCAD'08), pp. 32–37, San Jose, USA, November 2008.

S.-C. Huang and J.-H. R. Jiang, "A Dynamic Accuracy-Refinement Approach to Timing-Driven Technology Mapping," in *Proc. IEEE Int'l Conf. on Computer Design* (ICCD'08), pp. 538–543, Lake Tahoe, USA, October 2008.

R.-R. Lee, J.-H. R. Jiang, and W.-L. Hung, "Bi-Decomposing Large Boolean Functions via Interpolation and Satisfiability Solving," in *Proc. ACM/IEEE Design Automation Conference* (DAC'08), pp. 636–641, Anaheim, USA, June 2008.

J.-H. R. Jiang, D.-W. Chiou, and C.-E. Wu, "Quantum Mechanical Search and Harmonic Perturbation," *Quantum Information Processing*, vol. 6, issue 5, pp. 349–362, October 2007.

J.-H. R. Jiang and W.-L. Hung, "Inductive Equivalence Checking under Retiming and Resynthesis," in *Proc. IEEE/ACM Int'l Conf. on Computer-Aided Design* (ICCAD'07), pp. 326–333, San Jose, USA, November 2007.

C.-C. Lee, J.-H. R. Jiang, C.-Y. Huang, and A. Mishchenko, "Scalable Exploration of Functional Dependency by Interpolation and Incremental SAT Solving," in *Proc. IEEE/ACM Int'l Conf. on Computer-Aided Design* (ICCAD'07), pp. 227–233, San Jose, USA, November 2007. (best paper nominee)

C.-H. Hsu, S.-J. Chou, J.-H. R. Jiang, and Y.-W. Chang, "A Statistical Approach to the Timing-Yield Optimization of Pipeline Circuits," in *Proc. Int'l Workshop on Power and Timing Modeling, Optimization and Simulation* (PATMOS'07), pp. 148–159, Goteborg, Sweden, September 2007.

A. Mishchenko, R. K. Brayton, J.-H. R. Jiang, and S. Jang, "SAT-based Logic Optimization and Resynthesis," in *Proc. Int'l Workshop on Logic Synthesis* (IWLS'07), pages 358–364, San Diego, USA, May 2007.

J.-H. R. Jiang, D.-W. Chiou, and C.-E. Wu, "Quantum Mechanical Search and Harmonic Perturbation," in quant-ph/0702007, February 2007.

J.-H. R. Jiang and R. K. Brayton, "Retiming and Resynthesis: A Complexity Perspective," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, December, 2006.

A. Mishchenko, S. Chatterjee, J.-H. R. Jiang, and R. K. Brayton, "Integrating Logic Synthesis, Technology Mapping, and Retiming," in *Proc. Int'l Workshop on Logic and Synthesis*, pp. 177–181, 2005.

J.-H. R. Jiang, "On Some Transformation Invariants under Retiming and Resynthesis," in *Proc. Int'l Conf. on Tools and Algorithms for the Construction and Analysis of Systems* (TACAS'05), pp.413–428, Edinburgh, UK, April 2005.

A. Mishchenko, S. Chatterjee, J.-H. R. Jiang, and R. K. Brayton, "FRAIGs: A Unifying Representation for Logic Synthesis and Verification." ERL Technical Report, EECS Dept., UC Berkeley, March 2005.

A. Mishchenko, R. K. Brayton, J.-H. R. Jiang, T. Villa, N. Yevtushenko, "Efficient Solution of Language Equations Using Partitioned Representations," in *Proc. Design Automation and Test in Europe* (DATE'05), pp.418–423, Munich, Germany, March 2005.

J.-H. R. Jiang. *Discovering Invariants in the Analysis and Verification of Finite State Transition Systems.* Ph.D. Thesis, University of California, Berkeley, December, 2004.

J.-H. R. Jiang, A. Mishchenko, and R. K. Brayton, "On Breakable Cyclic Definitions," in *Proc. Int'l Conf. on Computer-Aided Design* (ICCAD'04), pp. 411–418, San Jose, USA, November 2004.

J.-H. R. Jiang and R. K. Brayton, "Functional Dependency for Verification Reduction," in *Proc. Int'l Conf. on Computer Aided Verification* (CAV'04), pp.268–280, Boston, USA, July 2004.

J.-H. R. Jiang and R. K. Brayton, "On the Verification of Sequential Equivalence," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 6, pp.686–697, June 2003.

J.-H. R. Jiang, A. Mishchenko, and R. K. Brayton, "Reducing Multi-Valued Algebraic Operations to Binary," in *Proc. Design Automation and Test in Europe* (DATE'03), pp.752–757, Munich, Germany, March 2003.

J.-H. R. Jiang and R. K. Brayton, "Depth-bounded Communication Complexity for Distributed Computation," in *Proc. Int'l Workshop on Logic and Synthesis* (IWLS'03), 2003.

M. Gao, J.-H. R. Jiang, Y. Jiang, Y. Li, A. Mishchenko, S. Sinha, T. Villa and R. K. Brayton, "Optimization of Multi-Valued Multi-Level Networks," (invited paper) in *Proc. Int'l Symposium on Multiple-Valued Logic* (ISMVL'02), 2002.

M. Gao, J.-H. R. Jiang, Y. Jiang, Y. Li, S. Sinha and R. K. Brayton, "MVSIS," in *Proc. Int'l Workshop on Logic Synthesis* (IWLS'01), 2001.

J.-H. R. Jiang, Y. Jiang and R. K. Brayton, "An Implicit Method for Multi-Valued Network Encoding," in *Proc. Int'l Workshop on Logic Synthesis* (IWLS'01), 2001.

J.-H. R. Jiang, J.-Y. Jou and J.-D. Huang, "Unified Functional Decomposition for FPGA Logic Synthesis," *IEEE Transactions on Very Large Scale Integration Systems*, vol. 9, no. 2, pages 251-260, April 2001.

J.-H. R. Jiang and I. H.-R. Jiang, "Optimum Loading Dispersion for High-Speed Tree-Type Decision Circuitry," in *Proc. Int'l Conf. on Computer-Aided Design* (ICCAD'99), pages 520-525, November 1999.

J.-H. R. Jiang, J.-Y. Jou and J.-D. Huang, "Compatible Class Encoding in Hyper-function Decomposition for FPGA Synthesis," in *Proc. Design Automation Conference* (DAC'98), pages 712-717, June 1998.

J.-H. R. Jiang, J.-Y. Jou, J.-D. Huang and J.-S. Wei, "A Variable Partitioning Algorithm of BDD for FPGA Technology Mapping," *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, pages 1813-1819, October 1997.

J.-H. R. Jiang, J.-Y. Jou, J.-D. Huang and J.-S. Wei, "BDD Based Lambda Set Selection in Roth-Karp Decomposition for LUT Architecture," in *Proc. Asia and South Pacific Design Automation Conference* (ASP-DAC'97), pages 259-264, January 1997.

Presentations

Scalable Hardware Synthesis and Verification with Craig Interpolation. Invited talk, Emerging Information and Technology Conference (EITC), Cambridge, MA, USA, August 2009.

Hardware Equivalence and Property Verification. Invited short course, Formosan Summer School on Logic, Language, and Computation (FLOLAC), Taipei, Taiwan, July 2009.

Quantifier Elimination via Functional Composition. Contributed paper, CAV, Grenoble, France, June 2009.

English Technical Writing. Invited talk, International PhD Student Workshop on SOC (IPS), Kenting, Taiwan, August 2008.

Inductive Equivalence Checking under Retiming and Resynthesis. Contributed paper, ICCAD, San Jose, CA, USA, November 2007.

Scalable Exploration of Functional Dependency by Interpolation and Incremental SAT Solving. Contributed paper, ICCAD, San Jose, CA, USA, November 2007.

A Statistical Approach to the Timing-Yield Optimization of Pipeline Circuits. Contributed paper, PATMOS, Gothenburg, Sweden, September 2007.

On Some Transformation Invariants under Retiming and Resynthesis. Contributed paper, TACAS, Edinburgh, UK, April 2005.

On breakable cyclic definitions. Contributed paper, ICCAD, San Jose, CA, November 2004.

Functional dependency for verification reduction. Contributed paper, CAV, Boston, MA, July 2004. (Invited presentation, Formal Circuit Verification Workshop, Pelion, Greece, August 2004.)

Invariant verification in the sum state space. Invited presentation, Formal Circuit Verification Workshop, Lisbon, Portugal, August 2003.

Reducing multi-valued algebraic operations to binary. Contributed paper, DATE, Munich, Germany, March 2003.

Sequential equivalence checking in the sum state space. Invited presentation, Dagstuhl, Germany, August 2002. (On the verification of sequential equivalence. Contributed paper, IWLS, New Orleans, LA, June 2002.)

An implicit method for multi-valued network encoding. Contributed paper, IWLS, Tahoe City, CA, June 2001.

Compatible class encoding in hyper-function decomposition for FPGA synthesis. Contributed paper, DAC, San Francisco, CA, June 1998.

References

Robert K. Brayton, Professor, UC Berkeley; `brayton@eecs.berkeley.edu`

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Andreas Kuehlmann, Professor, UC Berkeley; `kuehl@cadence.com`

Jing-Yang Jou, Professor, National Chiao Tung University; `jyjou@faculty.nctu.edu.tw`