Computer-Aided VLSI System Design

DFT/ATPG HW

Due in one week

Purpose

In this homework, you have to perform DFT insertion to the synthesized LCD controller gate-level netlist. You also have to generate test patterns by using TetraMAX® ATPG.

Problem 1: Synthesize the LCD Controller

1. Use your own HW2 design, or the HW2 reference design on the CVSD course webpage.
2. Synthesize the reference design subjected to the constraints from HW4.
3. Save the synthesized design.
4. Verify the synthesized design by your testbench in HW4.

HINT: You do not have to close design compiler after synthesis. You can continue to perform DFT insertion in the following steps without setting the design constraints again.

Problem 2: Perform DFT insertion

5. Perform DFT insertion with **4 scan chains** and fix any DRC violation.
6. Save the dft insertion results.
7. Modify your testbench and verify the dft inserted design.

HINT: You have to fix the input of the scan enable signal to normal mode.

Problem 3: Generate test patterns

8. Generate test patterns for the scan-ready design.
9. Save the ATPG results.
10. Verify the Verilog format test patterns

Online Submission (FTP):

Please submit a zipped file named *StudentID_HW5.zip*, including:

Script Files:

1. "syn.tcl" : synthesis and dft insertion script in one file
2. "atpg.tcl" : atpg script

Synthesis Results:

3. "lcd_ctrl.vg" : gate level netlist (non-scan)
4. "lcd_ctrl.sdf" : pre-scan (non-scan) sdf file
5. "report.txt" : pre-scan report summarizing timing, power, and area

DFT Insertion Results:

6. "lcd_ctrl_dft.vg" : gate level netlist (scan-ready)
7. "lcd_ctrl_dft.sdf" : post-scan (scan-ready) sdf file
8. "report_dft.txt" : post-scan report summarizing timing, power, and area
9. "lcd_ctrl_dft.spf" : test protocol file
10. "lcd_ctrl_dft.scan_path" : scan path report
11. "lcd_ctrl_dft.scan_path" : scan cell report

ATPG Results:

12. "lcd_ctrl_atpg.stil" : STIL format test patterns

Questions:

13. "Answers.txt" : answer the following questions by **your results**.
    (A) How many flip-flops are chained?
    (B) What is the area before scan chain insertion? What is the area after scan chain insertion? How much is the area overhead percentage of scan?
    (C) How long (ns) is the critical path delay before scan chain insertion? How long the critical path after scan chain insertion? How many percent is the delay overhead?
    (D) How many total faults (uncollapsed) are there in the circuit? What is the test coverage (%)? What is the fault coverage (%)?
    (E) How many patterns do we have?

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