SOC Encounter Homework

Description

In this homework, you are going to implement your Verilog HW2 design into GDSII layout. Please add to your synthesized design with *scan chains*, and include *pad cells* for SOC Encounter. Finally, you need to submit an electronic *report* (upload to the homework FTP site) describing what you have done. (There is no particular report style. However please include the specified items.)

Design Libraries & Data Preparation

The complete design libraries are available in ~cvsd/CUR/SOCE/SOCE_Lab.tar.gz used in P&R Labs. You can choose to add pad cells after synthesis, or before synthesis (use a wrapper-like gate-level top module with pad cells to include your RTL, more preferable). However notice that the input/output delay's definitions will be different. The SDC file is not part of the library, so you should create it by yourself, or you can use *write_sdc* in DV to generate it automatically. If the memory compiler is needed, related information can be found in Verilog Lab2. Be sure to generate all the memory data/libraries for SOC Encounter. Finally, you may check the Lab materials for more hints.

Online Submission (FTP):

Please submit a zipped PDF report named *StudentID_HW7.zip*, including:

Basic (75%)

1. Topic & timing/delay information.
2. Synthesis reports & DfT-related reports (summarized).
3. Final chip layout figure (big & clear enough to see) & chip size (*um x um*).
4. Pre-layout & post-layout simulation results (summarized).

Advanced (25%)

5. Complete power planning (VDD/VSS/IOVDD/IOVSS number, power ring/strips width, voltage drop & electron migration figures…).
6. Better I/O & modules' placement (explanations, amoeba view…).
7. Other related discussions if applicable.