I/O Pad Insertion for SOC Encounter

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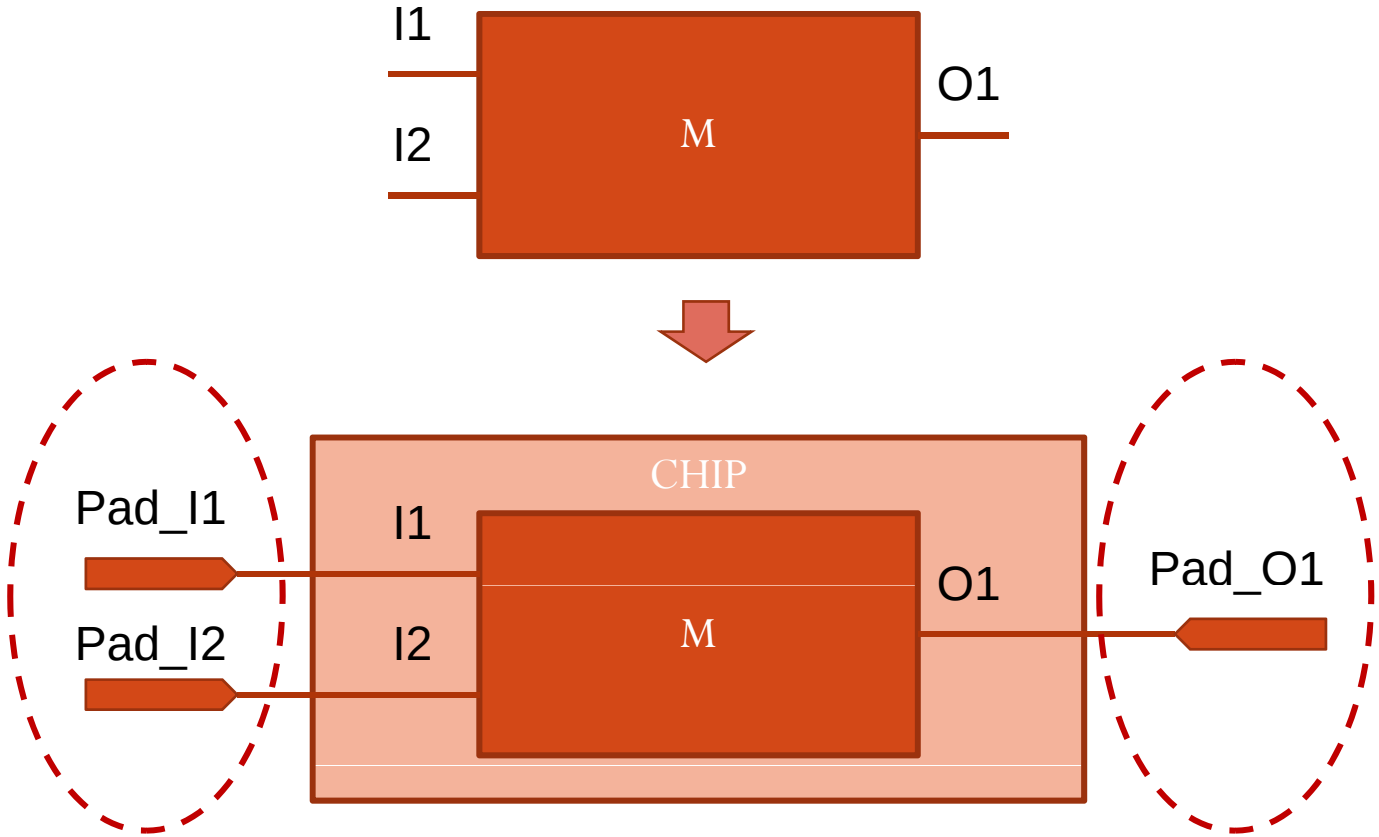
Gate-Level Netlist

- For a chip design, the I/O pads should be added on the top module.



Gate-Level Netlist (Example)

```
module M (O1, I1, I2);
  output O1;
  input I1;
  input I2;
Endmodule;
```

Original design (M.v)

```
module M (O1, I1, I2);
  output O1;
  input I1;
  input I2;
endmodule;

module CHIP (O1, I1, I2); // top module with I/O pads
  output O1;
  input I1, I2;
  wire i_I1, i_I2, i_O1;
  M M (.O1(i_O1), .I1(i_I1), .I2(i_I2));
  PDIDGZ Pad_I1 (.PAD(I1), .C(i_I1));
  PDIDGZ Pad_i2 (.PAD(I2), .C(i_I2));
  PDO02CDG Pad_O1(.PAD(O1), .I(i_O1));
endmodule;
```

Modified design (CHIP.v)

Gate-Level Netlist (Notes)

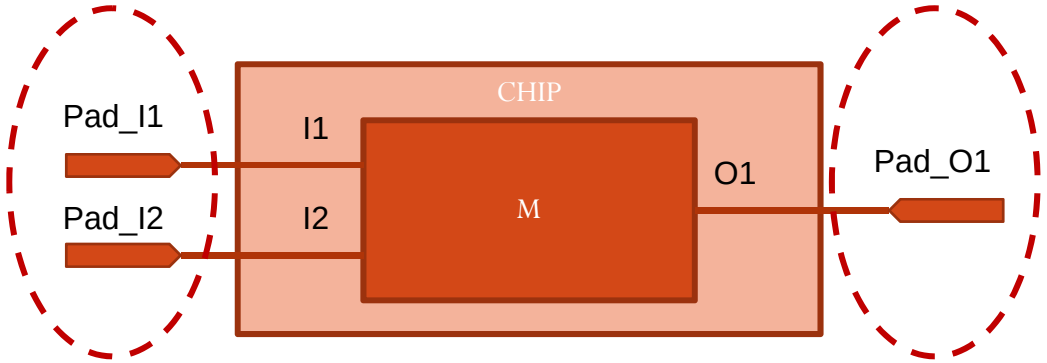
- Pads PDIDGZ and PDO02CDG are available types for input and output pads, respectively, for tsmc18 process. There are also other types of I/O pads could be used (please refer to tpz973.v) and for other libraries, different pads might be used (different names, of course).
- For accurate simulation, I/O pads should be also considered for timing delay assumptions. That is, tpz973.v should be included for tsmc18 process.
  - E.g., for verilog simulation, you should use

    ncverilog +access+r tsmc18.v tpz973.v CHIP.v

I/O Pad Assignment

- You should write .ioc file according to your design before P&R.
- In .v file, if no power pad information is included, you may add a new power pad by yourself.
  - VDD: PVDD1DGZ, PVDD2DGZ // tsmc18 library
  - VSS: PVSS1DGZ, PVSS2DGZ // tsmc18 library
  - Note: there are two types of power pads: (1) power pads for the core (design), (2) power pads for I/O pads
- Corner pads
  - PCORNERDG // tsmc18 library
- For other pads (design inputs/outputs), you should arrange them by yourself.

I/O Pad Assignment (Example)

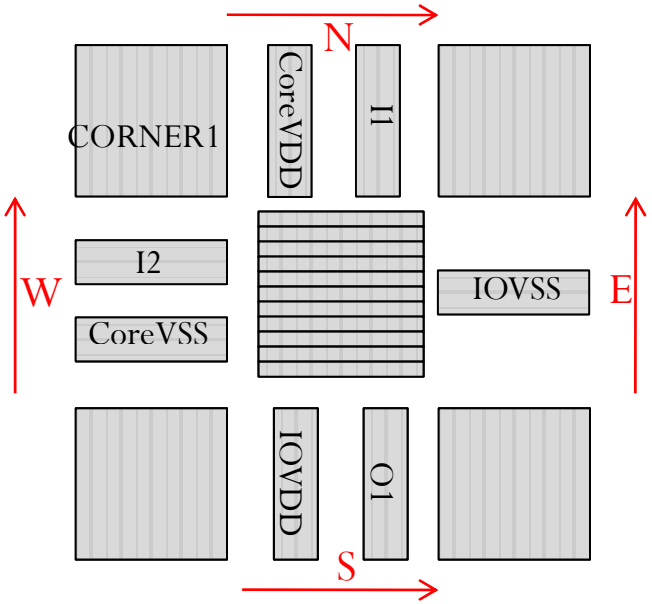



```
Version: 1
Pad: CORNER1        NW  PCORNERDG
Pad: Pad_I1          N
Pad: Pad_CoreVDD     N   PVDD1DGZ

Pad: CORNER2        NE  PCORNERDG
Pad: Pad_I2          W
Pad: PAD_CoreVSS     W   PVSS1DGZ

Pad: CORNER3        SW  PCORNERDG
Pad: Pad_O1          S
Pad: PAD_IOVDD       S   PVDD2DGZ

Pad: CORNER4        SE  PCORNERDG
Pad: PAD_IOVSS       E   PVSS2DGZ
```



I/O Pad Assignment (Notes)

- For correct P&R, you should make sure that in the .v file (CHIP.v), I/O pads are correctly connected to your original design without pads.
- For power and corner pads (which are not included in the .v file), pad types should be specified in the .ioc file.
- Pads are not necessarily uniformly distributed. (That is, we can have different numbers of pads in different directions) However, uniform assignment is suggested.
- You might use more than one set of power pads (E.g., IOVDD1, IOVDD2, CoreVDD1, CoreVDD2).
- Different rearrangements will result in different placement, routing, timing, power, etc.