Computer-Aided VLSI System Design

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Fall 2010

Course Info

- Instructor
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- Course webpage
  - http://cc.ee.ntu.edu.tw/~jhjiang/instruction/courses/fall10-cvsd/cvsd.html
  - Lecture materials will be password protected due to copyright issues
    - Password is ???

Schedule

Date	Lecture	Lecturer	Lab	Lab Tutor	Assignment	Project
9月17日	Overview	Roland	Linux; X-editor	林辰軒		
9月24日	Verilog (1): Cadence Verilog Language - Chapter 1-11	蘇冠羽	Verilog Lab 1	張恩瑞	Verilog HW 1	
10月1日	Verilog (2): Cadence Verilog Language - Chapter 11-17	蘇冠羽	Verilog Lab 2	張恩瑞		
10月8日	Verilog (3): Behavior Modeling and Debugging (Verdi)	張恩瑞	---		Verilog HW 2	
10月15日	Verilog (4): Testbench Writing and Synthesizable Codes	張恩瑞	---			Topic Announcement
10月22日	Synthesis (1): Design Compiler	林辰軒	Synthesis Lab	張家偉	Synthesis HW; Verilog HW 3	
10月29日	Synthesis (2): Design Compiler	林辰軒	---			
11月5日	DFT and ATPG (Tetramax)	陳柏瑞	DFT/ATPG Lab	白炳川	DFT/ATPG HW	
11月12日	Midterm Exam					Proposal Due
11月19日	Static Timing Analysis (PrimeTime)	黃泳霖	STA Lab	黃泳霖	Verilog HW 4	
11月26日	Placement and Routing (SoC Encounter)	徐孟楷	P&R Lab 1	徐孟楷		
12月3日	Placement and Routing (SoC Encounter)	施信瑋	P&R Lab 2	施信瑋	P&R HW	
12月10日	DRC, LVS, LPE (Calibre)	許博豪	DRC/LVS Lab	許博豪		
12月17日	Verification	吳政穎	Verification Lab	葉昱甫		
12月24日	FPGA	莊富凱/廖家群	FPGA Lab	莊富凱/廖家群		
12月31日	Project Presentation					
1月7日	Project Presentation					
1月14日	Project Presentation					Final Report Due

Grading

- Lab 10%
- Homework 40%
- Midterm 25%
- Project 25%
  - Presentation 5%
  - Final report 20%

Policies

- No cheating and plagiarism
  - 0 final score for any cheating/plagiarism identified
- Check with TAs before leaving each lab to make sure all goals accomplished and to get credits
- Enrollment
  - Capacity limit about 90 students
    - Priority
      1. GIEE, PhD
      2. GIEE, MS 2+
      3. EE, 4
      4. GIEE, MS 1
      5. Other graduate students

Format

- Lecture
  - In 229 EE2
  - 2-3 hours
- Lab
  - Introduction in 229 EE2
  - Practice in PC rooms 130, 132 EE2; or practice in 229 using your own laptop
  - 0-1 hour

To-Do List

- Get cad.ee.ntu.edu.tw (IC design lab, 231 EE2) account
  - Visit http://cad.ee.ntu.edu.tw
  - Print out and fill in account application form; put it in Prof. Jiang's mailbox (in EE2 Building) by 9/20 for processing
  - You'll need the account for next week's lab
- Acquire the Cadence Verilog reader
  - Order it in the printing center located in the basement of the NTU main library (or have it by other means)
    - (Reference prices $199 w/ binding; $170 w/o binding)
  - Please have it at hand in next two weeks' lectures