Computer-Aided VLSI System Design (CVSD), Fall 2010

National Taiwan University

http://cc.ee.ntu.edu.tw/~jhjiang/instruction/courses/fall10-cvsd/cvsd.html

Term Project

Objectives:

In this project, you will need to use all the tools that you learned in the class to design your own IC. The second choice is that you can help to test new design tools and methodologies or develop new design flows for students in the future.

Suggested Topics

There are two types of projects, VLSI Design and Design Flow/Methodology Exploration.

Type 1: VLSI Design

For Type 1 projects, you can choose one of the following topics and design an IC with the design flow taught in this course. Note that, the completeness of your project is very important. You must go through the whole design flow and generate the final layout which can pass the post-sim simulation. Besides, the more complete verification process, the higher score you can get. Suggested topics include but not limited to

1. Parwan processor (level of difficulty: low)

This is an academic 8-bit simple processor. In this project, we will extend its functionality. In additional to using tool, you will also learn microprocessor architecture, verification, coding style and so on. For more details, see the file in the cad server under ~cvsd/10F/Project/Parwan/ directory. See the file *parwanProject.doc* for a full description of this project.

2. 8251 USART (level of difficulty: low)

In this project, you will learn design and verification of a useful circuit, the Intel 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART), designed for data communication with Intel's microprocessor families. It is used as a peripheral device and is programmed by the CPU to operate using many serial data transmission techniques. The USART accepts data characters from the CPU in parallel format and

then converts them into a continuous serial data stream. It accepts serial data streams and converts them into parallel data characters for the CPU. For more details, see the file in the cad server under ~cvsd/10F/Project/8251/ directory. See the file *8251Project.doc* for a full description of this project.

3. DCT (level of difficulty: low)
Discrete cosine transform (DCT) is an important module in JPEG, MPEG, and H.26x video/image compression standards. In this project, based on a well-known paper of DCT hardware architecture, you will learn how to implement the hardware architecture with Verilog-HDL and design the chip for DCT. This project is also a typical example of hardware design for digital signal processing applications. For more details, see the file in the cad server under ~cvsd/10F/Project/dct/ directory. See the file *dctProject.doc* for a full description of this project.

4. 8051 micro controller (level of difficulty: high) maximum 4 members allowed
The 8051 are microcontroller with an 8-bit CPU, memory, interrupt controller, timers, serial I/O and digital I/O on a single piece of silicon. It has wide applications and is very popular in the embedded systems. You will gain a lot of experience from this "real world" design. For more details, see the file in the ~cvsd/10F/Project/8051/ directory. Please see the *8051Project.doc* for a full description of this project.

6. MIPS processor (level of difficulty: high) maximum 4 members allowed
This is a 5-stage pipeline processor. The goal of this project is to develop a MIPS like processor and verify it. A past report about the project can be found in the cad server under ~cvsd/10F/Project/MIPS directory.

5. Opencores.org (level of difficulty depends)
You can search for some useful cores in the opencores website (http://www.opencores.org). Your choice has to be suitable in size (i.e. no smaller than 10K gates). You can refer to their source RTL codes but you CANNOT copy their source codes.

7. Other topics (level of difficulty depends)
You can design an IC that you will need in your own research, but the gate count should be larger than 10K gates.

Type 2: New Design Flow/Methodology Exploration

For Type 2 projects, you can help to explore new design flow/methodology for future

instruction. You can help to apply new design tools and methodologies and show us the performance of them. Or, you can help to enhance the design flow of this course. Note that, the completeness is very important. You must test the new tool with real designs (you can ask them from TAs) and show the performance of this new tool as well as your comments. Besides, please make the handouts, tutorials, labs, or other documentation for this new tool. The more complete documentation, the higher score you can get. Suggested topics include but not limited to

1. Design flow with SystemVerilog (level of difficulty: medium)
2. Design flow with SystemC and ESL tools (level of difficulty: high)
3. Design flow with Formality (level of difficulty: low)
4. New P&R tool: Magama (level of difficulty: high)
5. P&R with multiple power domains (level of difficulty: medium)
6. Advanced design techniques with power compiler (level of difficulty: low)
7. Other new tools, implementation styles, design methodologies, and design flow (level of difficulty depends). See CIC webpage at http://www.cic.org.tw for available tools and choices.

Teaming

You can team up a group of no more than 3 students (unless specified otherwise). Each student is graded independently according to his own contributions.

Project Schedule

11/12/2010 proposal due (including your topic, team members, and a short description of your plan); name your proposal as ***StudentID_Proposal.txt*** or ***StudentID_Proposal.pdf*** and submit through the ftp server announced on the course webpage (one submission is sufficient for each team)

12/10/2010 progress report (in about 4 pages describe your progress); name your proposal as ***StudentID_Progress.pdf*** and submit through the ftp server announced on the course webpage (one submission is sufficient for each team)

12/31, 01/07, 01/14 presentation (10~20 minutes each group)

01/17/2010 final report due

Presentation

Suggest one presenter for each group and 10~20 minute presentation (to be specified).

Use figures or tables, instead of text, whenever possible. Show ONLY your special features and the detailed implementation specifications, such as area, gate-count, working frequency, etc. Do not spend time on what other people already know.

Requirements for final report and submission

- (Type 1) In the report, you will need to describe clearly how you did the following jobs:

  RTL coding, functional verification and debugging, synthesis, scan chain insertion and ATPG, timing analysis, place and route, DRC/LVS, and power analysis

  FPGA implementation is a bonus, but not required.
- (Type 1) In the report, show important results, including area, equivalent gate count, timing, ATPG test pattern length, fault coverage, die size, and power. Attach important parts of your codes and scripts if needed.
- (Type 2) The report should be a complete documentation of the new design tool, including presentation PowerPoint files, tutorial documentation, codes, and scripts. The performance evaluation should also be included.

In the report, you must SPECIFY contributions of each member. General tasks (such as reading the codes, reading manuals) cannot be counted as contributions. Each member is graded according to his/her contributions.

List reference papers, documentations, and URLs if any.

Hardcopy of your report has to be submitted to Prof. Jiang's office (242, EEII) by 17:00 pm on the due date. Attach a CD-ROM with your hardcopy report. Include all your related files (including scripts, codes, report, results, etc).

Note that, you have to give up the copyright of your reports (including the documents, PowerPoint, codes, and scripts). The reports may be posted on the website to be accessed by students in the future.

Grading Policy

For those groups who have presentation,

- Presentation 20% (+5% extra bonus for good presentations)
- Final report 80% (efforts+innovation+completeness) x difficulty

  (level of difficulty: 1.2 =very difficult; 1.1=difficult; 1.0=medium; 0.9=easy; 0.8=very easy)

The proposal and progress report will be considered when your final score is on the

pass-fail boundary.