Computer-Aided VLSI System Design

DFT/ATPG HW

Due in one week

Purpose

In this homework, you have to perform DFT insertion to the synthesized color transform engine (CTE) gate-level netlist. You also have to generate test patterns by using TetraMAX® ATPG.

Problem 1: Synthesize the color transform engine (CTE)

1. Use your own CTE design in HW2, or the reference CTE design in HW4 on the CVSD course webpage.
2. Synthesize the reference design subjected to the constraints from HW4.
3. Save the synthesized design.
4. Verify the synthesized design by your testbench in HW4.

HINT: You can skip Problem 1 if you use the result of HW4. If you use the reference design, you do not have to close design compiler after synthesis. You can continue to perform DFT insertion in the following steps without setting the design constraints again.

Problem 2: Perform DFT insertion

5. Perform DFT insertion with **6 scan chains** and fix any DRC violation.
6. Save the dft insertion results.
7. Modify your testbench and verify the dft inserted design. Make sure your dft inserted design passes the verification step in *HW4(B)*.

HINT: You have to check the active state of your reset signal.

Problem 3: Generate stuck-at fault test patterns

8. Generate stuck-at fault test patterns for the scan-ready design.
9. Save the ATPG results.
10. Verify the Verilog format test patterns (optional).

Online Submission (FTP):

Please submit a zipped file named *StudentID_HW5.zip*, including:

Script Files:

1. “syn.tcl” : synthesis and dft insertion script in one file
2. “atpg.tcl” : atpg script

Synthesis Results:

3. “CTE.v” : gate level netlist (non-scan)
4. “CTE.sdf” : pre-scan (non-scan) sdf file
5. “report.txt” : pre-scan report summarizing timing, power, and area

DFT Insertion Results:

6. “CTE_dft.v” : gate level netlist (scan-ready)
7. “CTE_dft.sdf” : post-scan (scan-ready) sdf file
8. “report_dft.txt” : post-scan report summarizing timing, power, and area
9. “CTE_dft.spf” : test protocol file
10. “CTE_dft.scan_path” : scan path report
11. “CTE_dft.scan_path” : scan cell report

ATPG Results:

12. “CTE_atpg.stil” : STIL format test patterns

Questions:

13. “Answers.txt” : answer the following questions by **your results**. All answers must base on your own result. There is no golden answer for all students.
    (A) How many flip-flops are chained? How many scan cells in every scan chain, respectively? What are the inputs and outputs of these scan chains? What is the name of the scan enable pin for your scan chain?
    (B) What is the area before scan chain insertion? What is the area after scan chain insertion? How much is the area overhead percentage of scan chain? Try to explain why scan chain introduces area overhead.
    (C) Ignore the input external and output external delay. How long (ns) is the critical path delay before scan chain insertion? How long the critical path after scan chain insertion? How many percent is the path delay overhead? If the endpoint of the critical path is a register type gate, consider the setup time in your critical path delay. Sometimes, the most critical path changes. If your designs do so,

try to explain why. Sometimes, the individual gate delay changes in the critical path. Try to explain why?

(D) How many total faults (uncollapsed) are there in the circuit? How many patterns do we have? What is the test coverage (%)? What is the fault coverage (%)?

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