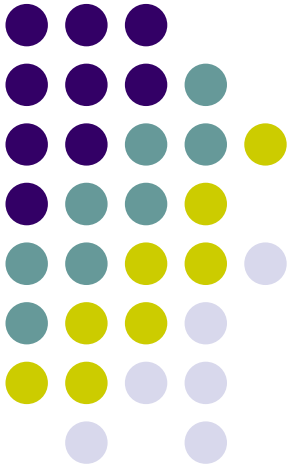
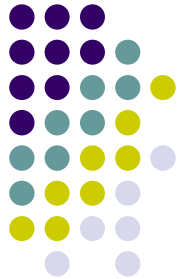
Introduction to FPGA

Guan-Lin Wu

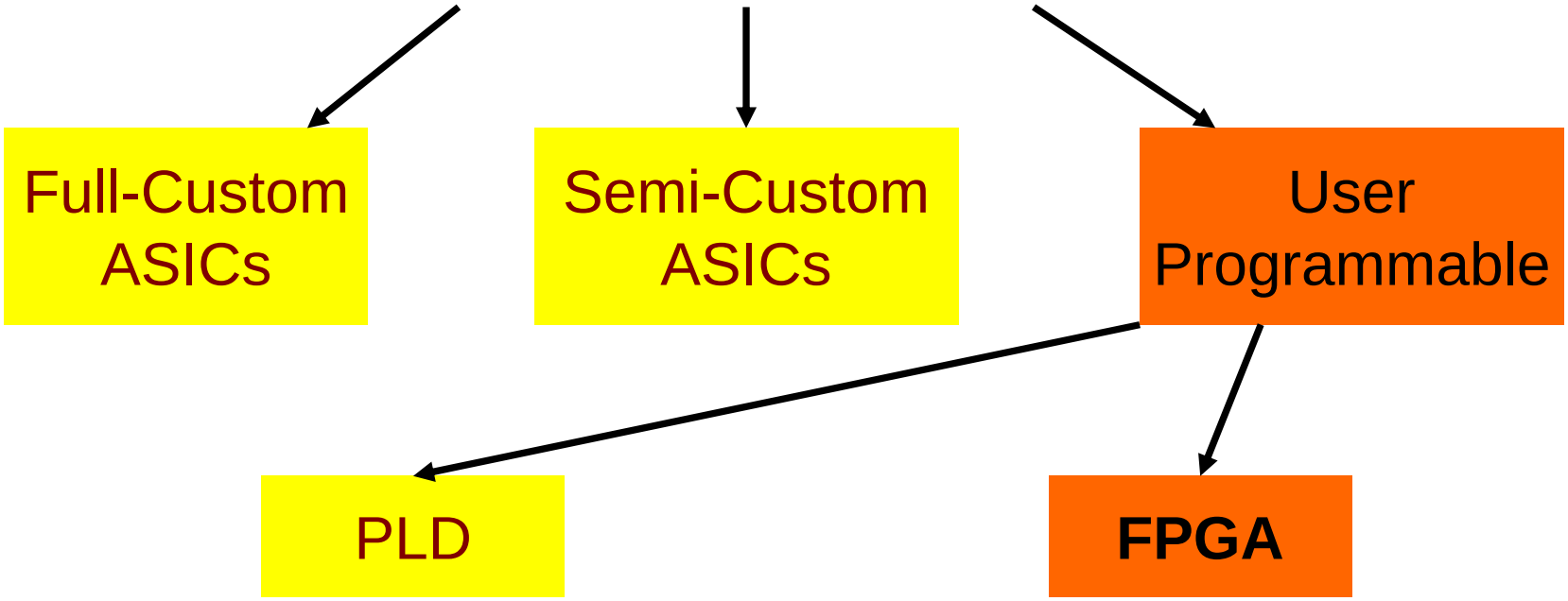


Outline



- Introduction to PLD
- Introduction to FPGA
- FPGA Example – Altera Cyclone II
- Altera Quartus II
- Lab

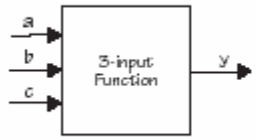
World of Integrated Circuits



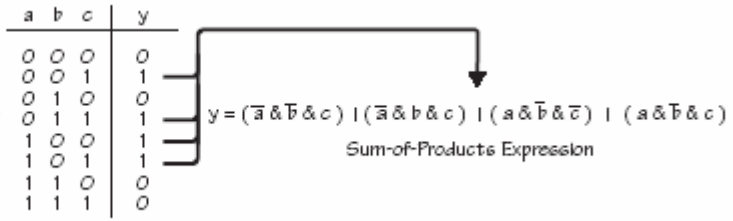
Digital Logic

Digital Logic Function

3 Inputs



Black Box



Truth Table

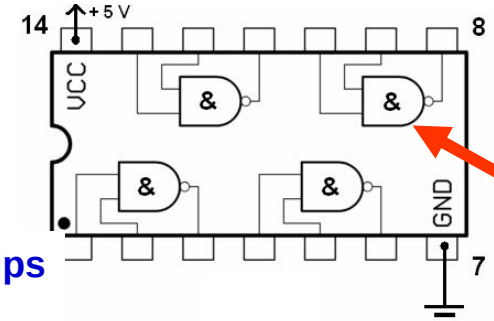
SUM of PRODUCTS

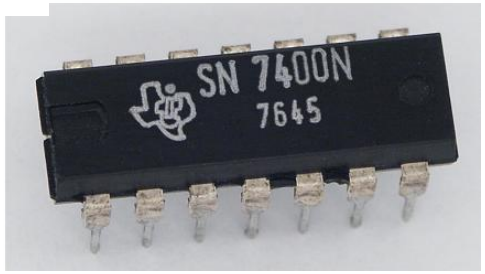
Product AND (&)
Sum OR (|)

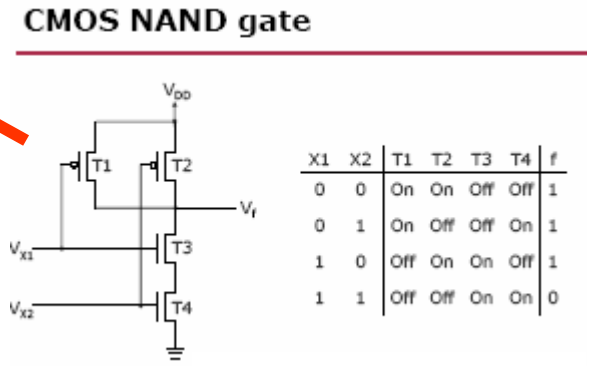
Boolean Logic Minimisation

Connect Standard Logic Chips
Very Simple Glue Logic

FIXED Logic



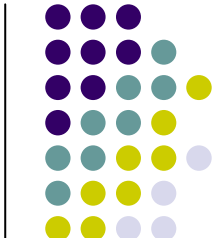




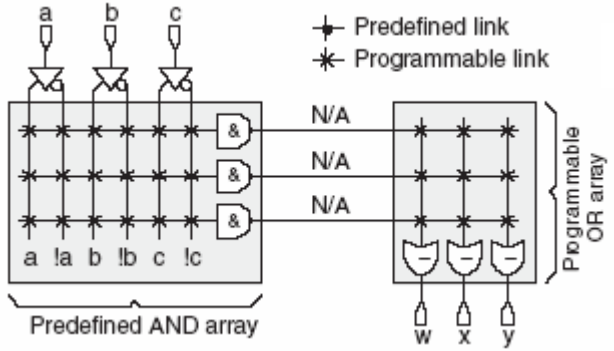
Transistor Switches

Programmable Logic Devices PLDs

- Different Types
- SUM of PRODUCTS
- Prefabricated
- Programmble Links
- Reconfigurable



Un-programmed State



Planes of ANDs, ORs

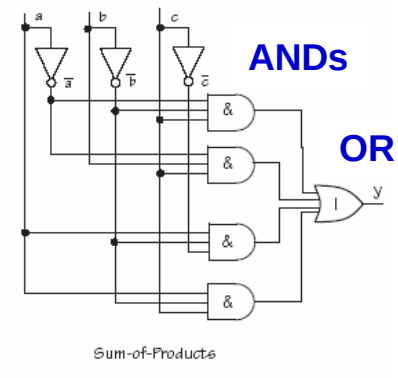
$y = (a \,\&\, b \,\&\, c)$

$x = (a \,\&\, b \,\&\, c) \mid (\bar{b} \,\&\, \bar{c})$

$w = (a \,\&\, c) \mid (\bar{b} \,\&\, \bar{c})$

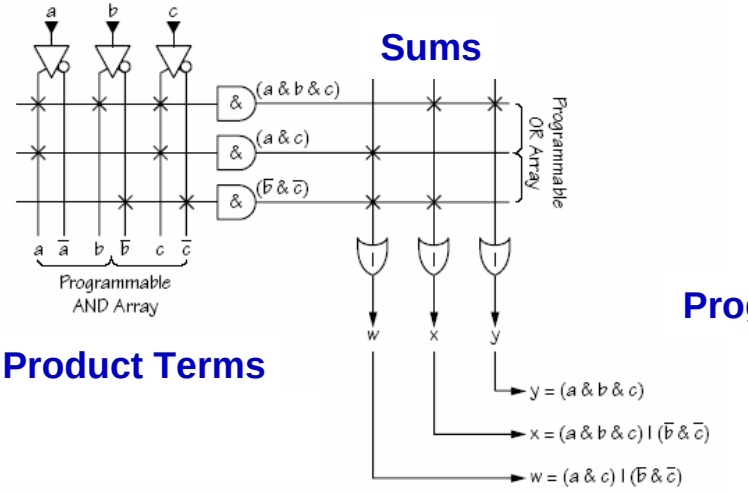
Logic Function

Inputs



Sum of Products

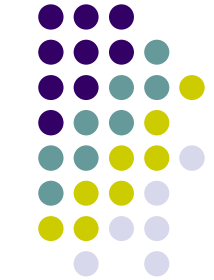
Sums



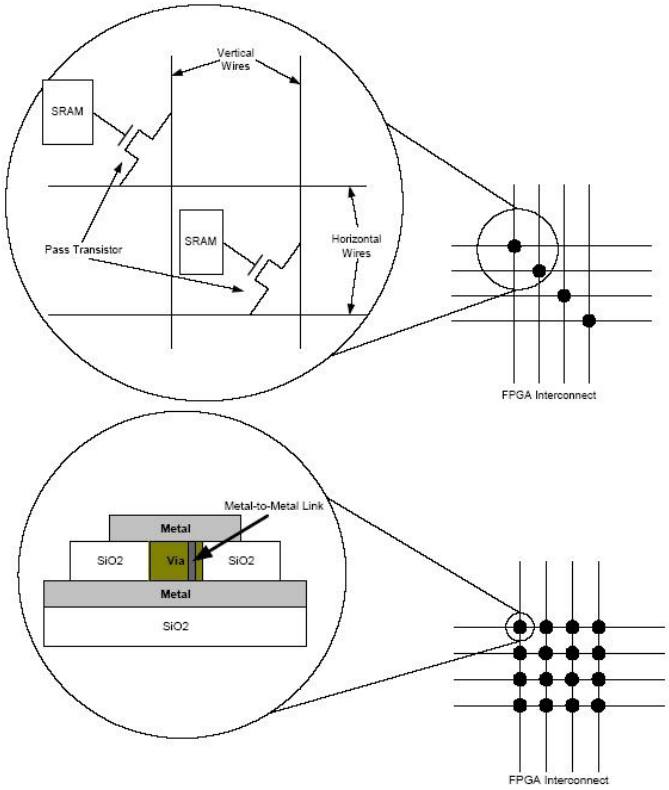
Product Terms

Programmed PLD

How can we make a “programmable logic”?

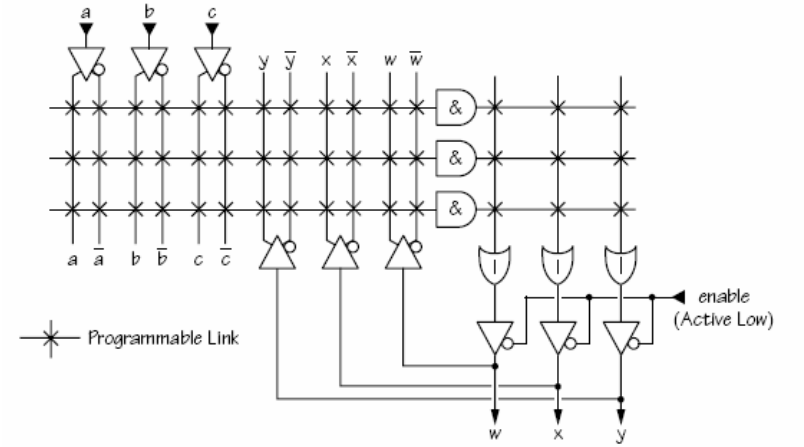


- SRAM-based
  - Reconfigurable
  - Track latest SRAM technology
  - Volatile
  - Generally high power
- Anti-fuse technique
  - One-time programmable
  - Non-volatile – security app.

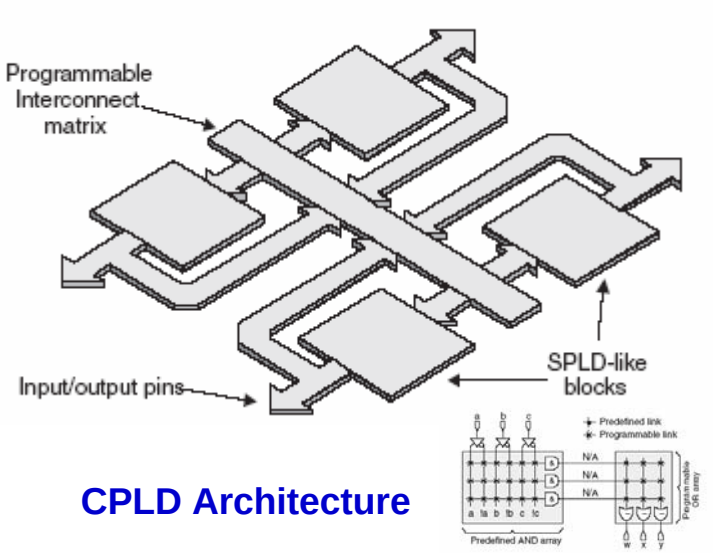


Complex PLDs

- CPLDs
- Programmable PLD Blocks
- Programmable Interconnects
- Electrically Erasable links

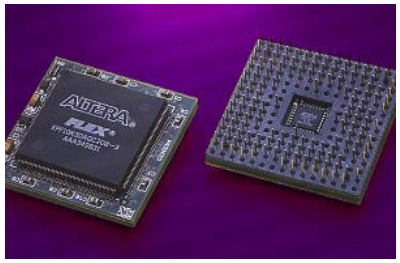


Feedback Outputs



CPLD Architecture

Field Programmable Gate Arrays FPGA

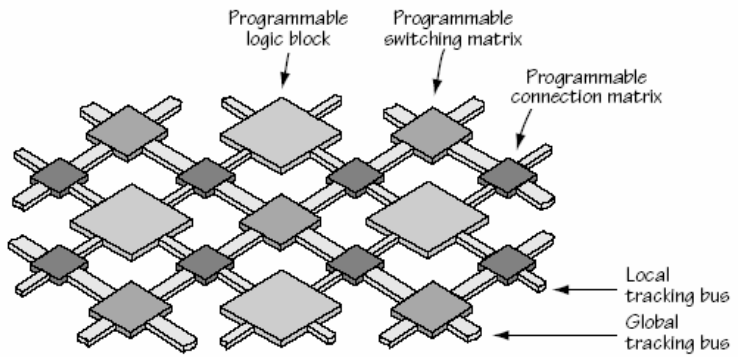


- Field Programmable Gate Array
  - New Architecture
  - ‘Simple’ Programmable Logic Blocks
  - Massive Fabric of Programmable Interconnects

Large Number of Logic Block ‘Islands’

1,000 … 100,000+

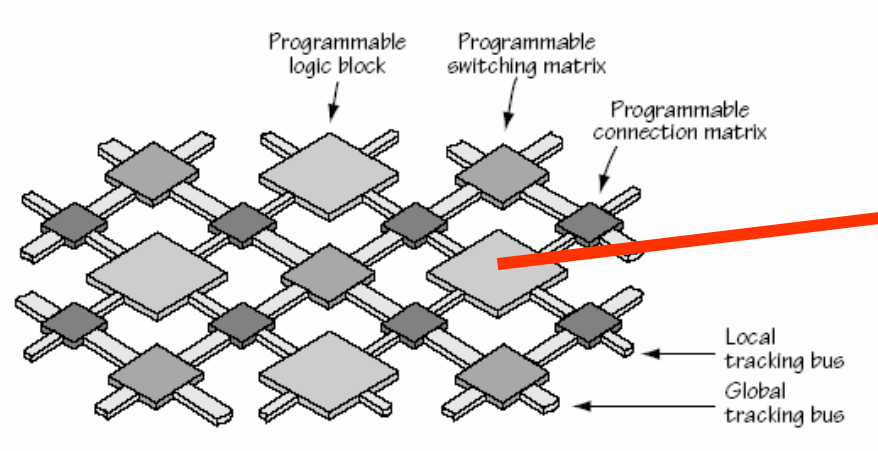
in a ‘Sea’ of Interconnects



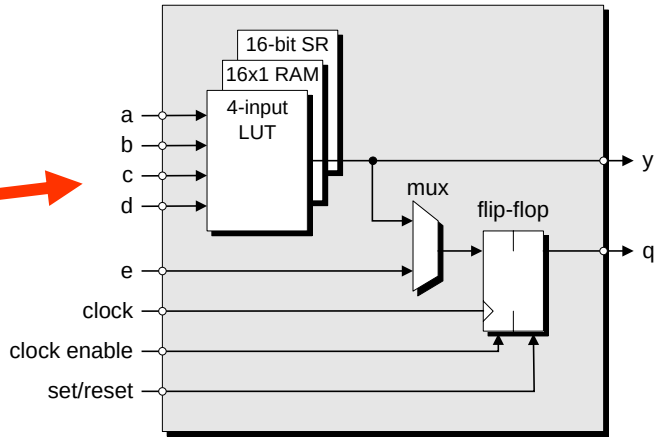
FPGA Architecture

Logic Blocks

- Logic Functions implemented in Lookup Table LUTs
- Multiplexers (select 1 of N inputs)
- Flip-Flops. Registers. Clocked Storage elements.



FPGA Fabric

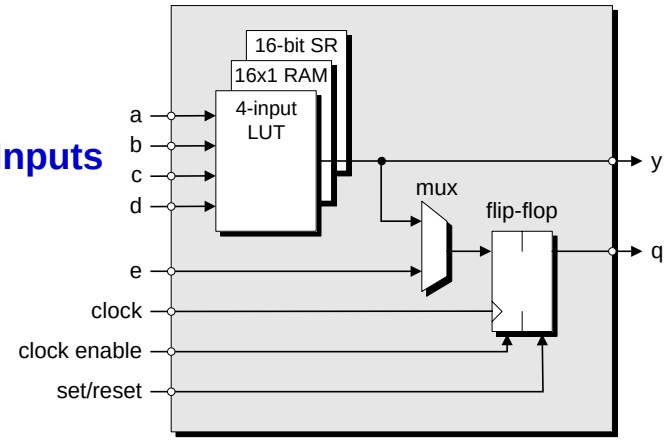


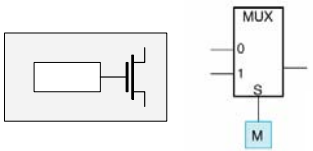
Logic Block

Lookup Tables LUTs

- LUT contains Memory Cells to implement small logic functions
- Each cell holds ‘0’ or ‘1’ .
- Programmed with outputs of Truth Table
- Inputs select content of one of the cells as output

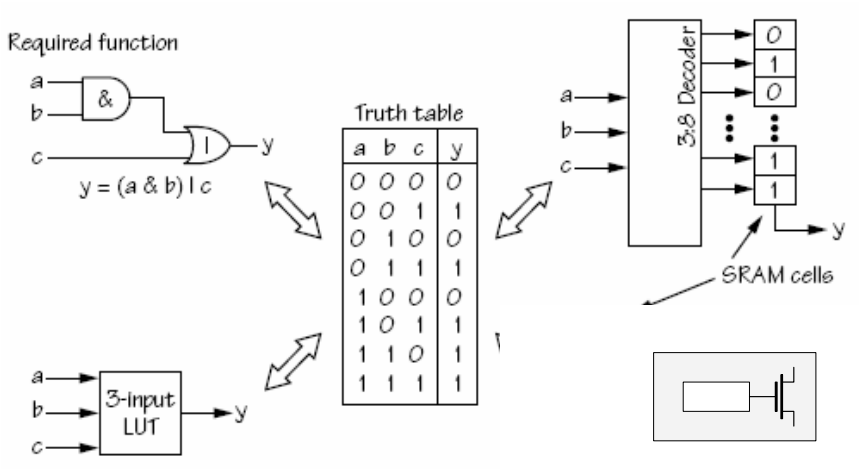
3 – 6 Inputs





Multiplexer MUX

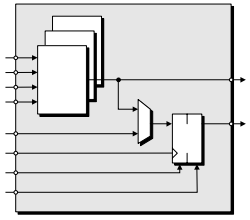
3 Inputs LUT -> 8 Memory Cells

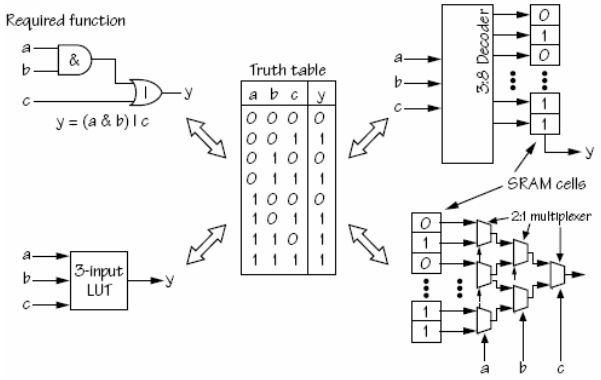


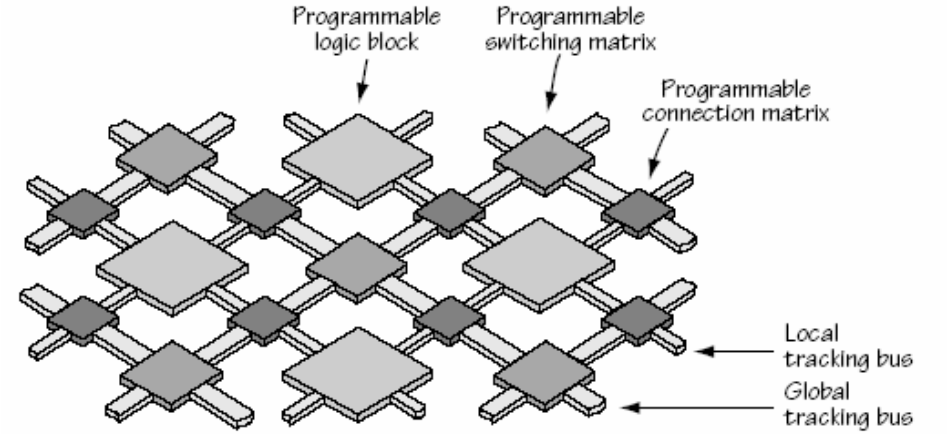
Static Random Access Memory SRAM cells

Logic Blocks

- Larger Logic Functions built up by connecting many Logic Blocks together







LUT

b

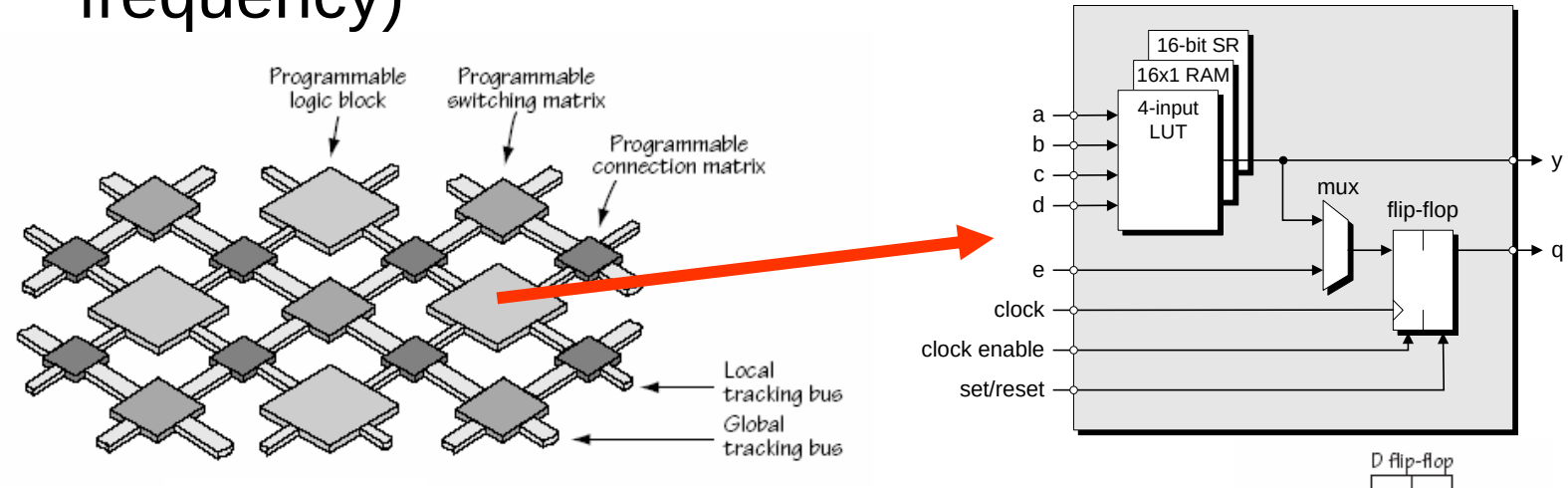
c

mux

y

Clocked Logic

- Flip Flops on outputs. CLOCKED storage elements.
- Sequential Logic Functions (cf Combinational Logic LUTs)
- Pipelines. Synchronous Logic Design
- FPGA Fabric driven by Global Clock (e.g. BX frequency)

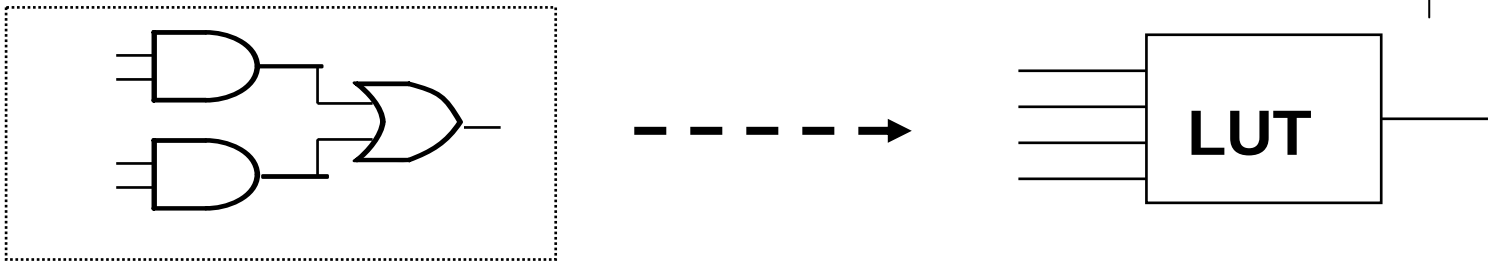


FPGA Fabric

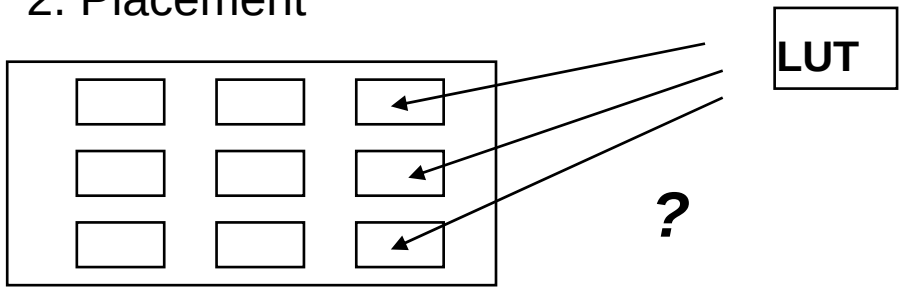
Clock

Circuit Compilation

1. Technology Mapping

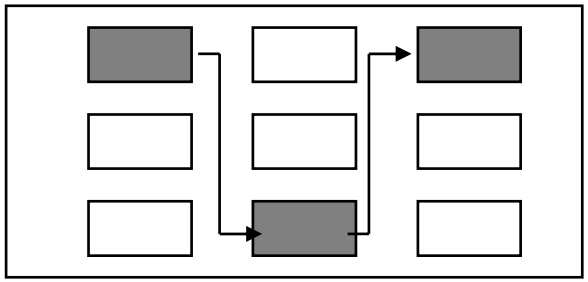


2. Placement



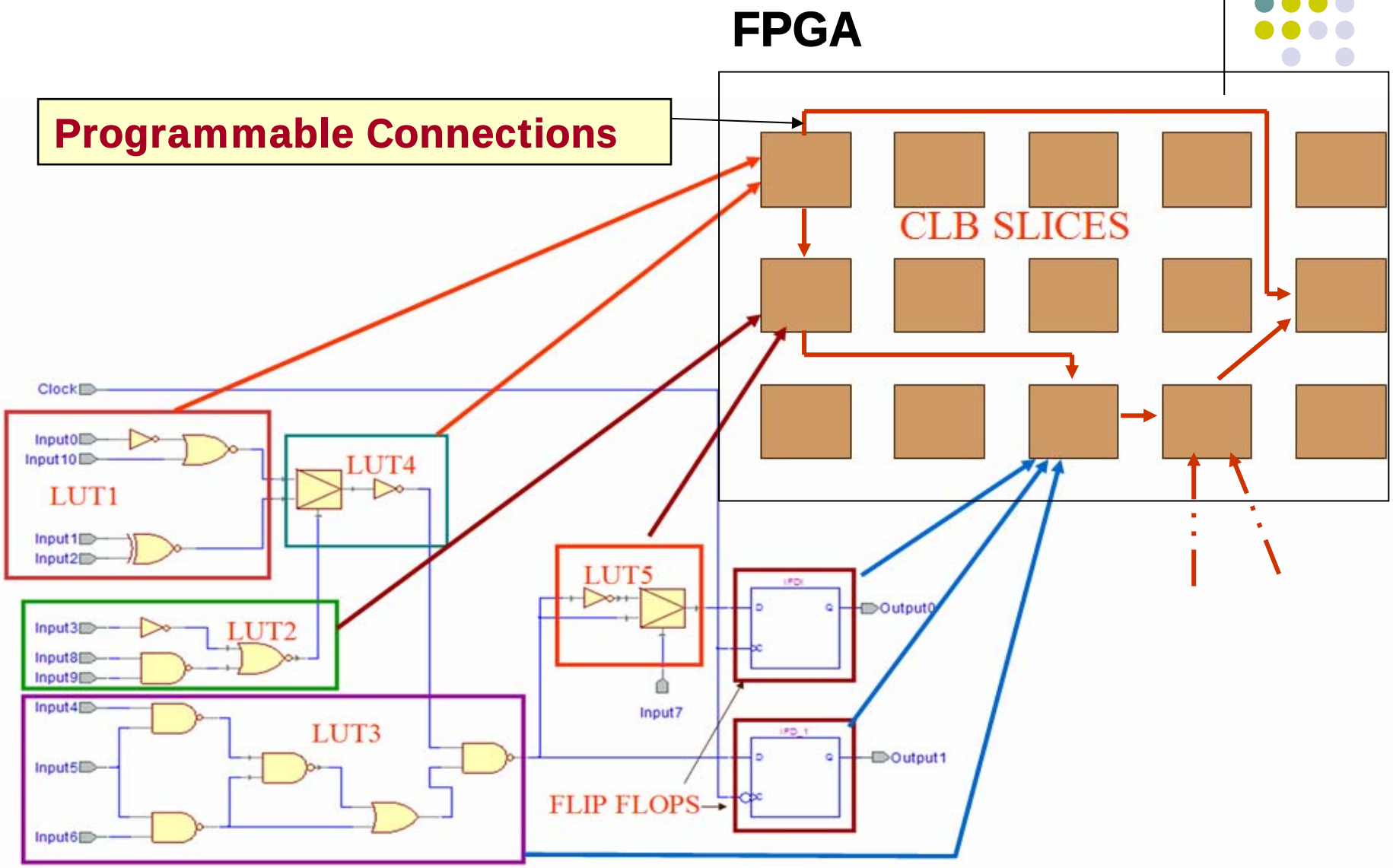
Assign a logical LUT to a physical location.

3. Routing

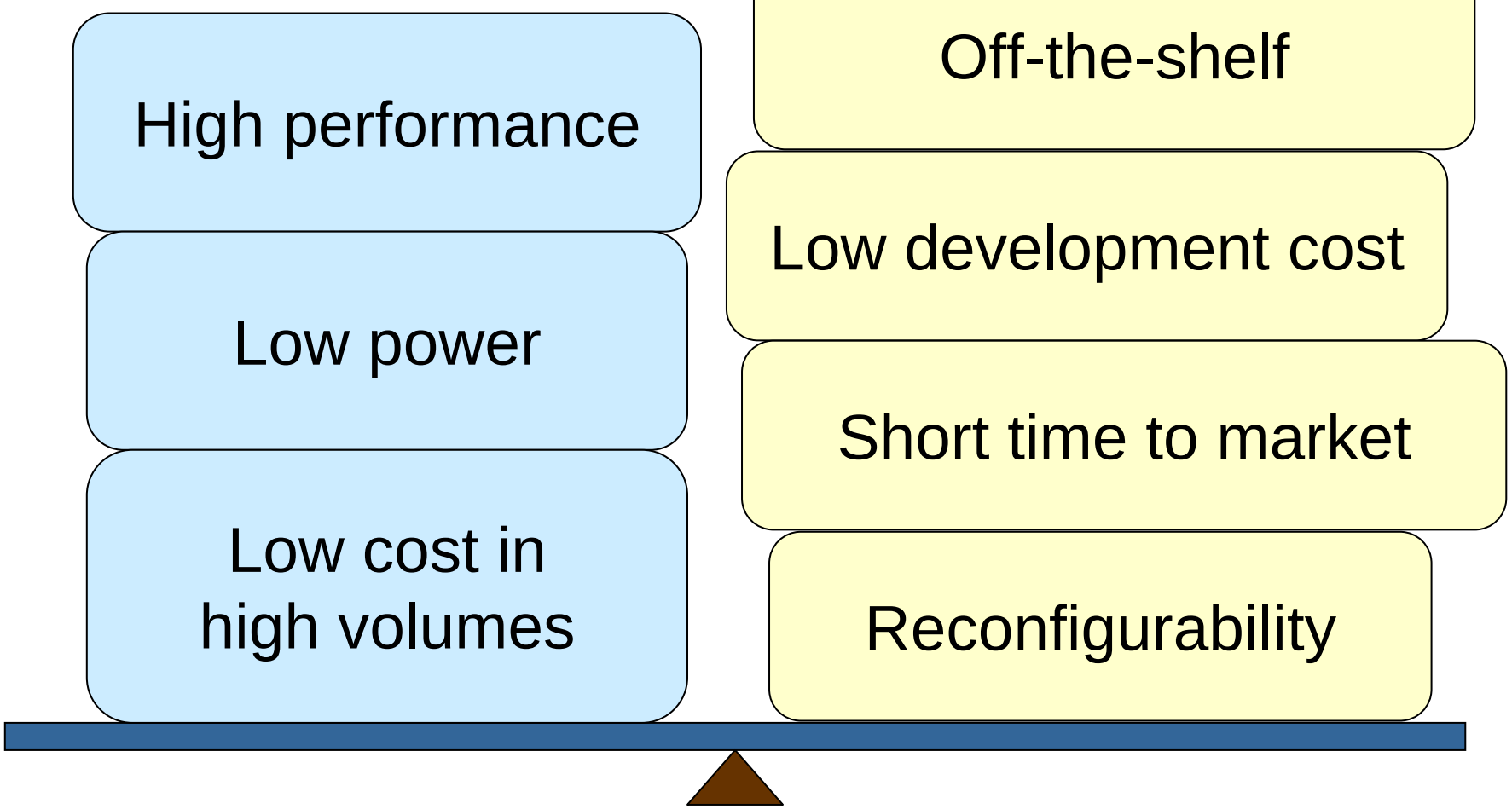


Select wire segments And switches for Interconnection.

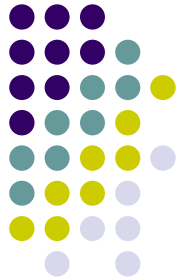
Routing Example



Which Way to Go?

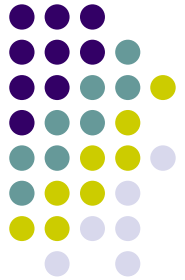


Other FPGA Advantages



- Manufacturing cycle for ASIC is very costly, lengthy and engages lots of manpower
  - Mistakes not detected at design time have large impact on development time and cost
  - FPGAs are perfect for rapid prototyping of digital circuits
- Easy upgrades like in case of software
- Unique applications
  - reconfigurable computing

Major FPGA Vendors



SRAM-based FPGAs

- **Xilinx, Inc.**
- **Altera Corp.**

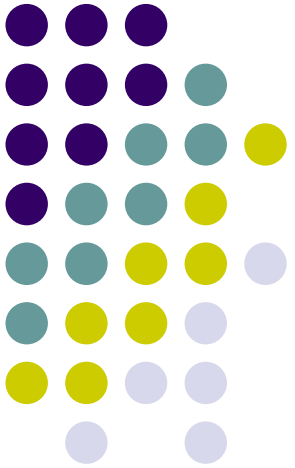
} **Share over 60% of the market**

- Atmel
- Lattice Semiconductor

Flash & antifuse FPGAs

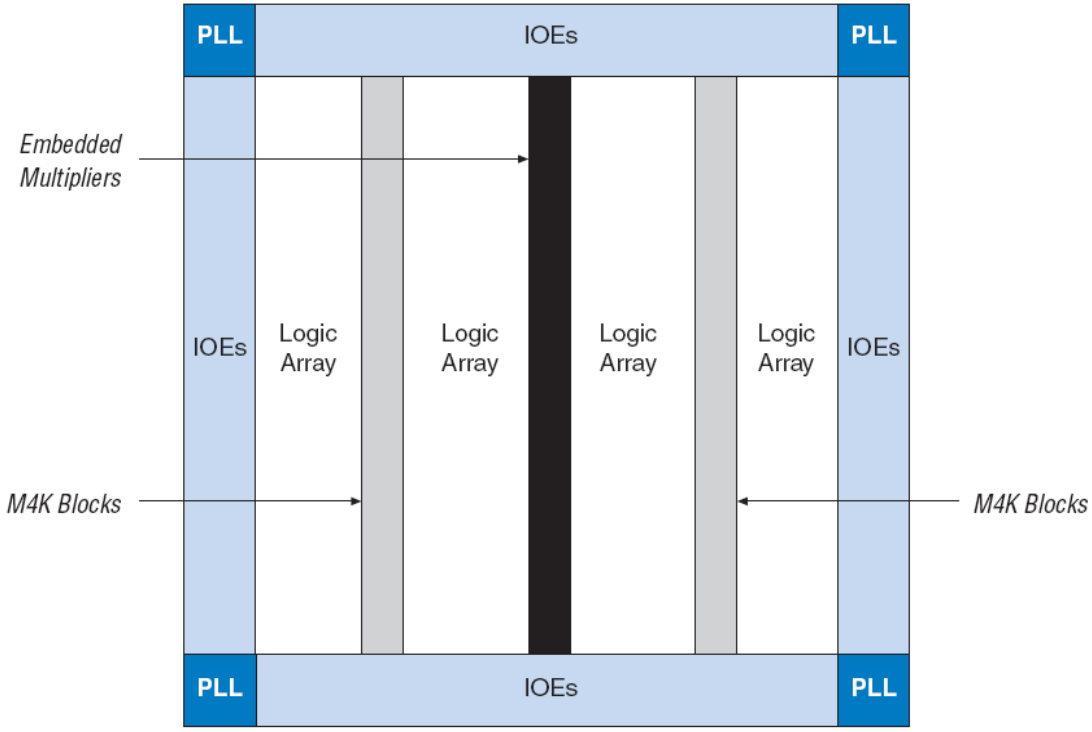
- Actel Corp.
- Quick Logic Corp.

FPGA Example – Altera Cyclone II

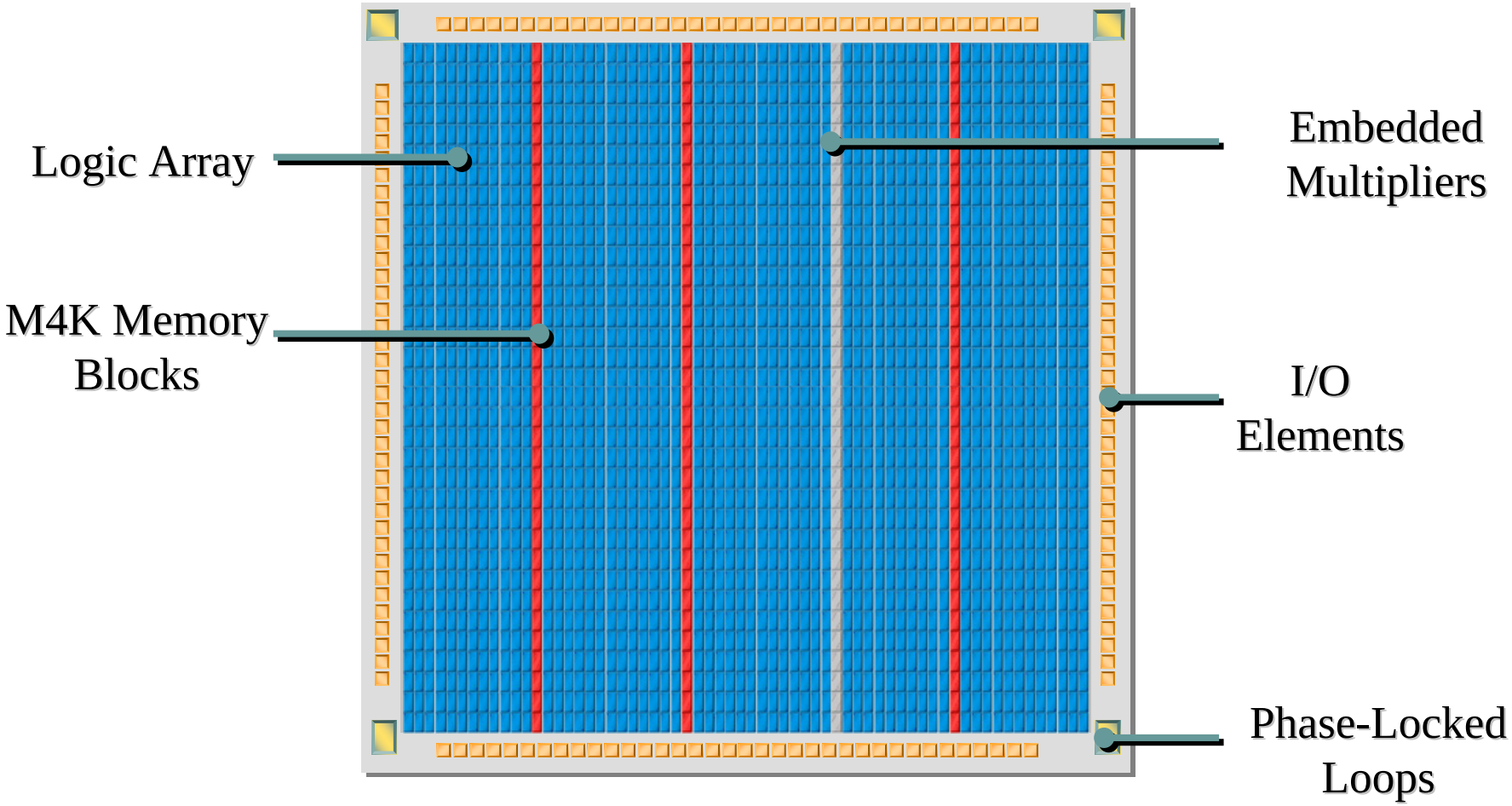


Cyclone II EP2C20 Block

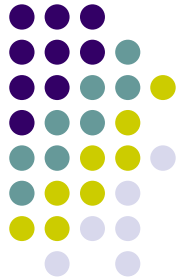
- Logic array – LUTs
- Block memory – M4K blocks
- Embedded Multipiers
- Input/output Modules (IOEs)
- PLLs



Cyclone II EP2C20 Block



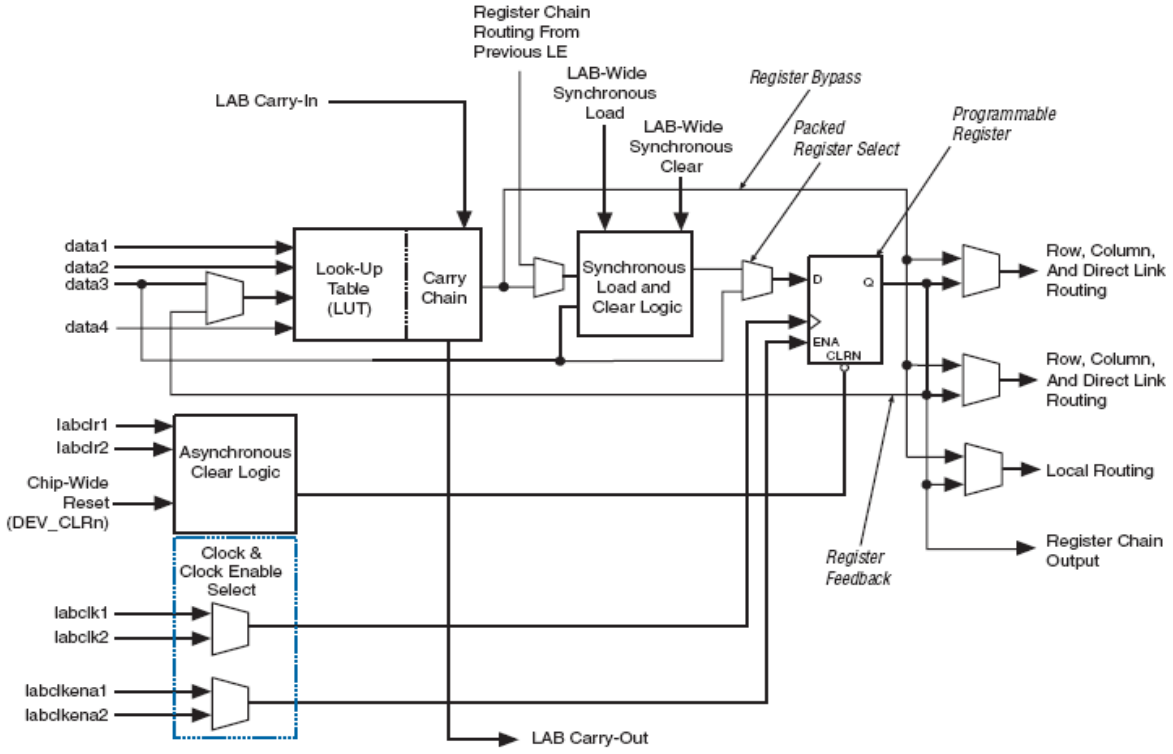
Cyclone II EP2C20



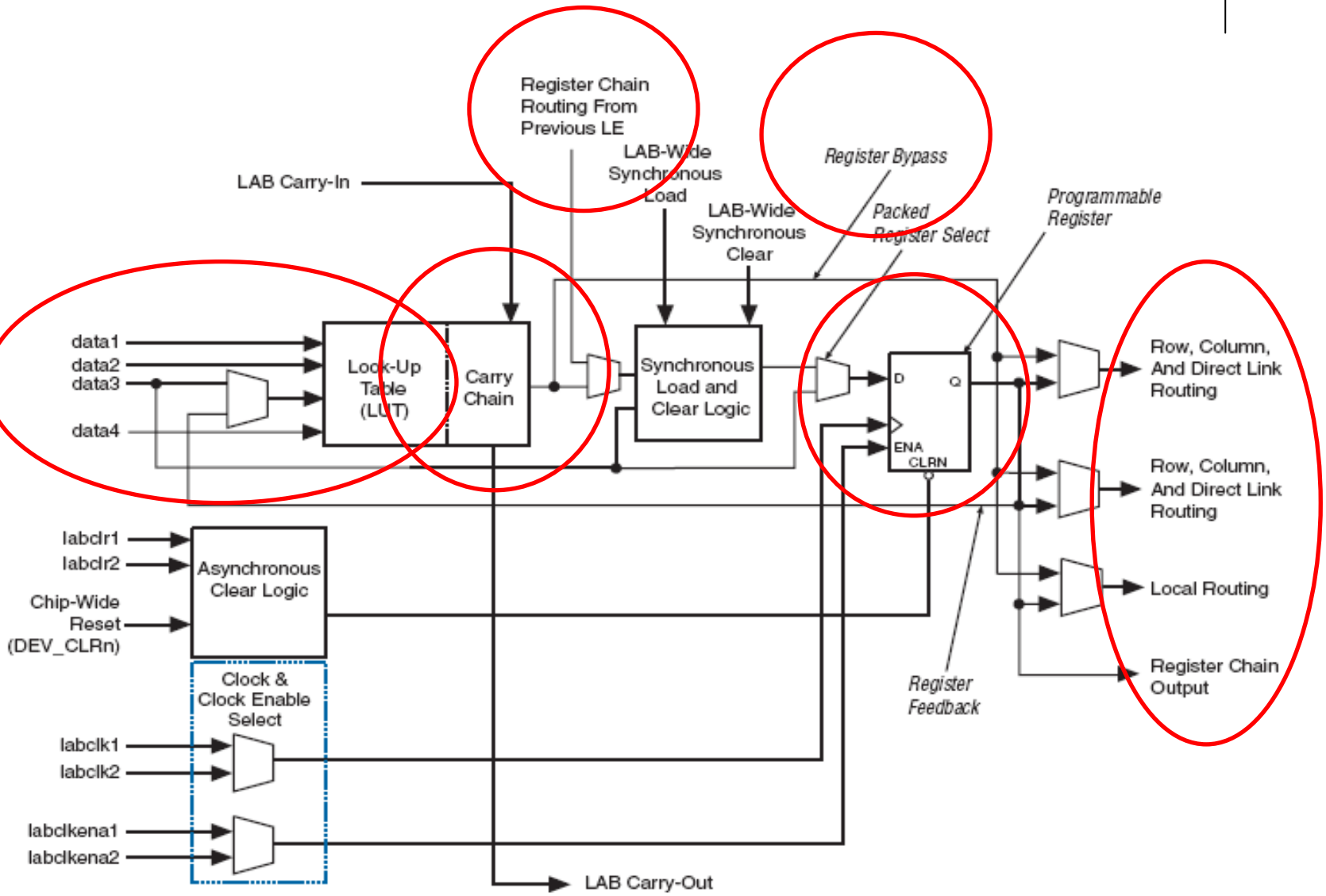
- 18,752 LEs
- 52 M4K RAM blocks
- 240K total RAM bits
- 52 9x9 embedded multipliers
- 4 PLLs
- 16 Clock networks
- 315 user I/O pins
- SRAM Based volatile configuration

Logic Element

- 16 LEs forms a Logic Array Block (LAB)
  - Normal mode
  - Arithmetic mode

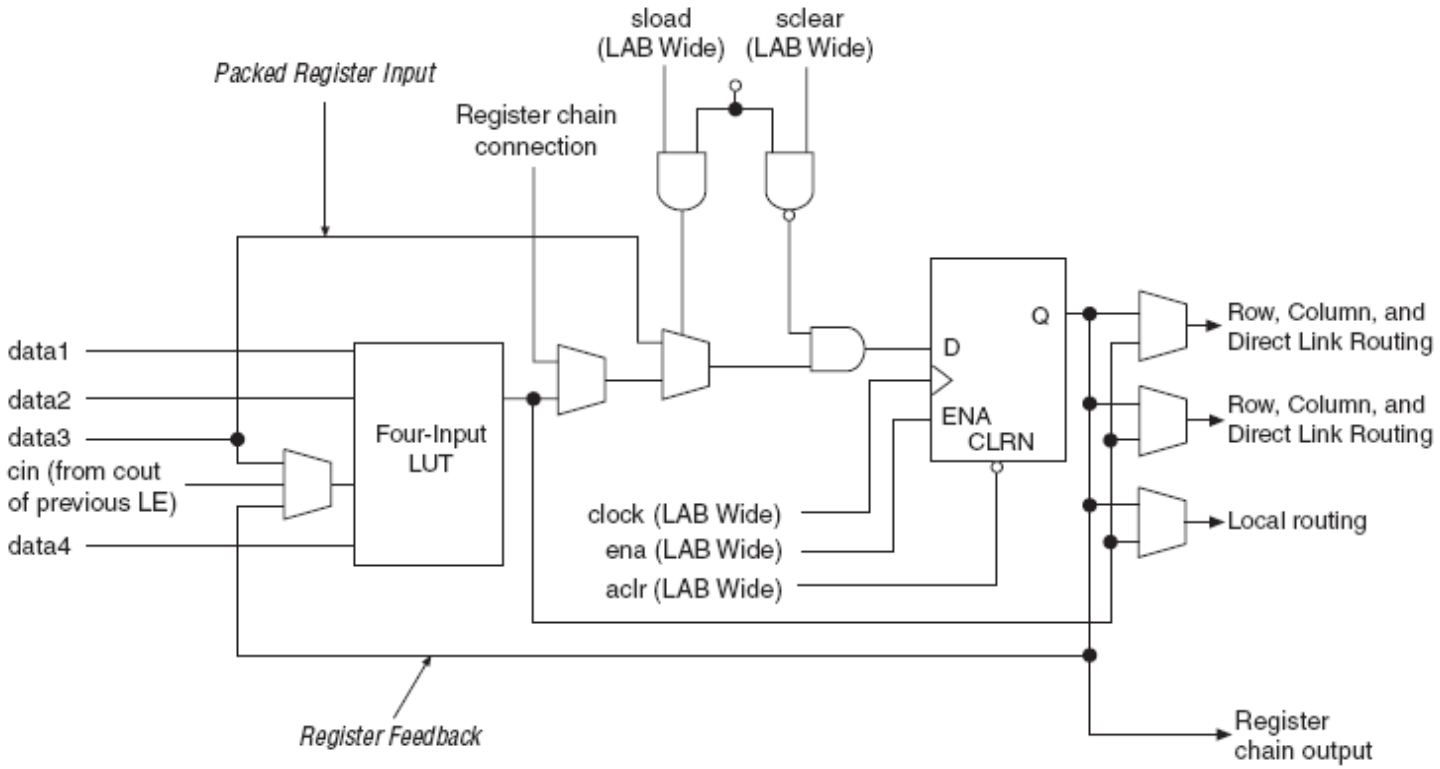


Logic Element



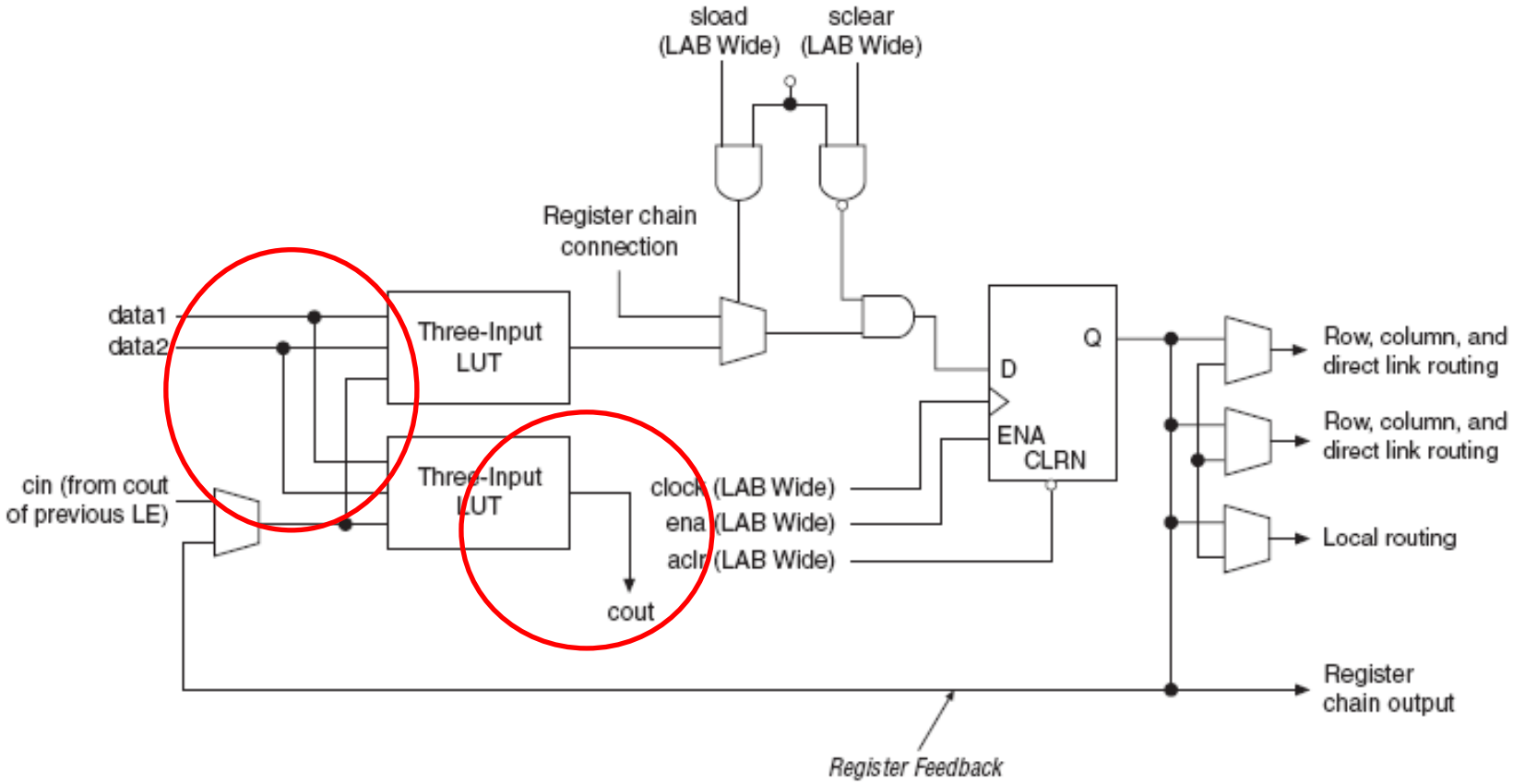
Logic Element

- Normal Mode – general logic operations

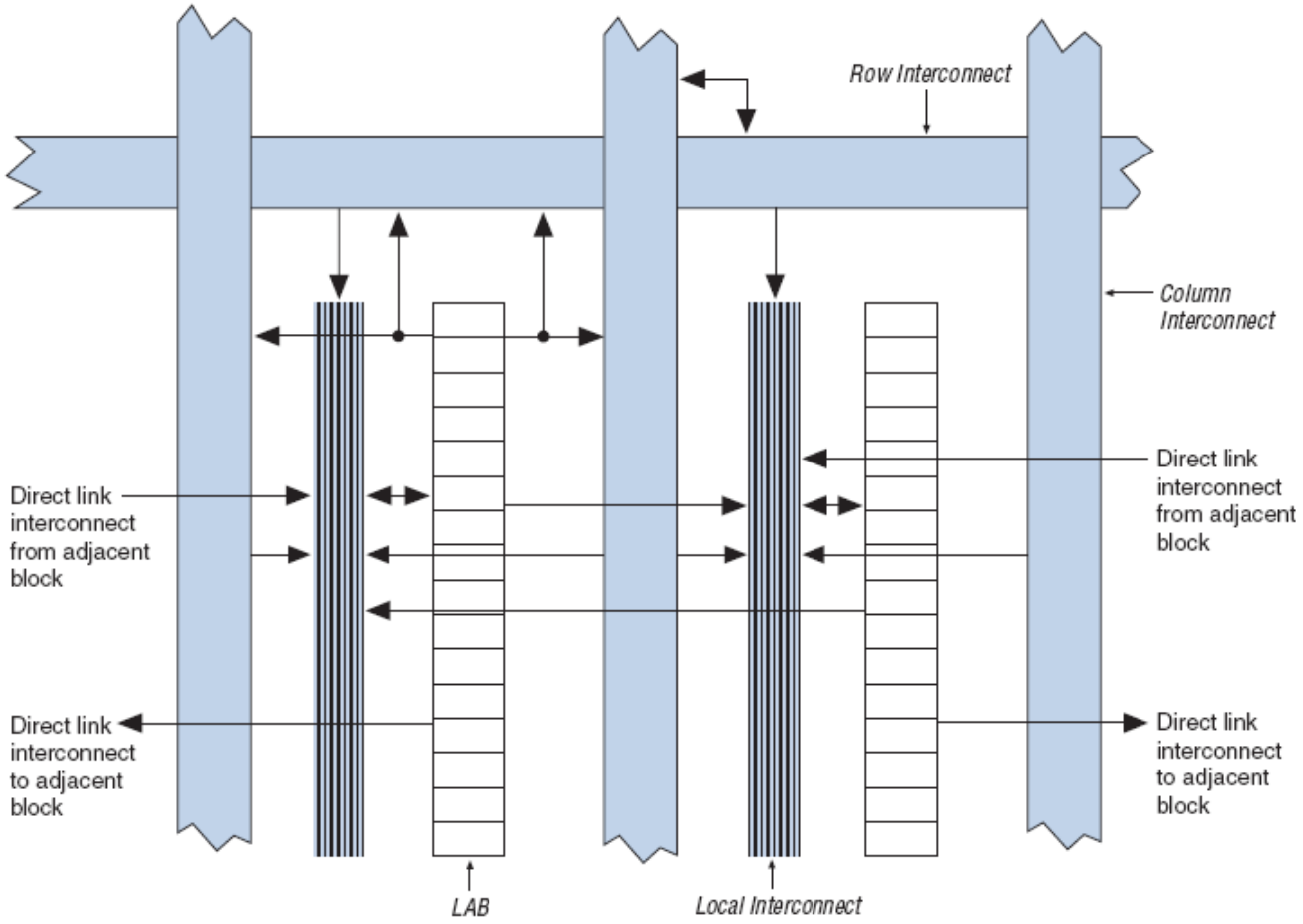


Logic Element

- Arithmetic Mode – adder, counter, accumulators, comparator

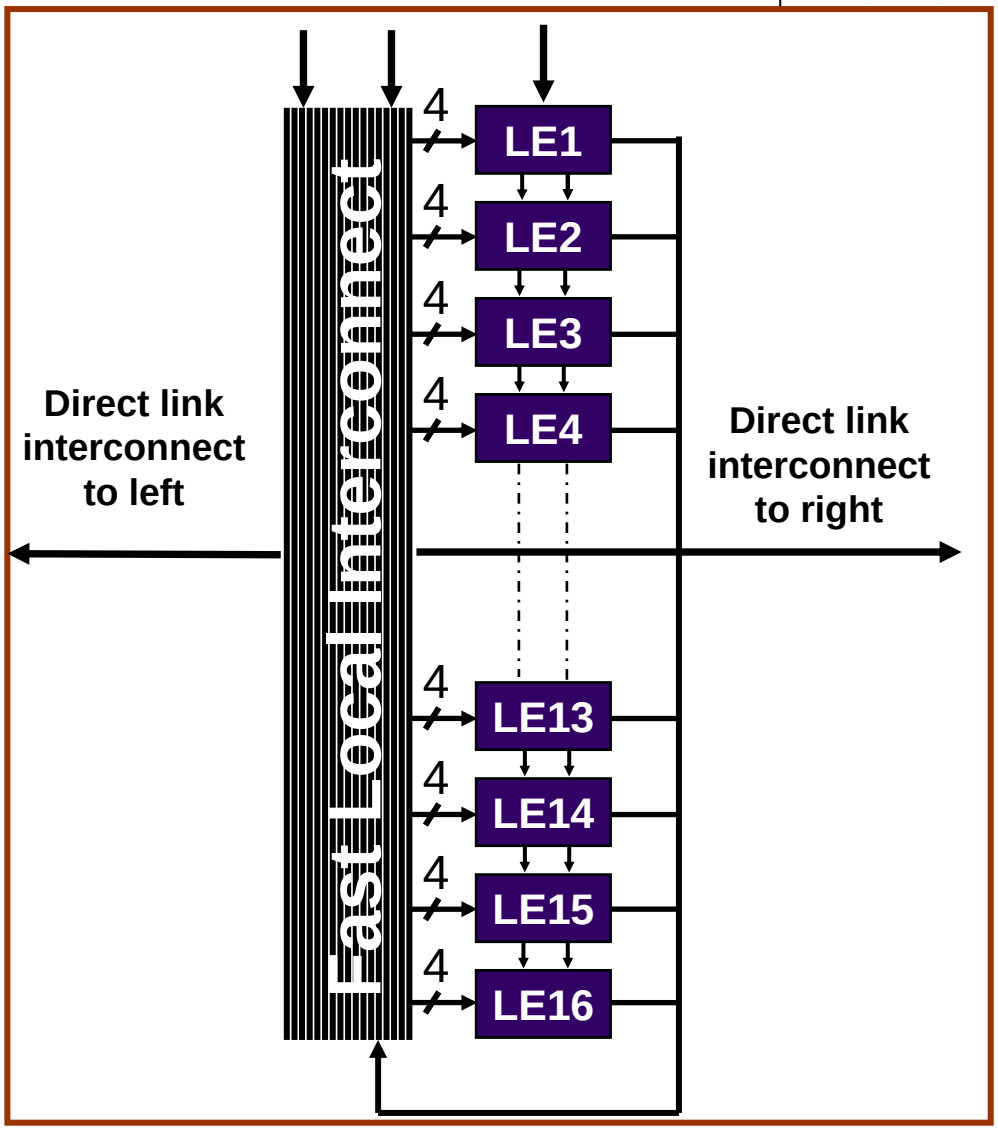


Logic Array Blocks Structure



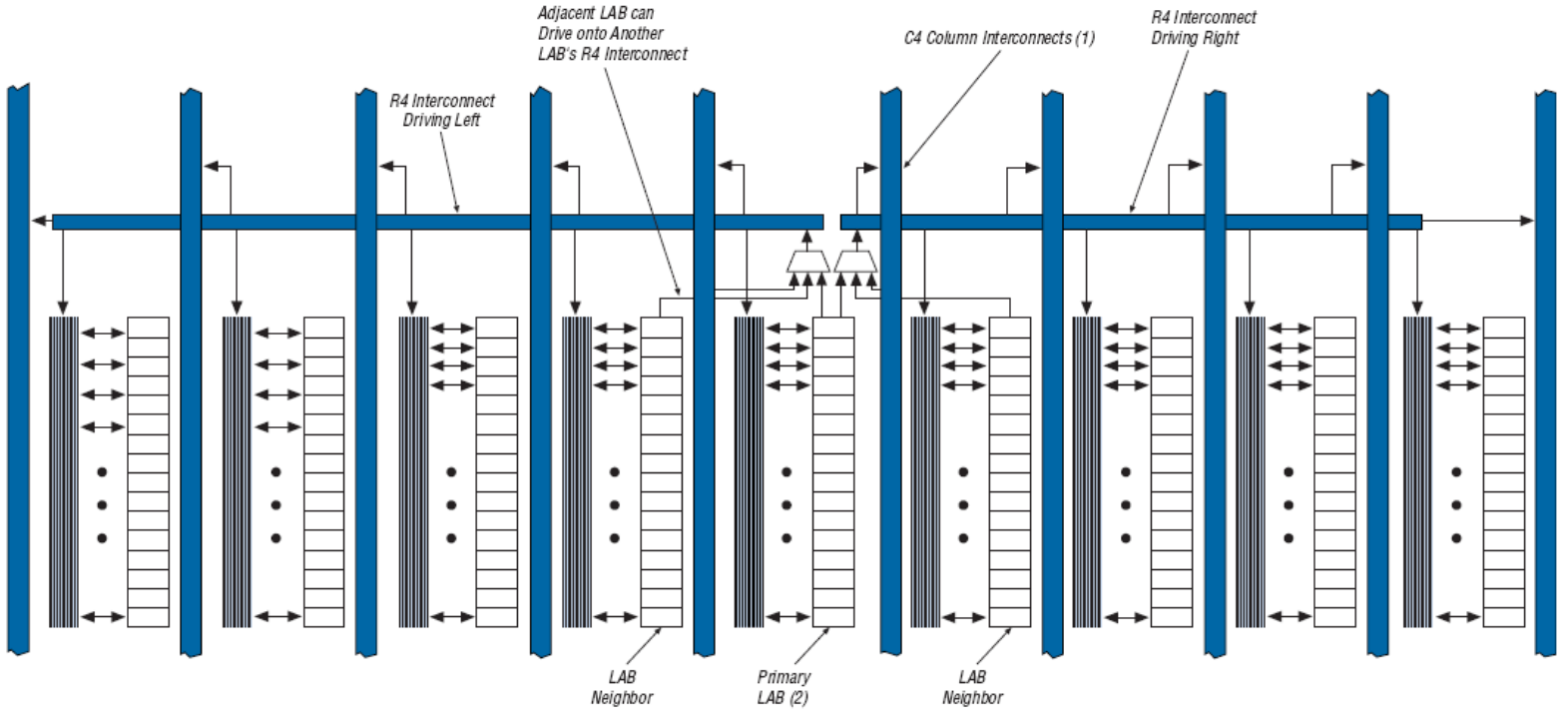
Cyclone II Logic Array Block (LAB)

- 16 LEs
- Local Interconnect
- LE carry chains
- Register chains



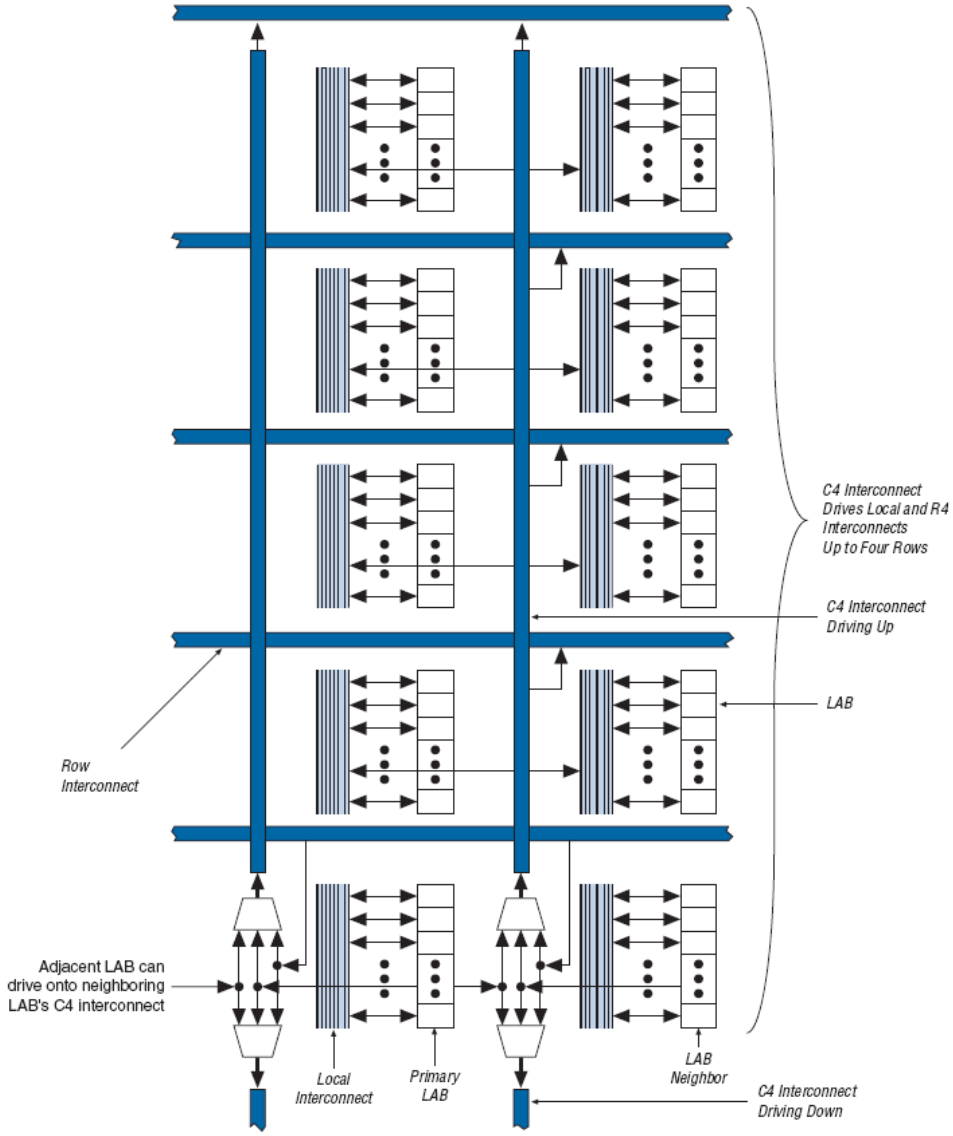
Row Interconnect Connections

- Direct link, R4, R24 interconnects



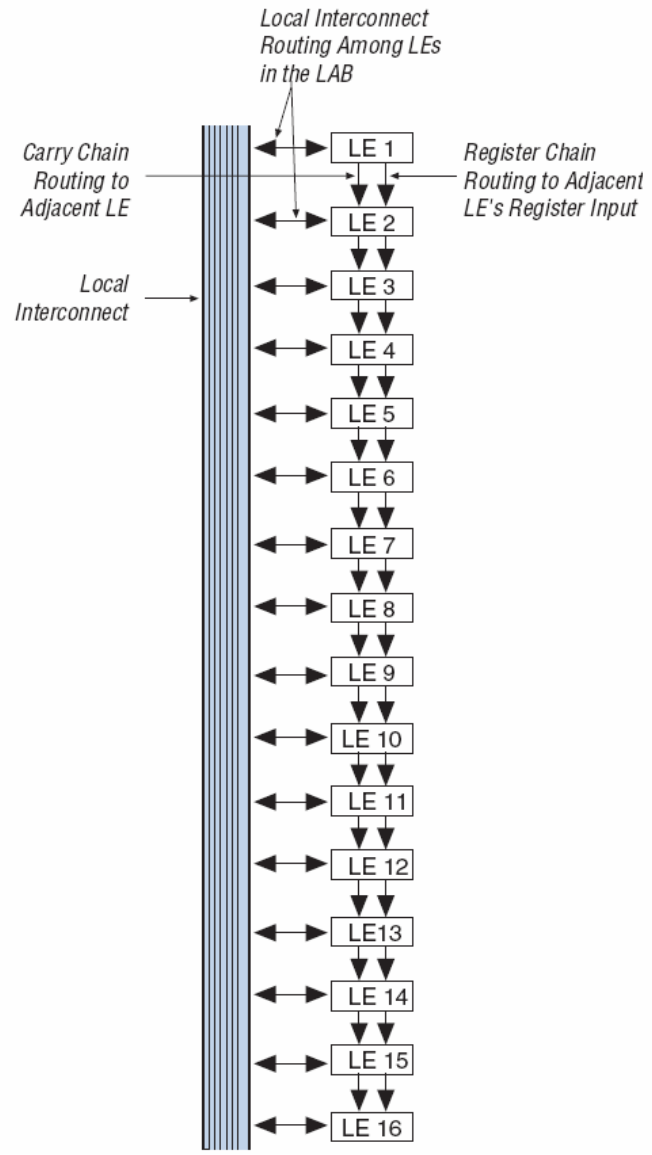
Column Interconnect Connections

- Register chain, C4, C16



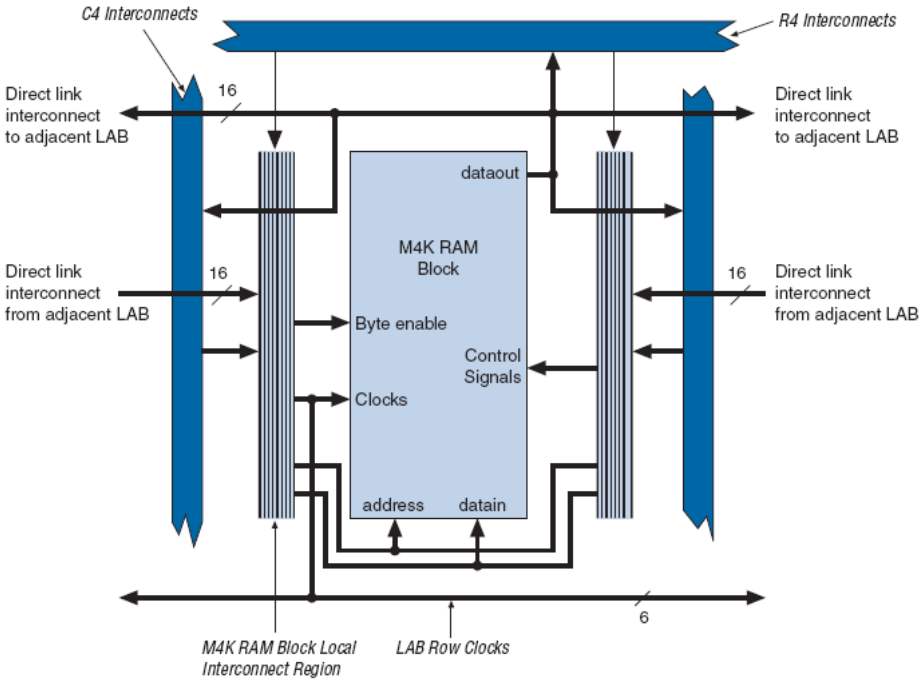
Register Chain Interconnects

- LEs can be connected for implementing fast adder, counters, shift register

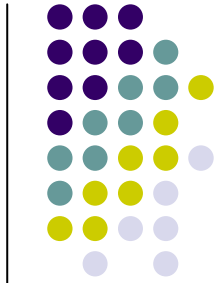


M4K RAM

Memory Mode	Description
Single-port memory	M4K blocks support single-port mode, used when simultaneous reads and writes are not required. Single-port memory supports non-simultaneous reads and writes.
Simple dual-port memory	Simple dual-port memory supports a simultaneous read and write.
Simple dual-port with mixed width	Simple dual-port memory mode with different read and write port widths.
True dual-port memory	True dual-port mode supports any combination of two-port operations: two reads, two writes, or one read and one write at two different clock frequencies.
True dual-port with mixed width	True dual-port mode with different read and write port widths.
Embedded shift register	M4K memory blocks are used to implement shift registers. Data is written into each address location at the falling edge of the clock and read from the address at the rising edge of the clock.
ROM	The M4K memory blocks support ROM mode. A MIF initializes the ROM contents of these blocks.
FIFO buffers	A single clock or dual clock FIFO may be implemented in the M4K blocks. Simultaneous read and write from an empty FIFO buffer is not supported.

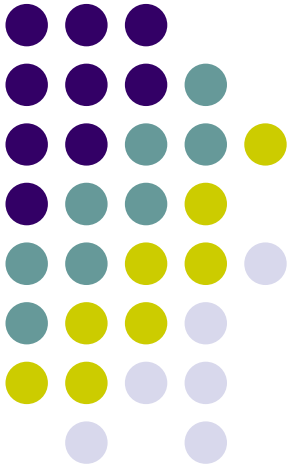


Cyclone II I/O Features

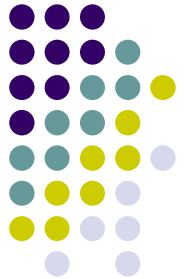


- In/Out/Tri-state
- Different Voltages and I/O Standards
  - PCI, PCI-X, LVDS I/O standard
- Flip-flop option
- Pull-up resistors
- DDR interface
- Series resistors
- Bus keeper
- Drive strength control
- Slew rate control
- Single ended/differential

Advance Architecture on Modern FPGAs

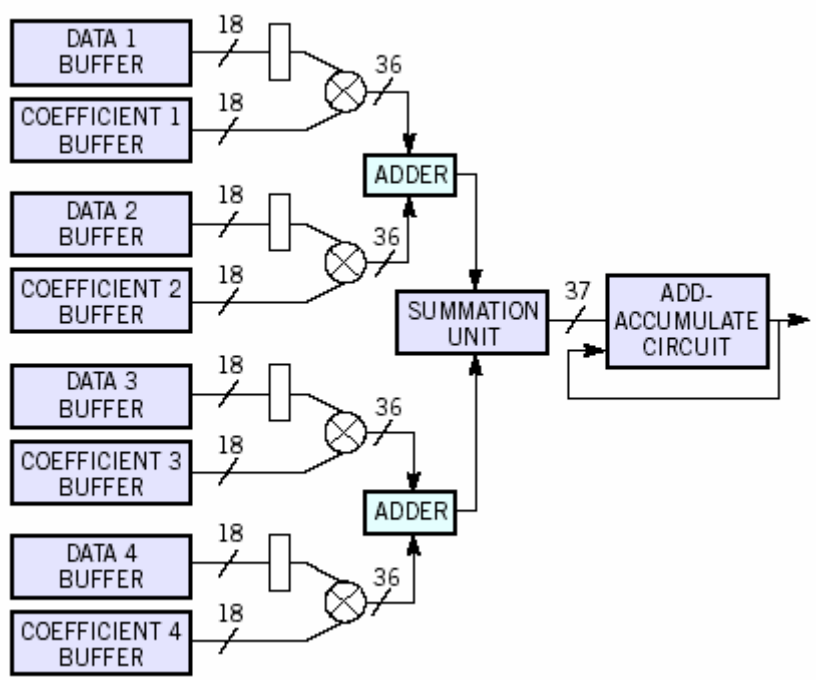


More Guts

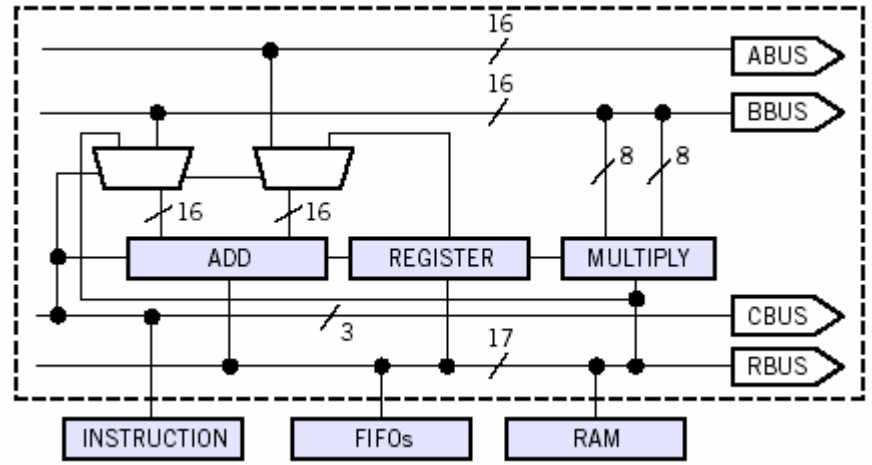


- Additional components
  - Dedicated computation units
  - Processor cores
  - DSP blocks

Dedicate Arithmetic Blocks



Altera

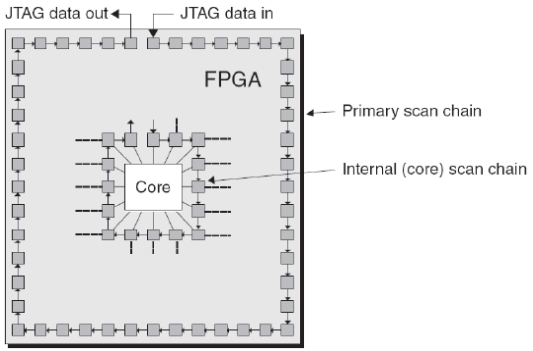


QuickLogic

Xilinx

Processor Cores

Features	Altera	Xilinx
Hard Processor	ARM9227 RISC (200MHz) Host Device: Excalibur	IBM PowerPC405 (300MHz) Host Device: Vertex II Pro
Soft Processor	Nios (32bits, 50MHz) Host Devices: Flex, APEX, ACEX, Mercury, Stratix	MicroBlaze (32bits, 150MHz) Host Devices: Spartan II, III, all Vertex families
Tools	Excalibur Solution Pack which includes GNUPro for SW design and Quartus II for HW design	Embedded Development Kit (EDK) which include WindRiver GNU compiler for SW design and ISE5.2i for HW design
Debuggers	SW debugger only	SW and HW (Chipscope Pro) debugger



Altera DE2-70