Introduction to FPGA

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Outline

- Introduction to PLD
- Introduction to FPGA
- FPGA Example – Altera Cyclone II
- Altera Quartus II
- Lab
World of Integrated Circuits

- Full-Custom ASICs
- Semi-Custom ASICs
- User Programmable
- PLD
- FPGA
Digital Logic

Digital Logic Function

3 Inputs

Black Box
Truth Table
SUM of PRODUCTS

Product AND (&) Sum OR (|)

Boolean Logic Minimisation

Connect Standard Logic Chips
Very Simple Glue Logic

FIXED Logic

Transistor Switches

CMOS NAND gate
Programmable Logic
Devices PLDs

- Different Types
- SUM of PRODUCTS
- Prefabricated
- Programmable Links
- Reconfigurable

Logic Function

\[ y = (a \land b \land c) \]
\[ x = (a \land b \land c) \lor (\overline{b} \land \overline{c}) \]
\[ w = (a \land c) \lor (\overline{b} \land \overline{c}) \]

Programmed PLD

Un-programmed State

Planes of ANDs, ORs

Sum of Products

Inputs

ANDs

OR

Programmable AND Array

Product Terms

Sums
How can we make a “programmable logic”?

- SRAM-based
  - Reconfigurable
  - Track latest SRAM technology
  - Volatile
  - Generally high power

- Anti-fuse technique
  - One-time programmable
  - Non-volatile – security app.
Complex PLDs

- CPLDs
- Programmable PLD Blocks
- Programmable Interconnects
- Electrically Erasable links

![CPLD Architecture](image)

Feedback Outputs
Field Programmable Gate Arrays FPGA

- Field Programmable Gate Array
  - New Architecture
  - ‘Simple’ Programmable Logic Blocks
  - Massive Fabric of Programmable Interconnects

Large Number of Logic Block ‘Islands’
1,000 … 100,000+
in a ‘Sea’ of Interconnects

FPGA Architecture
Logic Blocks

- Logic Functions implemented in Lookup Table LUTs
- Multiplexers (select 1 of N inputs)
Lookup Tables LUTs

- LUT contains Memory Cells to implement small logic functions
- Each cell holds ‘0’ or ‘1’.
- Programmed with outputs of Truth Table
- Inputs select content of one of the cells as output

3 Inputs LUT -> 8 Memory Cells

3 – 6 Inputs

Static Random Access Memory SRAM cells

4-input LUT

Required function

Truth Table

5-input LUT

Multiplexer MUX

3:8 Decoder

16-bit SR
Logic Blocks

- Larger Logic Functions built up by connecting many Logic Blocks together
Clocked Logic

- Flip Flops on outputs. CLOCKED storage elements.
- Sequential Logic Functions (cf Combinational Logic LUTs)
- Pipelines. Synchronous Logic Design
- FPGA Fabric driven by Global Clock (e.g. BX frequency)
Circuit Compilation

1. Technology Mapping

Assign a logical LUT to a physical location.

2. Placement

Select wire segments
And switches for Interconnection.
Routing Example

Programmable Connections
Which Way to Go?

**ASICS**
- High performance
- Low power
- Low cost in high volumes

**FPGAs**
- Off-the-shelf
- Low development cost
- Short time to market
- Reconfigurability

Low power

Low cost in high volumes

Reconfigurability

Short time to market

Low development cost

Off-the-shelf

High performance
Other FPGA Advantages

- Manufacturing cycle for ASIC is very costly, lengthy and engages lots of manpower
  - Mistakes not detected at design time have large impact on development time and cost
  - FPGAs are perfect for rapid prototyping of digital circuits
- Easy upgrades like in case of software
- Unique applications
  - reconfigurable computing
Major FPGA Vendors

SRAM-based FPGAs
- Xilinx, Inc.
- Altera Corp.
- Atmel
- Lattice Semiconductor

Share over 60% of the market

Flash & antifuse FPGAs
- Actel Corp.
- Quick Logic Corp.
FPGA Example –
Altera Cyclone II
Cyclone II EP2C20 Block

- Logic array – LUTs
- Block memory – M4K blocks
- Embedded Multipiers
- Input/output Modules (IOEs)
- PLLs
Cyclone II EP2C20 Block

- Logic Array
- M4K Memory Blocks
- Embedded Multipliers
- I/O Elements
- Phase-Locked Loops
Cyclone II EP2C20

- 18,752 LEs
- 52 M4K RAM blocks
- 240K total RAM bits
- 52 9x9 embedded multipliers
- 4 PLLs
- 16 Clock networks
- 315 user I/O pins
- SRAM Based volatile configuration
Logic Element

- 16 LEs forms a Logic Array Block (LAB)
  - Normal mode
  - Arithmetic mode
Logic Element

LAB Carry-In

Register Chain Routing From Previous LE
LAB-Wide Synchronous Load
LAB-Wide Synchronous Clear

Register Bypass
Packed Register Select

Programmable Register

Row, Column, And Direct Link Routing

Row, Column, And Direct Link Routing

Local Routing

Register Chain Output

D Q

Row, Column, And Direct Link Routing

LAB Carry-Out

Clock & Clock Enable Select

Asynchronous Clear Logic

Chip-Wide Reset (DEV_CLRn)

labclk1
labclk2
labclkena1
labclkena2

labclrl
labclrl2
Logic Element

- Normal Mode – general logic operations
Logic Element

- Arithmetic Mode – adder, counter, accumulators, comparator
Logic Array Blocks Structure
Cyclone II Logic Array Block (LAB)

- 16 LEs
- Local Interconnect
- LE carry chains
- Register chains
Row Interconnect Connections

- Direct link, R4, R24 interconnects
Column Interconnect Connections

- Register chain, C4, C16
Register Chain Interconnects

- LEs can be connected for implementing fast adder, counters, shift register
# M4K RAM

<table>
<thead>
<tr>
<th>Memory Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single-port memory</td>
<td>M4K blocks support single-port mode, used when simultaneous reads and writes are not required. Single-port memory supports non-simultaneous reads and writes.</td>
</tr>
<tr>
<td>Simple dual-port memory</td>
<td>Simple dual-port memory supports a simultaneous read and write.</td>
</tr>
<tr>
<td>Simple dual-port with mixed width</td>
<td>Simple dual-port memory mode with different read and write port widths.</td>
</tr>
<tr>
<td>True dual-port memory</td>
<td>True dual-port mode supports any combination of two-port operations: two reads, two writes, or one read and one write at two different clock frequencies.</td>
</tr>
<tr>
<td>True dual-port with mixed width</td>
<td>True dual-port mode with different read and write port widths.</td>
</tr>
<tr>
<td>Embedded shift register</td>
<td>M4K memory blocks are used to implement shift registers. Data is written into each address location at the falling edge of the clock and read from the address at the rising edge of the clock.</td>
</tr>
<tr>
<td>ROM</td>
<td>The M4K memory blocks support ROM mode. A MIF initializes the ROM contents of these blocks.</td>
</tr>
<tr>
<td>FIFO buffers</td>
<td>A single clock or dual clock FIFO may be implemented in the M4K blocks. Simultaneous read and write from an empty FIFO buffer is not supported.</td>
</tr>
</tbody>
</table>
Cyclone II I/O Features

- In/Out/Tri-state
- Different Voltages and I/O Standards
  - PCI, PCI-X, LVDS I/O standard
- Flip-flop option
- Pull-up resistors
- DDR interface
- Series resistors
- Bus keeper
- Drive strength control
- Slew rate control
- Single ended/differential
Advance Architecture on Modern FPGAs
More Guts

- Additional components
  - Dedicated computation units
  - Processor cores
  - DSP blocks
Dedicate Arithmetic Blocks

Altera

Xilinx

QuickLogic

Xilinx
## Processor Cores

<table>
<thead>
<tr>
<th>Features</th>
<th>Altera</th>
<th>Xilinx</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hard Processor</td>
<td>ARM9227 RISC (200MHz)</td>
<td>IBM PowerPC405 (300MHz)</td>
</tr>
<tr>
<td></td>
<td>Host Device: Excalibur</td>
<td>Host Device: Vertex II Pro</td>
</tr>
<tr>
<td>Soft Processor</td>
<td>Nios (32bits, 50MHz)</td>
<td>MicroBlaze (32bits, 150MHz)</td>
</tr>
<tr>
<td></td>
<td>Host Devices: Flex, APEX,</td>
<td>Host Devices: Spartan II, III, all Vertex families</td>
</tr>
<tr>
<td></td>
<td>ACEX, Mercury, Stratix</td>
<td></td>
</tr>
<tr>
<td>Tools</td>
<td>Excalibur Solution Pack which includes GNUPro for SW design and Quartus II for HW design</td>
<td>Embedded Development Kit (EDK) which include WindRiver GNU compiler for SW design and ISE5.2i for HW design</td>
</tr>
<tr>
<td>Debuggers</td>
<td>SW debugger only</td>
<td>SW and HW (Chipscope Pro) debugger</td>
</tr>
</tbody>
</table>
Altera DE2-70