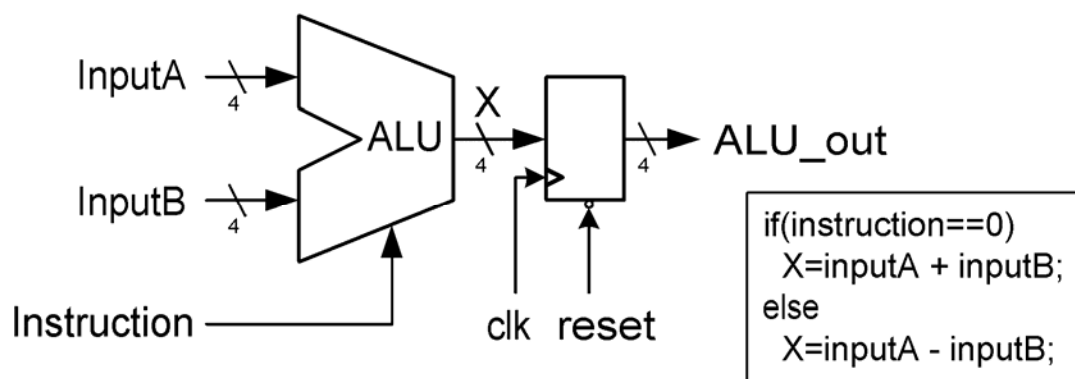


Computer-Aided VLSI System Design, Fall 2011

Verilog Lab 1: 4-Bit ALU with 2 Instructions

I. 4-Bit ALU with 2 Instructions:



II. Objectives:

In this lab, you will learn:

1. A synthesizable Verilog HDL code and the corresponding test bench.
2. How to run NC-Verilog simulator?

III. Environment Setup:

1. Source the default *cshrc* file:

```
source /usr/cadence/cshrc
```

IV. Lab Files:

1. Lab files are in `~cvsd/11F/Verilog/Lab1.tar`
2. Extract `Lab1.tar` in your working directory with command

```
tar -xvf Lab1.tar
```
3. Lab1 files are shown as below:

Filename	Description
<i>Lab1_alu.v</i>	RTL code for this ALU
<i>Lab1_test_alu.v</i>	Test bench for this ALU
<i>Lab1_alu_run.f</i>	Command-line file
<i>Lab1_test_alu_file.v</i>	Test bench with file I/O
<i>program.txt</i>	Input stimulus
<i>program_out.txt</i>	Correct answers

- Your *ALU* module looks like this

```

module ALU(alu_out,instruction,inputA,inputB,clk,reset);
output [3:0] alu_out;
input [3:0] inputA,inputB;
input instruction;
input clk,reset;

...

endmodule

```

V. Module Description:

This RTL describes a simple ALU with two 4-bit input signals and 2 instructions. One instruction is summation, and the other one is subtraction.

VI. Check Verilog Code by NC-Verilog:

- Type this command


```
ncverilog Lab1_alu.v
```
- NC-Verilog will report one error because the signal X is not declared. **Please help to add the declaration for the file *Lab1_alu.v*.**
- Run the command in step 1 again. No error should occur now.

VII. Run simulation with a test bench by NC-Verilog:

- Type this command


```
ncverilog Lab1_test_alu.v Lab1_alu.v
```
- 224 errors are found after simulation. Please read the file *alu_out.txt* to find out what happens. **Please modify the file *Lab1_alu.v* to fix these errors.**
- Run the command in step 1 again. The simulation result is correct now.
- Instead of the command in step 1, you can also use the command-line file to run simulation by typing this command.


```
ncverilog -f Lab1_alu_run.f
```

VIII. Run simulation with file I/O:

- Using the test bench *Lab1_test_alu_file.v* for simulation. Can you find out how this test bench works with file I/O?

```

$readmemb("program.txt",program); // Input stimulus
$readmemb("program_out.txt",answer); // Correct answers

```

IX. Checkpoints:

Please check with TAs before leaving this lab to make sure the following goals are accomplished and to get credits.

1. Please fix the declaration error in Section VI.
2. Please fix the simulation errors in Section VII.

END of LAB

Creator:

1st Edition: Chao-Tsung Huang, 2002

2nd Edition: Yu-Lin Chang, 2004

3rd Edition: Yu-Lin Chang, 2005

4th Edition: En-Jui Chang, 2010

5th Edition: En-Jui Chang, 2011