Computer-Aided VLSI System Design
TetraMAX® Lab: Automatic Test Pattern Generation (ATPG)

Objectives:

In this lab, you will learn:

How to generate single stuck-at fault test patterns for our simple ALU

Download Files from ~cvsd/CUR/Testing/ATPG

1. Create a work directory and copy the lab files into it
2. check if you have these files:

Filename	Description
ALU_syn_dft.v	Scan-ready gate level netlist for the simple ALU
ALU_syn_dft.spf	STIL format test protocol file (generated by DFT Compiler)
atpg.tcl	Reference script in this lab

3. Check the contents of these files.

Invoke Tetramax

To invoke Tetramax, first include the following C shell script

source /usr/cad/synopsys/CIC/tmax.csh

And then, you can do either one

tmax -nogui (command mode)

tmax & (GUI mode)

In this Lab, we will use the command mode. You are welcome to try the GUI mode. In the GUI mode, you can type in your commands in the command line, located at the bottom of the window.

STEP 1: Read Input Files

Read in your design and cell library

read_netlist ALU_syn_dft.v

Read in cell library in Verilog format

read_netlist <your library path>/tsmc13.v

NOTE: unlike the design compiler, Tetramax does not take the library in .ddc format. Instead, Tetramax reads library in Verilog format.

The location of tsmc13.v is at:

/home/raid2_2/course/cvsd/CBDK_IC_Contest/CIC/Verilog/tsmc13.v

STEP 2: Build Model

1. This step builds a model of your design for ATPG.

   run build_model ALU

   Question: How many violations do you see? _____

2. To probe further for the violations, type

   report violations -all

   Examine these violations,

   Question: What causes these violations? _____

NOTE: You may see some warning messages. Should you ignore these warning messages? Try to explain these warning messages.

STEP 3: Run DRC

The spf file tells the ATPG how to operate the circuit in test mode.
This step run design rule checking. Please type,

run drc ALU_syn_dft.spf

Question: Does our design pass all rules? _____

STEP 4: Set fault list

Specify the fault model. We use stuck-at fault model in this lab.

set faults -model stuck

Inject all faults into the circuit under test

add faults -all

STEP 5: Run ATPG

To obtain the maximum test coverage while minimizing the number of patterns, we can set the ATPG options as follows.
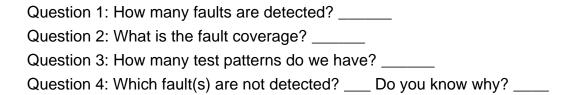
set_atpg -abort_limit 100 -merge high

run_atpg -auto_compression

Question: How many total faults do we have? _____

STEP 5 Review Results

To get a summary of your ATPG results, type

report_summaries

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Question 1: How many faults are detected? _____

Question 2: What is the fault coverage? _____

Question 3: How many test patterns do we have? _____

Question 4: Which fault(s) are not detected? ___ Do you know why? ____

The default test coverage is obtained by using uncollapsed fault list.   To use the collapsed fault list, type

set_faults -report collapsed

report_summaries

TetraMAX ATPG defines test coverage and fault coverage as follows:

$$\text{Test Coverage} = \frac{DT + (PT \times PT\_credit)}{All\_Faults - UD - (AN \times AU\_credit)} \times 100$$

$$\text{Fault Coverage} = \frac{DT + (PT \times PT\_credit)}{All\_Faults} \times 100$$

To display fault coverage in addition to test coverage with the summary report type

set_faults -fault_coverage

report_summaries

STEP 7 Save Patterns

To see your test patterns, type

report patterns -all

Save your patterns into files. There are many formats supported by TetraMAX.   WGL (Waveform Generation Language), and STIL (Standard Test Interface Language) are two of the popular formats. Depends on the test equipment you use, you can choose other different formats.

write_patterns ALU_syn_ATPG.wgl -format WGL

write_patterns ALU_syn_ATPG.stil -format STIL

Although ATPG should give us "correct" patterns, it is always good to verify the patterns. Save patterns in Verilog format so that you can verify your patterns using Verilog simulator.

write_patterns ALU_syn_ATPG_tb.v -format verilog

Question: How many files do you get by typing the last command? _____

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Try to run Verilog simulations and see if you get correct results.

Checkpoints:

Please check with TAs before leaving this lab to make sure the following goals are accomplished and to get credits.

1. Show your ATPG results.
2. Answer the questions in this lab.

END of LAB

Creator:

1st Edition: Chien-Mo Li, 2001

2nd Edition: Yu-Lin Chang, 2004

3rd Edition: Jui-Hsin Lai(Larry), 2008

4th Edition: Bing-Chuan Bai, 2010

5th Edition: Bing-Chuan Bai, 2011