Computer-Aided VLSI System Design

STA Lab 1: Static Timing Analysis

Objectives:

In this lab, you will learn:

1. How to use STA tools to analyze the timing of synchronous digital ASICs.
2. How to fix these problems of the timing violations.

Environment Setup:

1. Source the license file:

   source /usr/cad/synopsys/CIC/primetime.csh

Download files from ~cvsd/CUR/PrimeTime/STALab

1. Create a work directory and copy the lab files into it.
2. Check if you have these files.

Filename	Description
ALU_syn.v	Gate level Verilog code for the simple ALU
ALU.spef	Time and RC information file for the simple ALU
ALU_pt.script	Scripts to run PrimeTime
ALU_syn.script	Scripts to run PrimeTime
.Synopsys_dc.setup	Synopsys Dft Compiler setup file (same format as Design Vision). Define search paths, library name *etc*.

Invoke PrimeTime STA tool

To invoke PrimeTime, you can do either one

pt_shell (command mode)

primetime & (GUI mode)

We encourage everybody to use command mode because:

a. The command mode helps you to keep a record of what you have done.

b. The command mode runs more efficiently than GUI mode.

c. The command mode helps you to lookup the manual/reference quickly.

In spite of the above advantages, command mode sometimes is not as good as GUI mode in terms of debugging the schematic problem. We will use command mode throughout this Lab. You are welcome to try the GUI mode by yourself.

Start Operating PrimeTime STA tool

STA Environment Setting for TSMC 0.13um Technology:

1. Set search path *(If it has not been set up yet)*

   set search_path ". /home/raid2_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db "

2. Set link library

   set link_path "* typical.db fast.db slow.db"

Read Gate level Netlist Files and Link design:

1. Type these lines to read in CIC .18 library and your gate level netlist.

   read_verilog ./ALU_syn.v

2. Link all designs

   link_design ALU

Note, you have to check the search path and include library, if you get the error message after step 2.

Read Timing and RC information:

Reads leaf cell and net timing and RC information from a file in SPEF Format and uses that information to annotate the current design.

read_parasitics ALU.spef

Note: The file can be get during synthesis with "write_parasitics" comment.

Set Operating Conditions:

set_operating_conditions typical -library typical

Set Design Constraints:

This step tells the Dft Compiler how many scan chains you want. You can also specify the names of scan related pins (scan_enable, scan_in, scan_out). We will let Dft Compiler to choose the pin names for us.

1. Specify the clock name, period, and clock characteristic

```
create_clock -period 10 -waveform {0 5} [get_ports clk]
set design_clock [get_clock clk]
set_clock_uncertainty 0.5 $design_clock
set_clock_latency -min 1.5 $design_clock
set_clock_latency -max 2.5 $design_clock
```

set_clock_transition -min 0.25 $design_clock

set_clock_transition -max 0.30 $design_clock

set_propagated_clock $design_clock

2. Set wire load model

set_wire_load_model -name "ForQA" -library "typical"

3. Set wire load mode

set_wire_load_mode top

4. Report

report_design

report_reference

Questions:

How many reference cells will you have? _____.

And total area size = _____.

Timing analysis and report possible problems:

This step checks your scan specification for consistency. Please type the following commands to set the input/output delay:

set_input_delay 1.5 [get_ports inputA] -clock $design_clock

set_input_delay 1.5 [get_ports inputB] -clock $design_clock

set_input_delay 1.5 [get_ports instruction] -clock $design_clock

set_input_delay 1.5 [get_ports reset] -clock $design_clock

set_output_delay 1.5 [get_ports alu_out] -clock $design_clock

And then check the timing:

check_timing

set true_delay_prove_true_backtrack_limit 20000

report_timing -true

report_bottleneck

Questions:

Does the design meet the timing requirement? _____.

Find the critical path: Start-point = _____

End-point = _____

Change the setting and check the timing again:

create_clock -period 2 -waveform {0 1.0} [get_ports clk]

report_timing -true

Questions:

Now, does the design meet the timing requirement? _____.

Is it the setup time violation or the hold time violation? _ setup time _____.

If all other setting is the same, what is the maximum clock period for the design to meet the timing requirement? _____ ns.

Try to modify the setting and verify the number you get with STA tool. Do you succeed? _____.

Change the setting and check the timing again:

create_clock -period 10 -waveform {0 5.0} [get_ports clk]

set_output_delay 8 [get_ports alu_out] -clock $design_clock

report_timing -true

Questions:

Now, does the design meet the timing requirement? _____.

Where is the new critical path: Start-point = _____

End-point = _____

Reports:

1. Show the types of checks being done (setup, hold, min pulse width, recovery, removal and so forth)

report_constraint

report_constraint -all_violators

report_analysis_coverage

Questions:

How many timing violations are there in the design? _____

2. Change the setting and check the report again:

set_clock_uncertainty 0.0 $design_clock

report_constraint

report_constraint -all_violators

report_analysis_coverage

Questions:

Why are the hold-time violations fixed? Think about the clock setting in the previous synthesis Lab and try to explain. Note that the synthesis script can be referred in "*ALU_syn.script*."

_____

_____

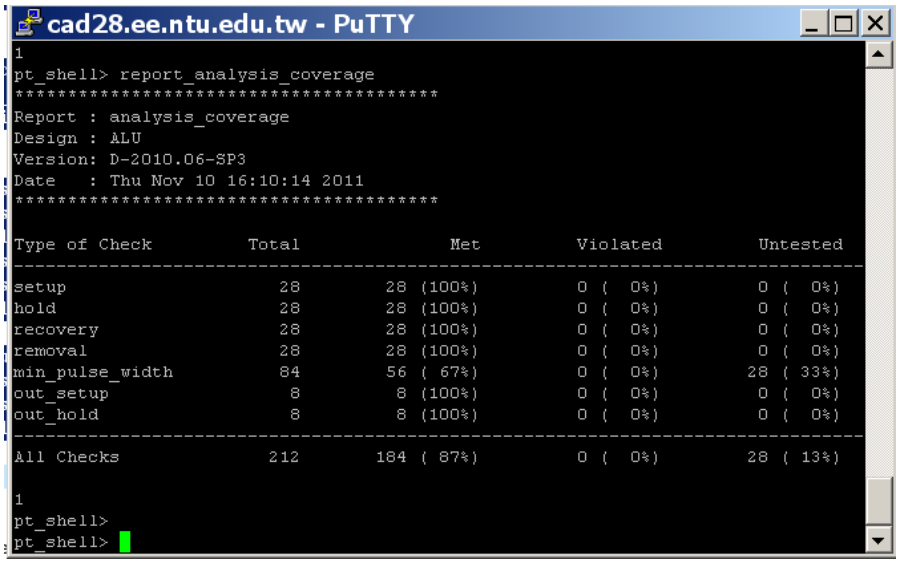
_____

_____

Checkpoints:

Please check with TAs before leaving this lab to make sure the following goals are accomplished and to get credits.

1. Show your final STA results as follows.



2. Show your answers of the questions in this lab document.

END of LAB……

Creator:

1st Edition: Huai-Yi Hsu, 2002

2nd Edtion: Yu-Lin Chang, 2004

3rd Edition: Yu-Lin Chang, 2006

4th Edition: Jui-Hsin Lai (Larry), 2008

5th Edition: Fu-Chen Chen, Chieh-Li Chen 2009

6th Edition: Yung-Lin Huang 2010

7th Edition: Tung-Chien Chen 2011