SOCE Lab (2/2): Clock Tree Synthesis and Routing

Lab materials are available at "~cvsd/CUR/SOCE/powerplan.tar.gz"
Please untar the file in the folder "SOCE_Lab" before lab

1 Open SOC Encounter

1.1 % source /usr/cadence/CIC/soc.csh

1.2 % encounter

Note: DO NOT add "&" after the command "encounter" (background mode). We will use two different interfaces for SoC Encounter, (1) terminal (command line) mode, and (2) graphic user interface (GUI).

2 Restore design

Design → Restore Design →SoCE…→select powerplan.enc

3 Perform timing analysis

Timing →Analyze Timing…***OK***

If worst negative slacks〈WNS〉is negative, optimization is needed to fix the problem. (If DRV has "max fanout violation," we also can use optimizationto fix it.)

Timing →Optimize…: for Optimization Type, select "Max Fanout" in addition，***OK***

If WNS is still negative after the optimization, please keep perform optimization until WNS is positive.

Add Tie High/Low Cell

4 Bind 1'b0 and 1'b1 to "tie high" and "tie low" cell, respectively

4.1 Set tiehi tielo mode

Design → Mode Setup…: select TieHiLO at left side, type TIEHI TIELO in Cell Name at right side, set Maximum Fanout = 10, and set Maximum Distance = 100. ***OK***

4.2 Place →Tie HI/LO →Add，set Cell Name = TIEHI TIELO，***OK***

(Note: TIEHI TIELO has a blank between the two words; do not use brace for the two words)

Clock Tree Synthesis

5 Clock →Design Clock

In Synthesis Clock Tree Form, click ***Gen Spec…***

5.1 In Generate Clock Spec Form, add cells with name in CLKBUF* or

CLKINV* into Selected Cells.
Set Output Specification Files = Clock.ctstch，***OK***

5.2 Open a new terminal〈please use another terminal instead of encounter's terminal〉，then use any text editor to modify Clock.ctstch
Set MaxDelay=1ns, and MinDelay=0ns; save the file.
(One can use the two values in default. However, the tool will, somehow, make efforts and consume time to meet the setting because of large delay. Thus, we use small value in the lab.)

5.3 Back to Synthesize Clock Tree Form, preserve Clock.ctstch in Clock Specification File，***OK***

5.4 After CTS, we can see clock timing results in log. Also, we can check clock_report/clock.report to see that constraints are met or not.

6 Clock →Display→Display Clock Tree…

6.1 In Display Clock Tree form, activate Display Clock Tree and All Level in Display Selection，***OK***

6.2 Switch to physical view and disable net display. Then we can see the distribution of the clock tree.

6.3 Clock →Display→Display Clock Tree…: select Display Clock Phase Delay，***OK***
Red (blue) color represents the most serious (lightest) phase delay.

6.4 Clock → Clock Tree Browser…，select CLK in Clock Tree Browser Form，***Select***，***OK***

6.5 In Clock Tree Browser, Display → Hide/Show →…Input Tran: we can see input transition time of al leaf instances

6.6 Browser →Close，close Clock Tree Browser

6.7 Clock →Display →Clear Clock Tree Display

7 (P.S. We can manually modify the clock tree in Edit.)

8 Design →Save Design as → SoCE…，use file name "cts.enc"

9 Perform Timing analysis again
Timing →Analysis Timing, select Post-CTS in Design Stage，***OK***

9.1 If WNS is negative，do Timing → Optimize… with Post-CTS，***OK***，

9.2 Repeat 9.1 until WNSis positive; then save the file with file name "cts.enc"

Q1: Currently, WNS is?_____；TNS is?_____。

Route Power

10 Connect Powerpin

10.1 Route →Special Route…

10.2 Net(s): VSS VDD

Route: use only Standard cell pins→***OK***

Disable net display, and then we can see that core cells are wired to power ring.

11 Check DRC and connectivity for Special Net

11.1 Place →Refine Placement…, ***OK***

Signal nets of trial route are removed.

11.2 Verify →Verify Geometry…, ***OK***

Confirm that there are no geometry violations.

11.3 Verify →Verify Connectivity…: select Special Only for Net type, deactivate unrouted net,

Any violation ?

(If there is any violation, select the wire/net with violations, and press capitalized 'T' to fix the violatiom. Repeat 11.3 until no more violations.)

12 Add IO Filler

12.1 Execute addIoFiller_tpz.cmd in encounter's terminal

encounter> source addIoFiller_tpz.cmd

12.2 The space of IO pads is filled.

13 Design →Save Design As →SoCE⋯: use file name "powerroute.enc"，Save

Routing

14 Route

14.1 Route →NanoRoute →Route… activate Timing drive and SI Driven

activate Insert Diodes and type ANTENNA for Diode Cell Name

14.2 Click Attribute

In NanoRoute/Attribute form

14.2.1 activate Nettype(s) and Clock Nets

14.2.2 Weight: 10

14.2.3 Spacing: 1

14.2.4 Avoid Detour: True (means that route as short as possible)

14.2.5 ***OK***

14.3 Click OK in NanoRoute form, and then routing starts

Any violation? (If overlap violations appear on the IO filler, we can ignore these. Tools → Clear Violation)

Q2: Total wire length? _____um。

15 Timing Analysis, Post route Optimization

15.1 Timing →Analysis Timing

Select Post-Route in Design Stage

Analysis Type: Setup

OK

15.2 If WNS is negative, the go to 15.3, or go to 15.4.

15.3 Timing →Optimize

Design Stage: Post-route

Activate Max Fanout

OK

Repeat 15.3 until WNS is positive.

15.4 Perform 15.1, but change Analysis Type to Hold for hold time

Q3: Setup time analysis: WNS = _____；TNS = _____。

Q4: Hold time analysis: WNS = _____；TNS = _____。

15.5 Design →Save Design As →SoCE…: use file name "routed.enc"

16 Add Core Filler

16.1 Place →Physical Cells →Add Filler…，click ***Select***

Add all filler to Selectable Cells Lists at left side from Cells List at right side. ***Close***

16.2 Click OK in Add Filler form

16.3 Verify Geometry…, ***OK***

16.4 Verify Process Antenna…, ***OK***

16.5 Verify Connectivity, activate All and unrouted net…, ***OK***

16.6 Design →Save Design As →SoCE: use file name "corefiller.enc"

17 Finish

17.1 Design →Save →Netlist…, Netlist File uses CHIP.v, ***OK***

17.2 Timing →Calculate Delay…, deactivate Ideal Clock, save as CHIP.sdf, ***OK***

17.3 Design →Save →DEF…, activate Save Scan，File Name uses CHIP.def, ***OK***

18 Add dummy metal

Route →Metal Fill →Add…, deactivate Tie High/Low to net(s)，OK

Then the layout is filled with dummy metals.

19 Add bonding pad

19.1 Use unix terminal

% perl addbonding.pl CHIP.def

19.2 Use encounter terminal

encounter> source bondPads.cmd

The bonding pads are added to IO pads.

Q5: How many bondpads are added (number of new instances)? _____

20 To make sure that the LVS verification and posim extraction can find the positions of IO power, we need to add power labels. The label positions must be on the pads.

20.1 Edit →Custom Object Editor: type METAL8 in Layer, and then press enter
Select Text, set text = IOVDD, Origin X = 1123, Y = 282, and Height = 10,
and then click ***Add to List***

20.2 Select Text, set text = IOVSS
Set Origin X = 1234, Y = 337
Add to List

20.3 ***Apply***, ***Close***. We can see that IOVDD and IOVSSare added in the expected positions.
Design →Save Design As →SoCE…: use file name “finish.enc”

21 Stream out GDS

21.1 Design →Mode Setup…: select StreamOut page at left side, and deactivate Virtual Connection at right side ***OK***

21.2 Design →Save →GDS/OASIS…: set Output Stream File = CHIP.gds
set Map Filie = library/streamOut.map
set Merge Stream File = library/gds/tpz013g3_v1.1.gds
library/gds/tsmc13gfsg_fram.gds
(use a blank between the two file names)
Activate Wire abstract information for LEF Macros
Unit: 1000
OK

21.3 Design →Exit, ***Yes***

Appendix: Power Analysis

1. Simulation-based power analysis
   1.1 Design →Save →Netlist… save as CHIP.v
   1.2 Timing → Extract RC…，click OK。
   1.3 Timing →Calculate Delay…，save delay as CHIP.sdf，deactivate Ideal Clock，click OK。
   1.4 Use CHIP.v and CHIP.sdf to obtain .vcd (CHIP.vcd) file by verilog simulation. The file can be used for the power analysis.
2. Power Analysis
   2.1 Power → Power Analysis → Set Power Analysis Mode…，OK。
   2.2 Power → Power Analysis → Run Power Analysis…，select VCD File，then set…
   Scope: scope module
   Start: start cycle
   Stop: end cycle
   2.3 Click ADD，OK。
   2.4 Power analysis results in text shows in CHIP.rpt
   Four representative values of total power consumption can be found at the bottom of CHIP.rpt: Internal Power, Switching Power, Total Power and Leakage Power。
3. Power Graph
   3.1 Power → Report → Power & Rail Result…，select power Datebase in Start, and type power.db (the generated power analysis file)
   3.2 For Power Analysis Plot Type in Plot, select ip-Instance Total Power，Apply Power consumption of each cell are displayed.
   3.3 For Action, select Clear Display，OK. The power graph is closed.
4. Rail Analysis
   4.1 Power → Rail Analysis → Early Rail Analysis…，open Early Analysis GUI window
   4.2 Set Net Name = VSS, Power data = Instance Current File，and type static_VSS.ptiavg。
   4.3 Click Create for Pad Location File，open Edit Pad Location window，
   Type VDD in Net, then click Auto Fetch
   Type VSS in Net, then click Auto Fetch
   4.4 We can find the positions of power/ground pad in Pad Location List; then click Save…, and save as CHIP.pp，click Save，Cancel
   4.5 Back to Early Analysis GUI window，Type CHIP.pp in Pad Location File，

click OK。

4.6 In Power & Rail Results window, select ir-IR Drop for Rail Analysis Plot Type in Plot, and click Linear of Auto Filter，Auto，Apply。

4.7 Encounter shows IR drop results. We can disable the display of Instance、Net、Special Net in display control to show the results.

5. EM power graph

5.1 In Power & Rail Results window, select er-Electromigraion Risk for Rail Analysis Plot Type in Plot, and click Linear of Auto Filter，Auto，Apply。

5.2 Encounter shows Electron migration results。

5.3 For Action, select Clear Display，OK. The power graph is closed.