Logic Synthesis & Verification, Fall 2011

National Taiwan University

Problem Set 6

Due on 2012/1/4 before lecture

1 [SDC and ODC]

Consider the Boolean network of Figure 1.

(a) Write down a Boolean formula for the SDC of the entire network.
(b) Write down a Boolean formula for the satisfiability don't cares SDC_4 of Node 4. Since SDC_4 is imposed by the fanins of Node 4, the formula should depend on variables $x_1, \ldots, x_4, y_1, \ldots, y_3$. How can you make SDC_4 only depend on y_1, y_2, y_3 such that we can minimize Node 4 directly?
(c) Compute the observability don't cares ODC_4 of Node 4.

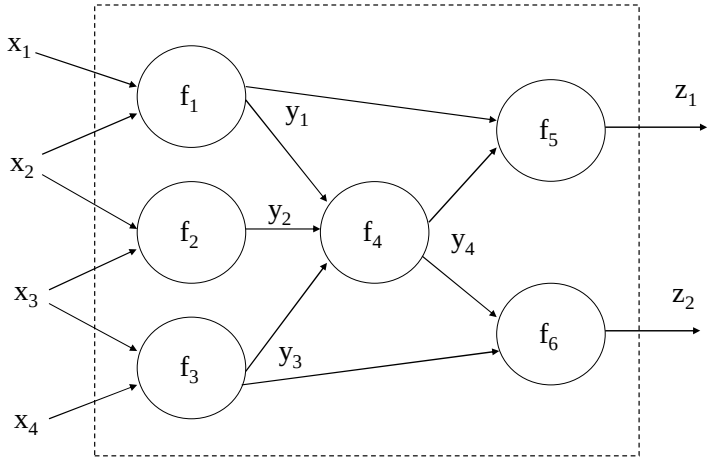

Fig. 1. A Boolean network, where $f_1 = x_1x_2$, $f_2 = x_2 \vee x_3$, $f_3 = \neg(x_3x_4)$, $f_4 = \neg y_1\neg y_2y_3 \vee y_1y_2\neg y_3$, $f_5 = y_1 \vee y_4$, and $f_6 = y_3y_4$.

2 [Don't Cares in Local Variables]

Consider the Boolean network of Figure 1. Suppose the XDC for z_1 is $\neg x_1\neg x_2\neg x_3\neg x_4$ and that for z_2 is $x_1x_2x_3x_4$.

(a) Compute the don't cares D_4 of Node 4 in terms of its local input variables y_1, y_2, and y_3. (Note that in general the computation of ODC may be affected by XDC especially when there exist different XDCs for different primary outputs.)
(b) Based on the computed don't cares, what is the best implementable function for Node 4 (in terms of the literal count and cube count)?

3 [Complete Flexibility]

Consider the Boolean network of Figure 1. Let $Y = \{y_1, y_2, y_3\}$.

(a) Suppose the XDC for z_1 is $\neg x_1 \neg x_2 \neg x_3 \neg x_4$ and that for z_2 is $x_1 x_2 x_3 x_4$. Write down the specification relation $S(X, Z)$.
(b) What is the influence relation $I(X, y_4, Z)$ of Node 4?
(c) What is the environment relation $E(X, Y)$ of Node 4?
(d) What is the complete flexibility $CF_4(Y, y_4)$ of Node 4?
(e) Is the previously computed don't care set D_4 of Node 4 subsumed by CF_4?

4 [Timing Analysis]

(a) Given the circuit of Figure 2, compute the *arrival time*, *required time*, and *slack* of every net assuming the required times for the primary output are 8ns. Identify the critical path(s).
(b) Given the circuit of Figure 2, perform the SAT-based functional timing analysis to compute the longest true delay. Show a general way to identify the longest true-delay path in SAT-based functional timing analysis.

5 [Retiming]

Consider the circuit of Figure 3.

(a) Draw the corresponding retiming graph.
(b) What are the corresponding W and D matrices?
(c) Write down the inequality constraints of the integer linear program for a retime function r satisfying the condition that the clock period $c \leq 4$ ns.
(d) Draw the corresponding constraint graph for the set of inequality constraints in (c).
(e) Is there a negative-weighted cycle in the constraint graph? Derive a feasible retime function if it exists.

(Hint: You may need to create a dummy node for every fanout point.)

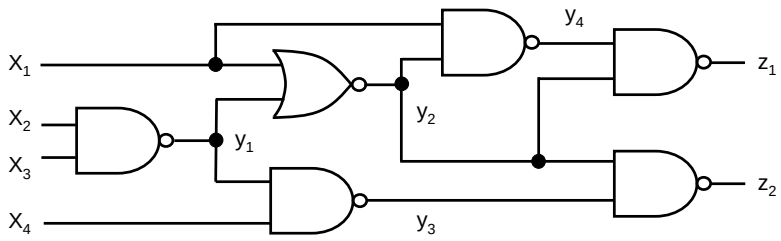

Fig. 2. A circuit under timing analysis. Assume the arrival times for all of the primary inputs are 0 except for x_2 with arrival time 1ns, the gate delay of a NAND is 2ns, and the gate delay of a NOR is 3ns.)

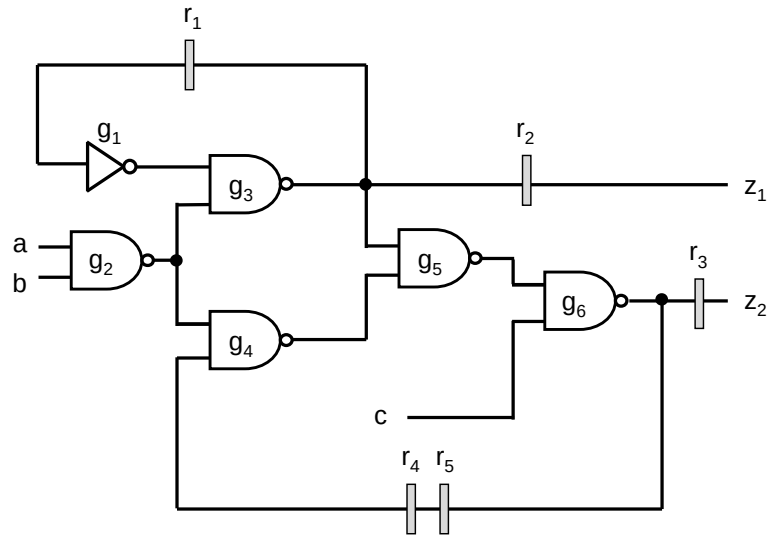

Fig. 3. A circuit under timing optimization, where NAND2 and INV are of gate delays 2ns and 1ns, respectively.