Switching Circuits & Logic Design

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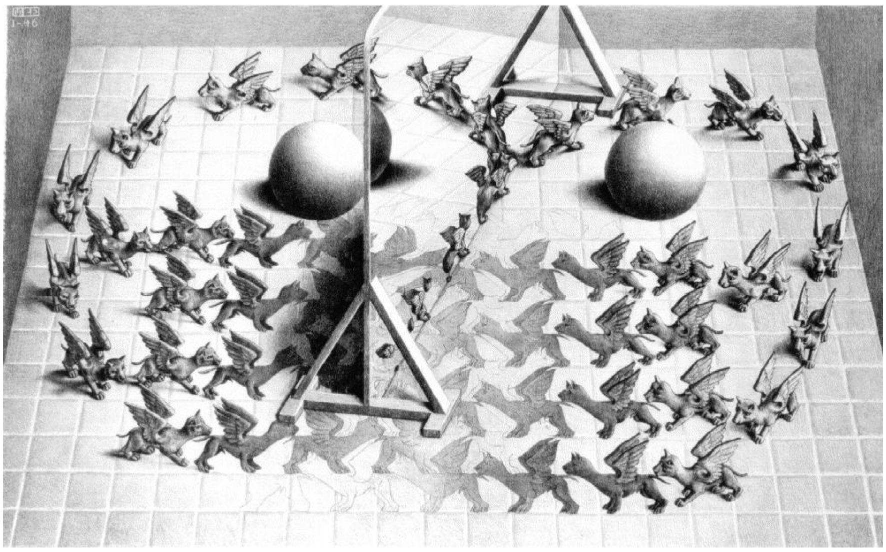
§13 Analysis of Clocked Sequential Circuits



Magic Mirror
M.C. Escher, 1946

Outline

- A sequential parity checker
- Analysis by signal tracing and timing charts
- State tables and graphs
- General models for sequential circuits

A Sequential Parity Checker

- When binary data is transmitted or stored, an extra bit (call a **parity bit**) is frequently added for the purposes of error detection
  - Odd (even) parity: the total number of 1's in the block, including the parity bit, is odd (even)

Example (8-bit words with odd parity)

7 data bits parity bit

0000000 1
0000001 0
0110110 1
1010101 1
0111000 0

8-bit word

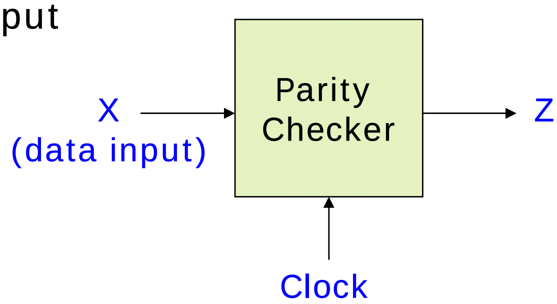
1010000 0

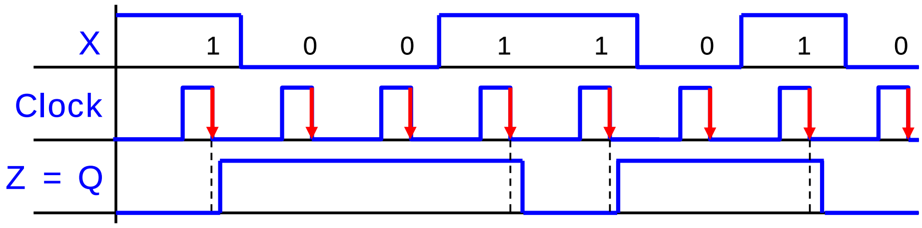
error occurred

A Sequential Parity Checker

- A parity checker for serial data
  - Z = 1 ⇔ the total number of 1 inputs received is odd (i.e., input parity is odd)
  - Z = 0 initially

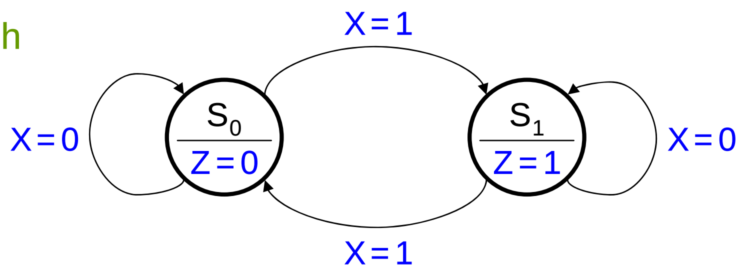
Block diagram





A Sequential Parity Checker

State graph

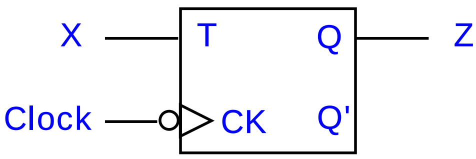


State table

Present State	Next State X=0	Next State X=1	Present Output
S_0	S_0	S_1	0
S_1	S_1	S_0	1

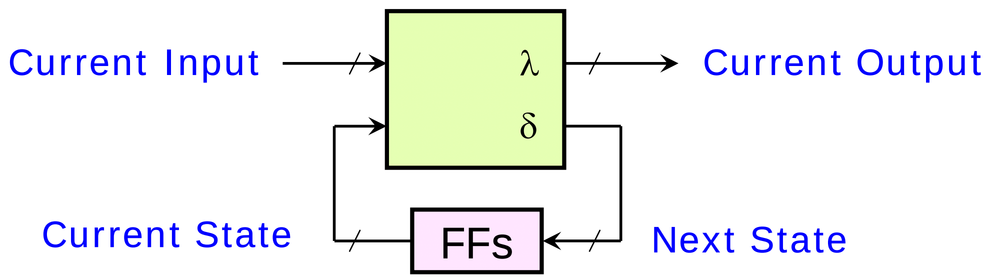
Q	Q^+ X=0	Q^+ X=1	T X=0	T X=1	Z
0	0	1	0	1	0
1	1	0	0	1	1

Logic circuit



Signal Tracing and Timing Charts

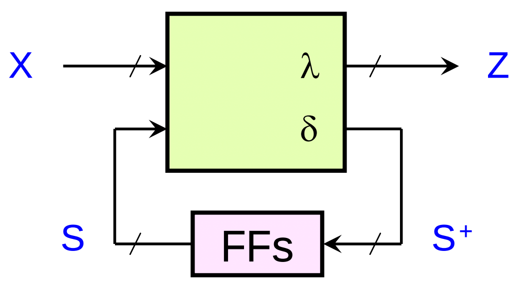
- Find the output sequence resulting from a given input sequence by tracing 0 and 1 signals through a circuit
  1. Assume an initial state of the flip-flops
  2. Given a current input at the present state, determine the circuit outputs and next state (flip-flop inputs)
  3. Update the present state to the next state, and repeat 2



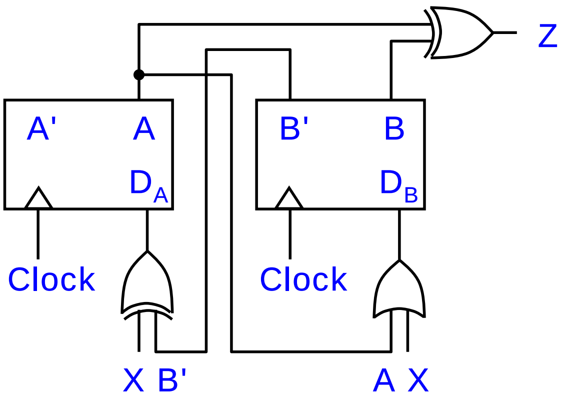
A sequential circuit with n FFs has 2^n states

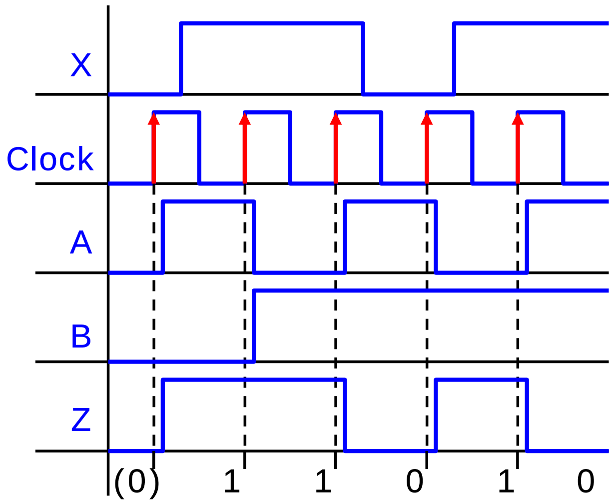
Signal Tracing and Timing Charts

- There are two types of clocked sequential circuits
  - **Moore machine**
    - Output depends only on the present state
      - Output function λ(S)
  - **Mealy machine**
    - Output depends on both the present state and the input
      - Output function λ(S,X)



Signal Tracing and Timing Charts
A Moore Sequential Circuit Example





Assume A=B=0 initially

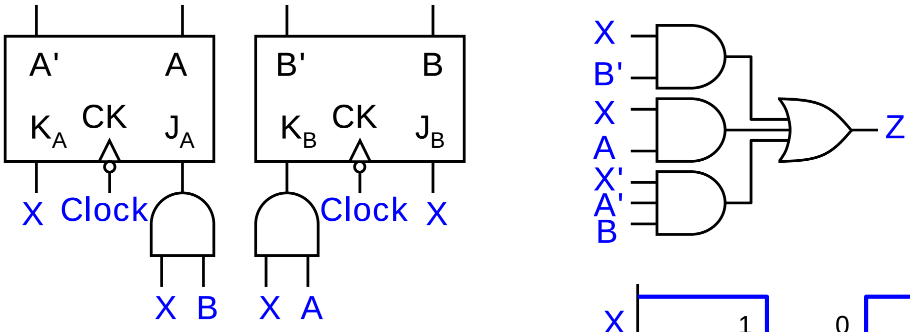
X = 0 1 1 0 1
A = 0 1 0 1 0 1
B = 0 0 1 1 1 1
Z = (0) 1 1 0 1 0

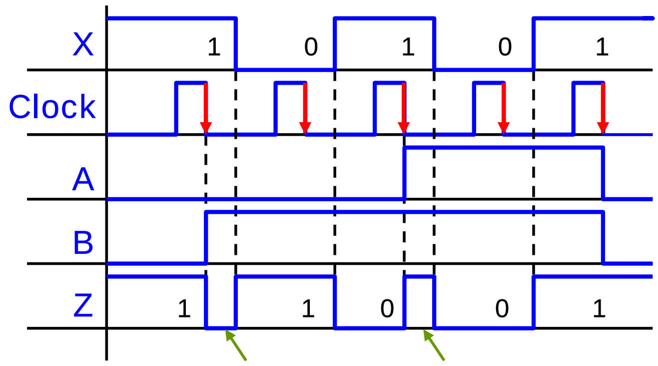
Output is a function of states only
⇒ a Moore circuit

Signal Tracing and Timing Charts
Moore Sequential Circuit

- For a Moore circuit, the output which results from application of a given input does not appear until after the active clock edge
  - The output sequence is displaced in time with respect to the input sequence

Signal Tracing and Timing Charts
A Mealy Sequential Circuit Example





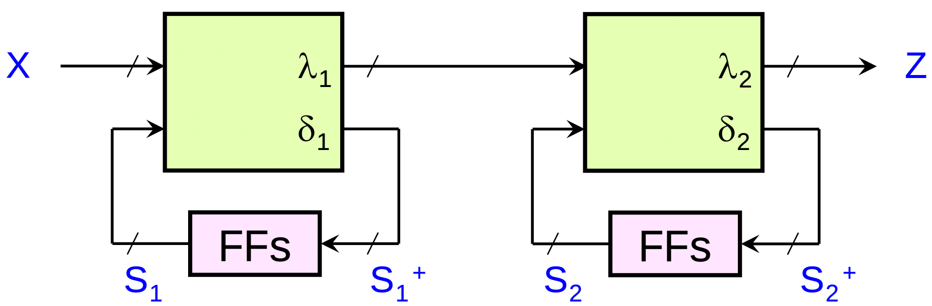
X =	1	0	1	0	1	
A =	0	0	0	1	1	0
B =	0	1	1	1	1	0
Z =	1(0)	1	0(1)	0	1	

false outputs

Output is a function of both states and inputs ⇒ a Mealy circuit

Signal Tracing and Timing Charts
Mealy Sequential Circuit

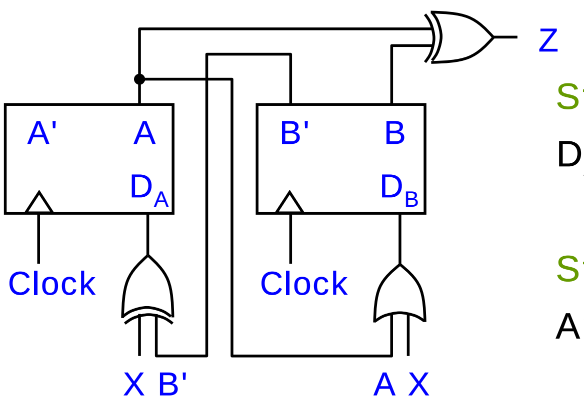
- For a Mealy circuit, the output may temporarily assume an incorrect value (called a **false output**, **glitch**, **spike**)
  - The false output occurs after the circuit has changed state and before the input is changed; however, the correct output must appear before the active clock edge
    - No false output can appear in a Moore circuit
  - The output sequence is not displaced in time with respect to the input sequence
  - If the output of the circuit is fed into a second sequential circuit which uses the same clock, the false outputs will not cause any problem because the inputs to the second circuit can cause a change of state only at the active clock edge



State Tables and Graphs

- Procedure to construct the state table
  1. Determine the FF input equations and output equations from the circuit
  2. Derive the next-state equation for each FF from its input equations
     - D FF $Q^+ = D$
     - D-CE FF $Q^+ = D \cdot CE + Q \cdot CE'$
     - T FF $Q^+ = T \oplus Q$
     - S-R FF $Q^+ = S + R'Q$
     - J-K FF $Q^+ = JQ' + K'Q$
  3. Plot a next-state map for each FF
  4. Combine these maps to form the state table (or called transition table)

State Tables and Graphs
A Moore Sequential Circuit Example



Step 1

$D_A = X \oplus B'$ $D_B = X + A$ $Z = A \oplus B$

Step 2

$A^+ = X \oplus B'$ $B^+ = X + A$

Step 3

A^+

AB \ X	0	1
00	1	0
01	0	1
11	0	1
10	1	0

B^+

AB \ X	0	1
00	0	1
01	0	1
11	1	1
10	1	1

Step 4

AB	A^+B^+ X=0	A^+B^+ X=1	Z
00	10	01	0
01	00	11	1
11	01	11	0
10	11	01	1

State Tables and Graphs
A Moore Sequential Circuit Example

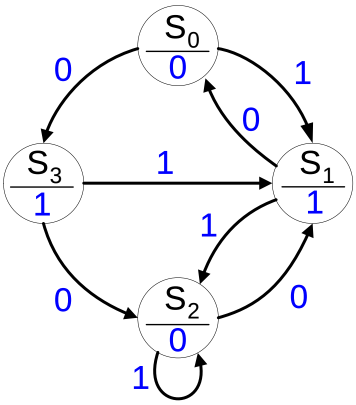
State tables

AB	A^+B^+ X=0	A^+B^+ X=1	Z
00	10	01	0
01	00	11	1
11	01	11	0
10	11	01	1

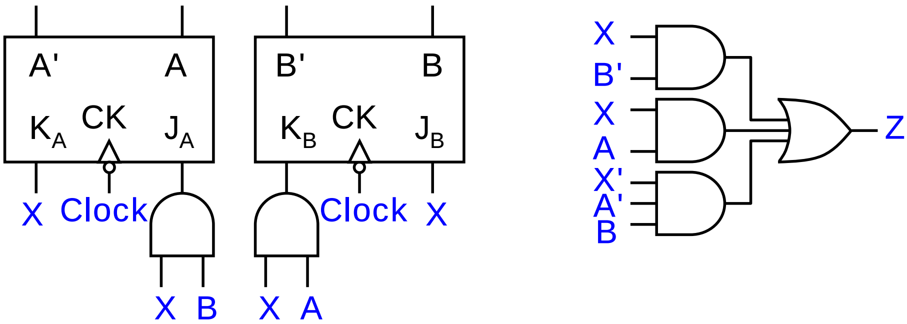
Symbolic representation

Present State	Next State X=0	Next State X=1	Present Output (Z)
S_0	S_3	S_1	0
S_1	S_0	S_2	1
S_2	S_1	S_2	0
S_3	S_2	S_1	1

State graph



State Tables and Graphs
A Mealy Sequential Circuit Example



Steps 1,2

$A^+ = J_A A' + K'_A A = XBA' + X'A$

$B^+ = J_B B' + K'_B B = XB' + (AX)'B = XB' + X'B + A'B$

$Z = X'A'B + XB' + XA$

State Tables and Graphs
A Mealy Sequential Circuit Example

Step 3

A^+

AB \ X	0	1
00	0	0
01	0	1
11	1	0
10	1	0

B^+

AB \ X	0	1
00	0	1
01	1	1
11	1	0
10	0	1

Z

AB \ X	0	1
00	0	1
01	1	0
11	0	1
10	0	1

Step 4

	A^+B^+		Z	
AB	X=0	X=1	X=0	X=1
00	00	01	0	1
01	01	11	1	0
11	11	00	0	1
10	10	01	0	1

State Tables and Graphs
A Mealy Sequential Circuit Example

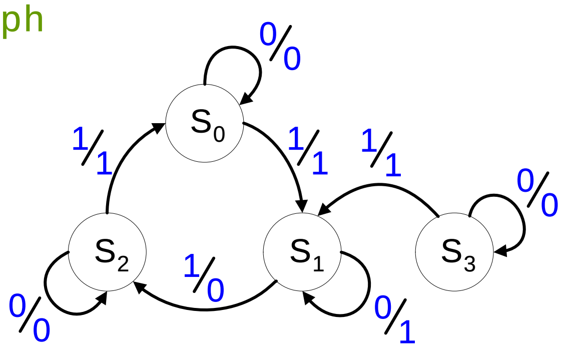
State tables

	A^+B^+		Z	
AB	X=0	X=1	X=0	X=1
00	00	01	0	1
01	01	11	1	0
11	11	00	0	1
10	10	01	0	1

Symbolic representation

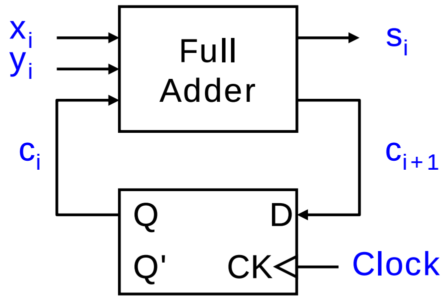
Present State	Next State		Present Output	
	X=0	X=1	X=0	X=1
S_0	S_0	S_1	0	1
S_1	S_1	S_2	1	0
S_2	S_2	S_0	0	1
S_3	S_3	S_1	0	1

State graph



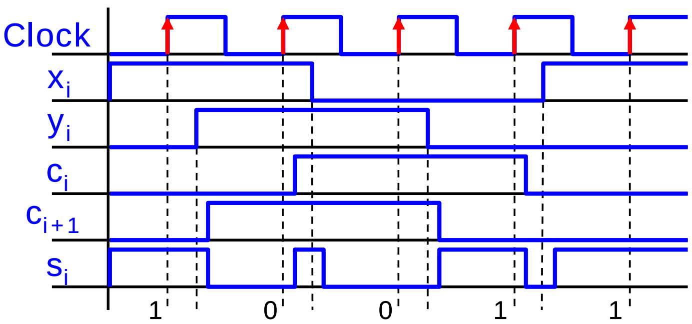
State Tables and Graphs
A Serial Adder Example

Serial adder with D FF

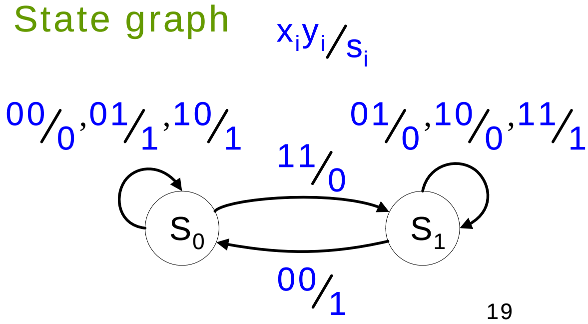


Truth table

x_i	y_i	c_i	c_{i+1}	s_i
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



State graph

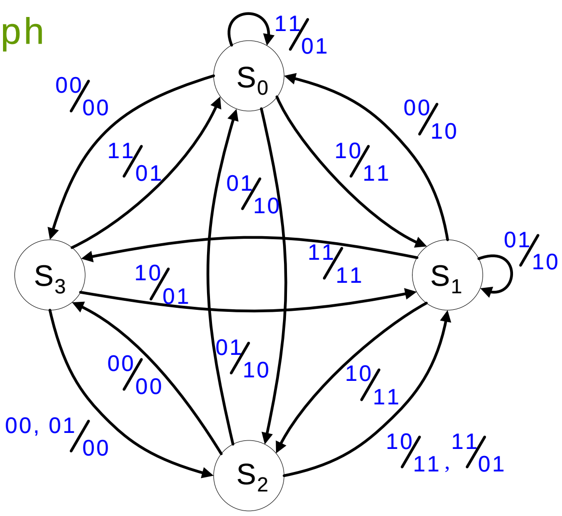


State Tables and Graphs
Example w/ Multiple Inputs & Outputs

State table

Present State	Next State X_1X_2 = 00	01	10	11	Present Output (Z_1Z_2) X_1X_2 = 00	01	10	11
S_0	S_3	S_2	S_1	S_0	00	10	11	01
S_1	S_0	S_1	S_2	S_3	10	10	11	11
S_2	S_3	S_0	S_1	S_1	00	10	11	01
S_3	S_2	S_2	S_1	S_0	00	00	01	01

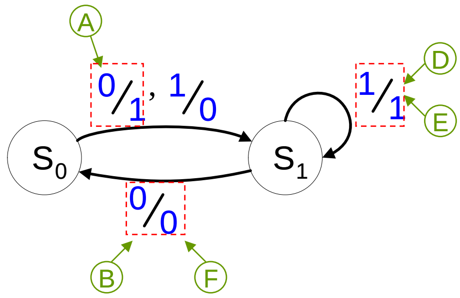
State graph



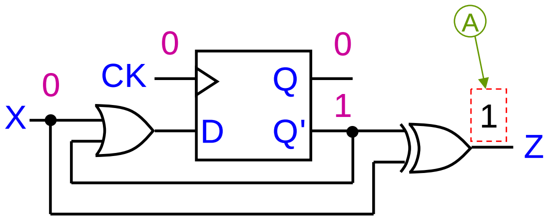
Given an initial state and an input sequence, we know the corresponding **state trace** and **output sequence**

State Tables and Graphs
Timing Charts

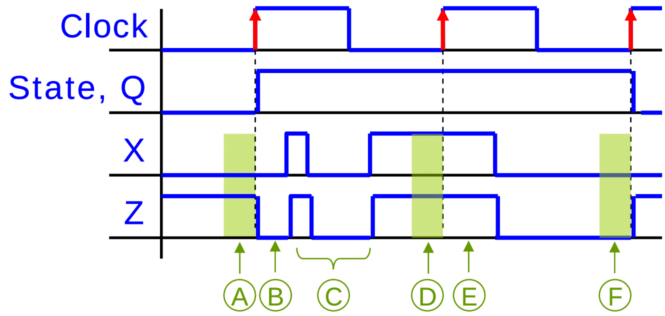
- Construction and interpretation of timing charts



Q		Present State X=0	X=1	Z X=0	X=1
0	S_0	S1	S1	1	0
1	S_1	S0	S1	0	1



Initial values are shown

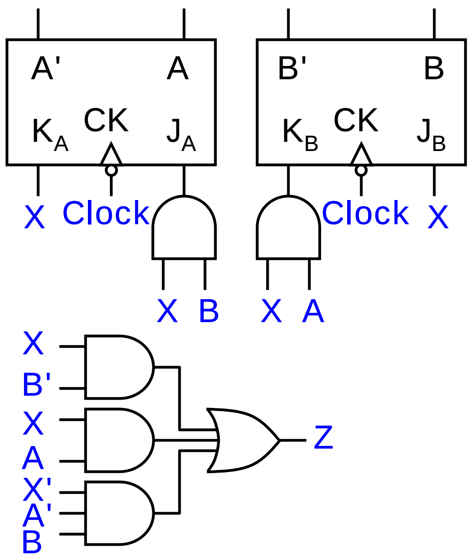


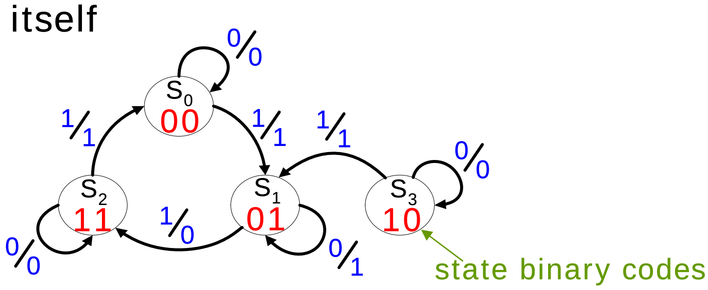
Read X and Z in shaded area

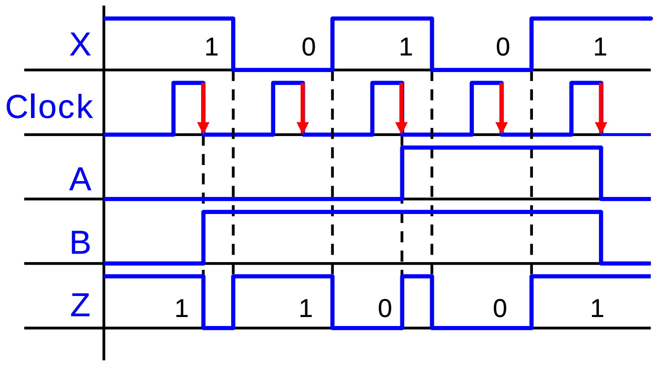
State Tables and Graphs
Signal Tracing and Timing Charts

- To plot a timing chart for a sequential circuit, the state graph (with states encoded in binary codes) can be a better reference than the circuit itself

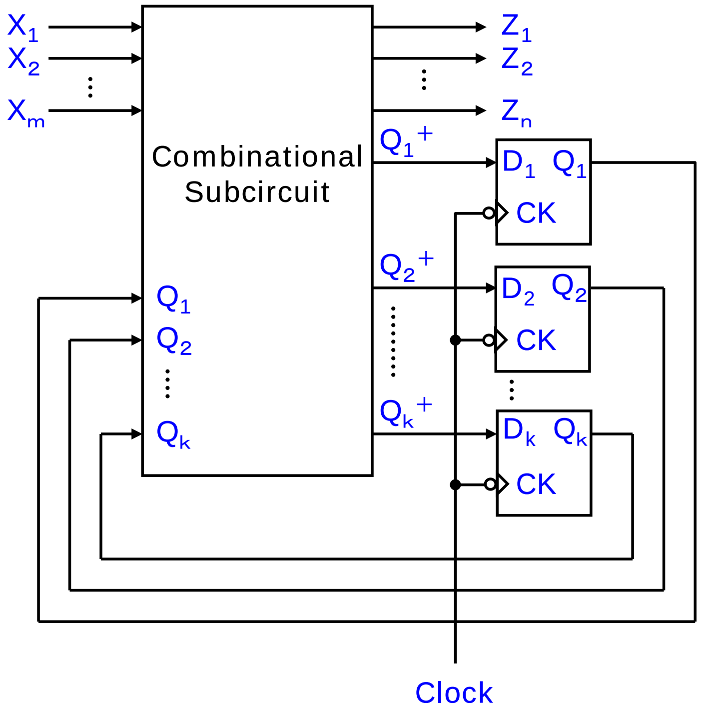
Prior Mealy circuit example







General Models for Sequential Circuits
Mealy Circuit Using D Flip-Flops



n output functions

$Z_1 = f_1(X_1,\ldots,X_m,Q_1,\ldots,Q_k)$

$\vdots$

$Z_n = f_n(X_1,\ldots,X_m,Q_1,\ldots,Q_k)$

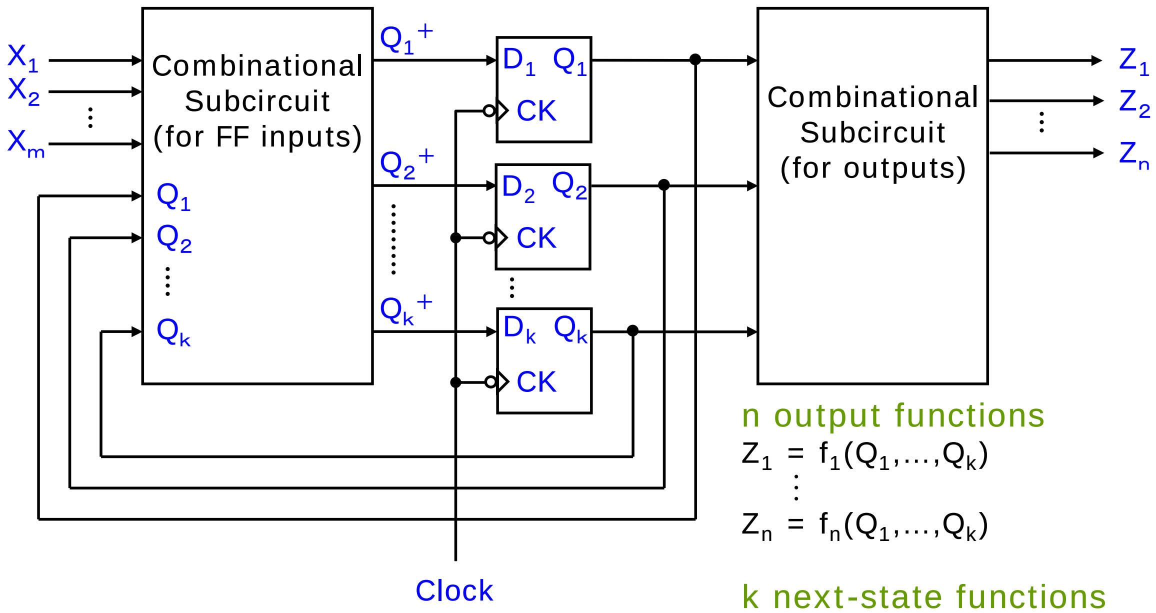
k next-state functions

$Q_1^+ = D_1 = g_1(X_1,\ldots,X_m,Q_1,\ldots,Q_k)$

$\vdots$

$Q_k^+ = D_k = g_k(X_1,\ldots,X_m,Q_1,\ldots,Q_k)$

General Models for Sequential Circuits
Moore Circuit Using D Flip-Flops



n output functions

$Z_1 = f_1(Q_1,\ldots,Q_k)$

$\vdots$

$Z_n = f_n(Q_1,\ldots,Q_k)$

k next-state functions

$Q_1^+ = D_1 = g_1(X_1,\ldots,X_m,Q_1,\ldots,Q_k)$

$\vdots$

$Q_k^+ = D_k = g_k(X_1,\ldots,X_m,Q_1,\ldots,Q_k)$

General Models for Sequential Circuits
Unary Representation

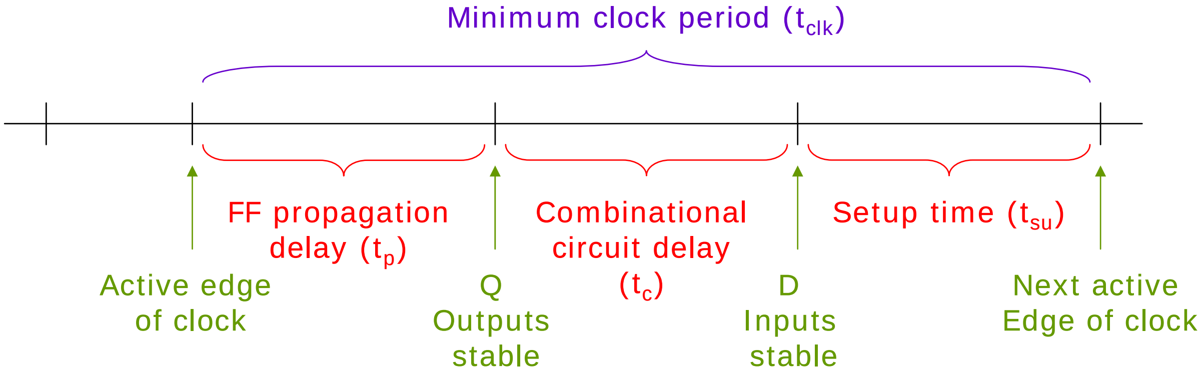
- $S^+ = \delta(S,X)$
- $Z = \begin{cases} \lambda(S,X) & \text{for Mealy machine} \\ \lambda(S) & \text{for Moore machine} \end{cases}$

Example (prior example with multiple inputs and outputs)

Present State	Next State X = 0	1	2	3	Present Output (Z) X = 0	1	2	3
S_0	S_3	S_2	S_1	S_0	0	2	3	1
S_1	S_0	S_1	S_2	S_3	2	2	3	3
S_2	S_3	S_0	S_1	S_1	0	2	3	1
S_3	S_2	S_2	S_1	S_0	0	0	1	1

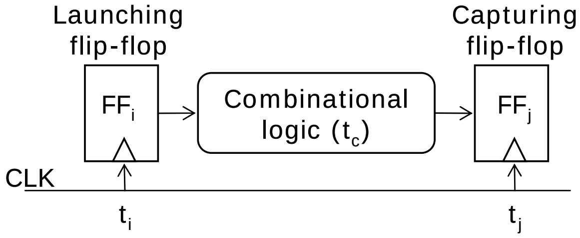
General Models for Sequential Circuits
Minimum Clock Period

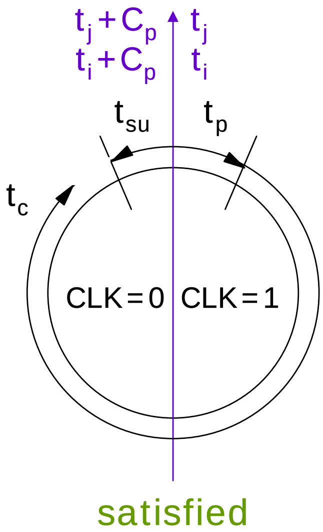
- The minimum clock period
  - $t_{clk}(\min) = t_x + t_c + t_{su}$, where t_x is the time after the active clock edge at which the X inputs are stable
  - $t_{clk}(\min) = t_p + t_c + t_{su}$, if $t_x \le t_p$

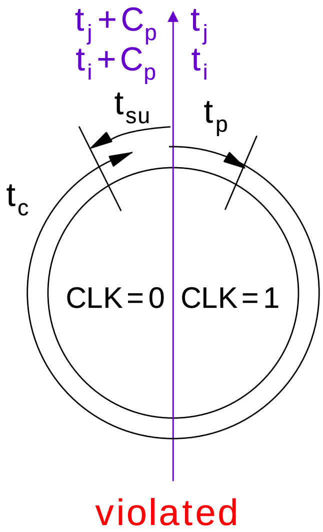


General Models for Sequential Circuits Timing Constraints

- Setup-time constraint
  - $C_p \geq t_p + t_c^{max} + t_{su}$







C_p: clock period

General Models for Sequential Circuits Timing Constraints

- Hold-time constraint
  - $t_p + t_c^{min} \geq t_h$