

# Logic Synthesis & Verification, Fall 2012

National Taiwan University

## Problem Set 6

Due on 2013/1/9 before lecture

### 1 [Technology Mapping]

- (10%) What are the criteria that make a collection of pattern graphs a legal cover of technology mapping? Which criterion is a unate condition? Which criterion is a binate condition? Why?
- (10%) Given the subject graph of Figure 1 and pattern graphs of Figure 2, express the feasibility of technology mapping in a CNF formula.
- (10%) Given the subject graph of Figure 1, perform dynamic programming to find optimum tree mapping using the pattern graphs of Figure 2. Show intermediate costs and the final optimum tree covering.
- (10%) Modify the subject graph of Figure 1 and pattern graphs of Figure 2 by inserting an inverter pair (i.e., a buffer) to every NAND-to-NAND wire. Perform technology mapping accordingly. What is the optimum tree covering? Is there any improvement due to the inverter pair insertion?

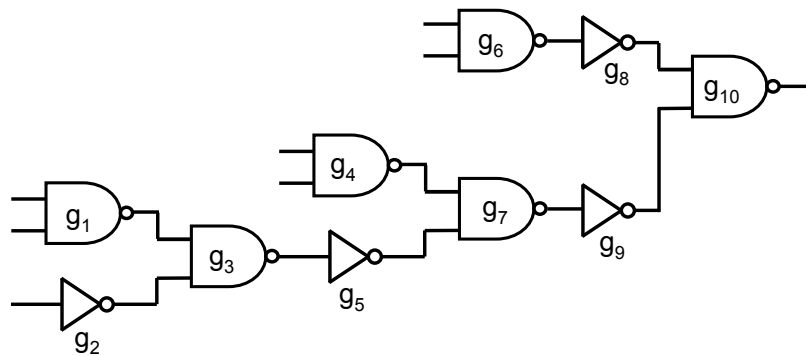
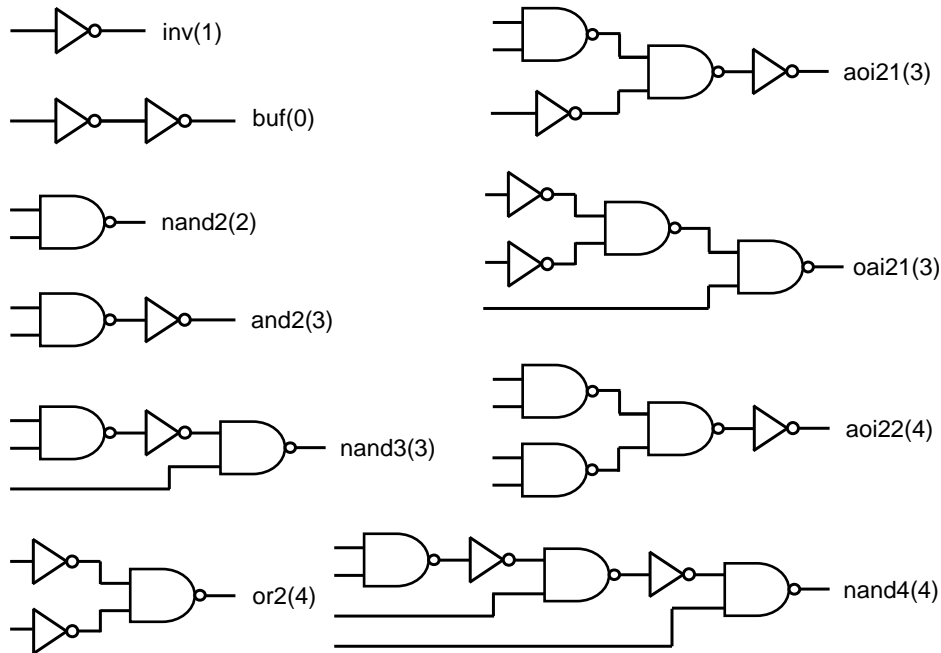


Fig. 1. Subject graph

### 2 [Timing Analysis]

- (5%) Given the circuit of Figure 3, compute the *arrival time*, *required time*, and *slack* of every net assuming the required times for the primary output are 8ns. Identify the critical path(s).



**Fig. 2.** Pattern graphs.

- (b) (10%) Given the circuit of Figure 3, perform the SAT-based functional timing analysis to compute the longest true delay.
- (c) (10%) Given the satisfying assignment in (b), identify the corresponding longest true delay path. (Hint: You may need the *exact sensitization criterion*, that is, the delay at a gate is determined by 1) the earliest arrival input with a controlling value, or 2) the latest arrival input when all inputs are of non-controlling values.)

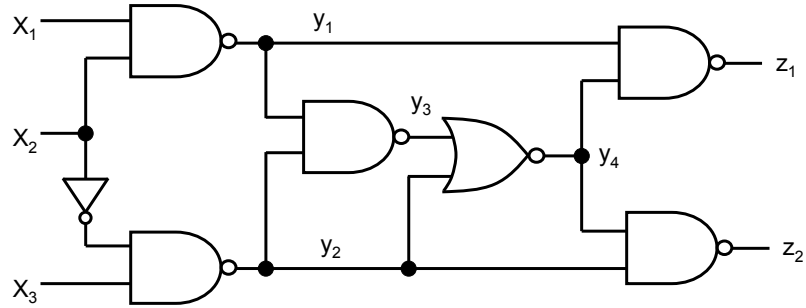
### 3 [Retiming]

Consider the circuit of Figure 4.

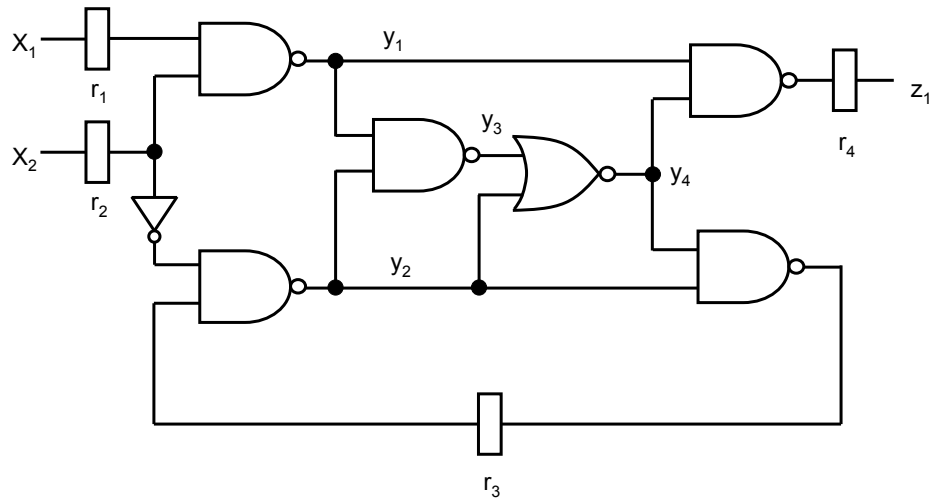
- (a) (10%) What is the minimum clock period achievable by clock skew scheduling? What are the corresponding skews of  $r_2$ ,  $r_3$ , and  $r_4$  (with respect to the clock of  $r_1$ )?
- (b) (5%) Draw the corresponding retiming graph.
- (c) (5%) What are the corresponding  $W$  and  $D$  matrices?
- (d) (5%) Write down the inequality constraints of the integer linear program for a retime function  $r$  satisfying the condition that the clock period  $c \leq 5$  ns.

- (e) (5%) Draw the corresponding constraint graph for the set of inequality constraints in (c).
- (f) (5%) Is there a negative-weighted cycle in the constraint graph? Derive a feasible retiming function if it exists.

(Hint: You may need to create a dummy node for every fanout point.)



**Fig. 3.** A circuit under timing analysis. Assume the arrival times for all of the primary inputs are 0 except for  $x_2$  with arrival time 1ns, the gate delay of a NAND is 2ns, and the gate delay of a NOR is 3ns.)



**Fig. 4.** A circuit under timing optimization, where NOR2, NAND2, and INV are of gate delays 3ns, 2ns and 1ns, respectively. Assume the setup and hold times of the registers are zero.