Switching Circuits & Logic Design

Jie-Hong Roland Jiang 江介宏

Department of Electrical Engineering National Taiwan University



Fall 2013

1

Course Info

- Instructor
 - Jie-Hong R. Jiang
 - office: 242 EEII
 - office hour: 16:00-18:00 Thu
 - email: jhjiang@cc.ee.ntu.edu.tw
 - phone: (02)3366-3685
- Course webpage
 - http://cc.ee.ntu.edu.tw/~jhjiang/instruction/courses/fall 13-ld/ld.html
 - http://access.ee.ntu.edu.tw/course/logic_design_103/in dex.html

Textbook

C. H. Roth, Jr. Fundamentals of Logic Design, 7th edition, Cengage Learning, 2013.

3

Schedule

```
§1 Introduction, Number Systems and Conversion
■ 9/13 §2 Boolean Algebra, §3 Boolean Algebra (Continued)
9/19,20
               -- (Mid-Autumn Festival)
               §4 Applications of Boolean Algebra
9/26
9/27
               §5 Karnaugh Maps
10/3,10/4
               -- (Prof. Jiang out of country)
10/10
               -- (National Day)
10/11
                §5 Karnaugh Maps, §7 Multi-Level Gate Circuits
10/17
               Quiz 1 (§1~§4)
               §7 Multi-Level Gate Circuits
10/18
10/24
               §8 Combinational Circuit Design
10/25
               §9 Multiplexers, Decoders, and PLDs
■ 11/1 Verilog: Combinational Circuits
11/7 --
11/8 Midterm Exam
```

Dates in boldface indicate additional makeup lectures (Thu 13:20-14:10; Fri 17:30-18:20, except for 9/27 17:30-19:20)

Schedule (cont'd)

```
11/14
               §11 Latches and Flip-Flops
11/15
                -- (NTU Anniversary)
                -- (Prof. Jiang out of country)
11/21,22
               §11 Latches and Flip-Flops, §12 Registers and Counters
11/28
11/29
               §12 Registers and Counters, §13 Analysis of Clocked
  Sequential Circuits
               §13 Analysis of Clocked Sequential Circuits
12/5
12/6 §14 Derivation of State Graphs and Tables
12/12
               Quiz 2 (§11~§13)
12/13,19
               §15 Reduction of State Tables (§15.1~2)
               §16 Sequential Circuit Design (§16.1~4)
12/20,26
12/27,1/2
               §18 Ckts for Arithmetic Operations (§18.1~2)
1/3
                Supplementary Materials
1/9
1/10 Final Exam
```

Dates in boldface indicate additional makeup lectures (Thu 13:20-14:10; Fri 17:30-18:20, except for 9/27 17:30-19:20)

Grading

■ Raw score

Homework
Quiz 1
Midterm
Quiz 2
Final
Participation
18%
4%
6%
5%

□ Final letter grade

- Grade on a curve based on the raw scores
- A+: within top 8% among the total student body of four classes

5

Policies

- □ Homework assignments due before lecture
 - 14:10-14:20 on Thursday or 15:20-15:30 on Friday
 - □Late homework penalty: -33% per day
 - Plagiarism strongly prohibited
 - ■No borrowing
 - □ Discussions are strongly encouraged, but solutions need to be written down independently

7

§0 Introduction

Good Old Days of Computation



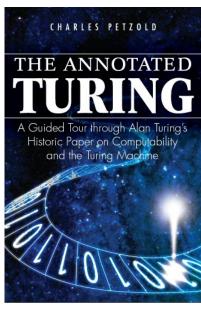


Babbage's difference engine (1822) powered by cranking a handle

9

Good Old Days of Computation

Computability and the Turing machine Alan Turing Cambridge, UK (1937)







Book cover: Wiley (2008)

10

Good Old Days of Computation

- □ ENIAC (1946)
 - First general purpose (Turing-complete) electronic computer
 - Vacuum-tube based implementation

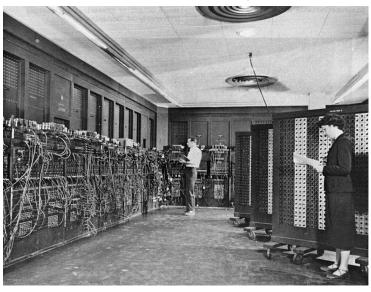


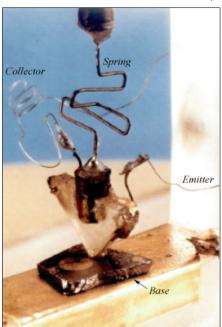


Photo: US Army, Roth audio

Good Old Days of Computation

The first point contact transistor

William Schockley, John Bardeen, and Walter Brattain Bell Laboratories, Murray Hill, New Jersey (1947)





Shockley

Photos: Lucent Technologies

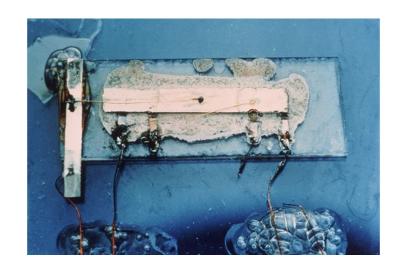
Good Old Days of Computation

The first integrated circuit Jack Kilby (1059)

Texas Instruments, Texas (1958)



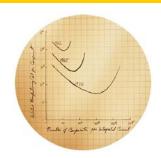


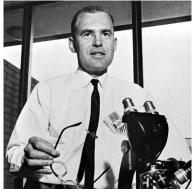


Photos: Texas Instructments

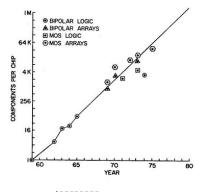
13

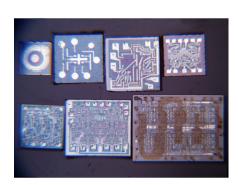
Roadmap of VLSI Design

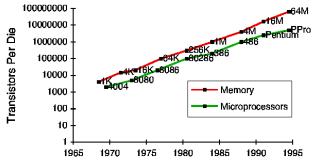




Gordon Moore at Fairchild (1962)





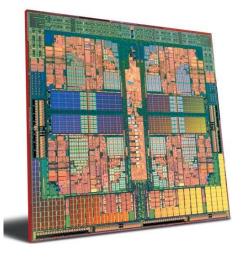


Photos: Intel

14

VLSI Design Nowadays

MPUs with billions of transistors



Systems with powerful capabilities



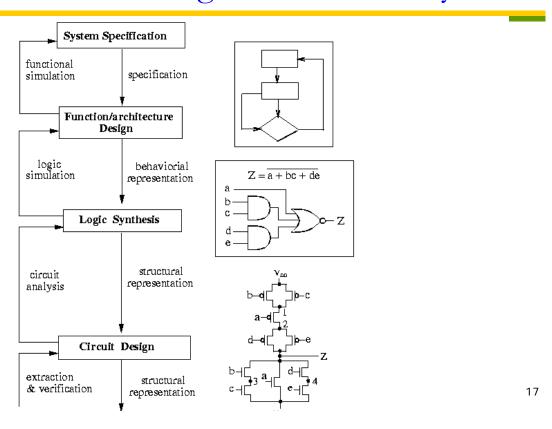
Photo: AMD; Apple

15

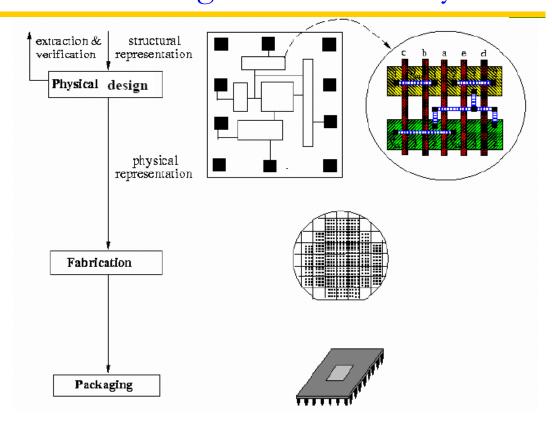
Cope with Complex Designs

- ■Proper design abstraction
 - E.g., treating digital circuits as switches
- Module-based design
- Design reuse
- Design automation
 - Computer-Aided Design (CAD) tools

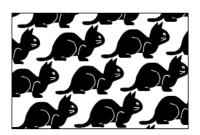
How to Build Digital Electronic Systems?



How to Build Digital Electronic Systems?



The World of **0** and **1**

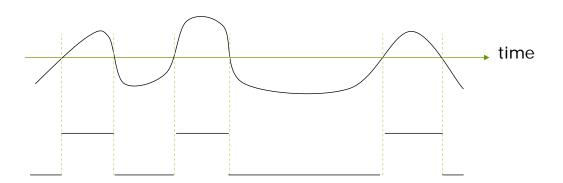


19

People to Know

- □ George Boole
 - Logic + algebra → Boolean algebra
- □Claude E. Shannon
 - Boolean algebra ↔ switching circuits

Digital vs. Analog



21

Digital vs. Analog

- Digital
 - Discrete in value
 - More artificial
 - Immune to noise
 - Easy error correction
 - Easy precision control
 - Easy design automation
 - Slow computation

- Analog
 - Continuous value
 - Closer to physical world
 - Vulnerable to noise
 - Hard error correction
 - Hard precision control
 - Hard design automation
 - Fast computation

Binary vs. Multi-Valued

- □ A digital system can be binary or multi-valued
 - Binary:

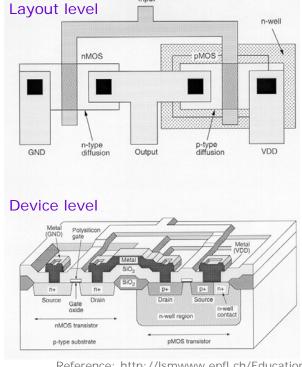
Signals with 2 values, e.g., {on, off}, {0,1},...

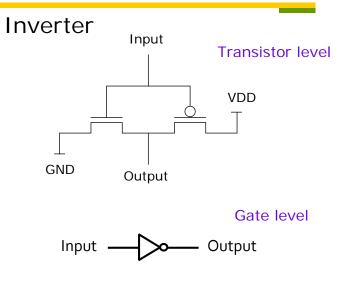
- Multi-valued:
 - Signals with > 2 values, e.g., {red, green, yellow}, {0,1,2,3}, ...
- Binary systems are still the most popular design choice
 - ☐ Simple and fast operations
 - ☐ Higher noise immunity

23

24

Digital Circuits and Boolean Algebra





Input Output

0 1
1 0

Switching Circuits and Logic Design

- This course is about digital circuit design at the gate level
 - Signals that we encounter are of {0,1} Boolean values
 - We will apply Boolean algebra to logic design
- Other applications
 - Biological network analysis and design
 - Gene regulatory networks can be abstracted as Boolean circuits
 - Non-conventional computation systems
 - E.g., quantum circuit design

25

Do You Know?

- ■What does "bit" stand for?
 - Binary Digit
- □ Who coined the term?
 - John Tukey (best known for his FFT algorithm)
- ■Who popularized the term?
 - Claude Shannon (in his famous paper entitled "A Mathematical Theory of Communication")