Logic Synthesis & Verification, Fall 2013

National Taiwan University

Problem Set 5

Due on 2013/12/27 17:30
(Please put your solution in the instructor's mailbox at EE2 Building.)

1 Factored Form

(a) (10%) Show that any factored form expression can be translated into a CMOS gate of $2n$ transistors. (Note that an inverter can be appended at the output with a total of $2n+2$ transistors.)

(b) (10%) Give an example of a CMOS gate with some constant $2k$ transistors (assuming each transistor has to be controlled by some input variable) such that its function cannot be expressed in any factored form of less than k literals. (Just need to show the NMOS network if you don't know how to construct its corresponding complementary PMOS network.)

2 Weak Division

(10%) Given an expression F and a divisor G, suppose $F = G \cdot H + R$ by weak division. Prove that H and R are unique.

3 [Kernelling and Factoring]

(10%) Consider the expression $F =$

$$abdh+abdi+abeh+abei+ah+ai+bf+cdh+cdi+ceh+cei+fgi+fh+fi+gh+gi.$$

Compute $\texttt{KERNEL}(0, F)$ with literals ordered alphabetically. Draw the kernelling tree (as in the slides) and list the kernels and their corresponding co-kernels.

4 [SDC and ODC]

(15%) Consider the Boolean network of Figure 1.

(a) Write down a Boolean formula for the SDC of the entire network.

(b) Write down a Boolean formula for the satisfiability don't cares SDC_4 of Node 4. Since SDC_4 is imposed by the fanins of Node 4, the formula should depend on variables $x_1, \ldots, x_4, y_1, \ldots, y_3$. How can you make SDC_4 only depend on y_1, y_2, y_3 such that we can minimize Node 4 directly?

(c) Compute the observability don't cares ODC_4 of Node 4.

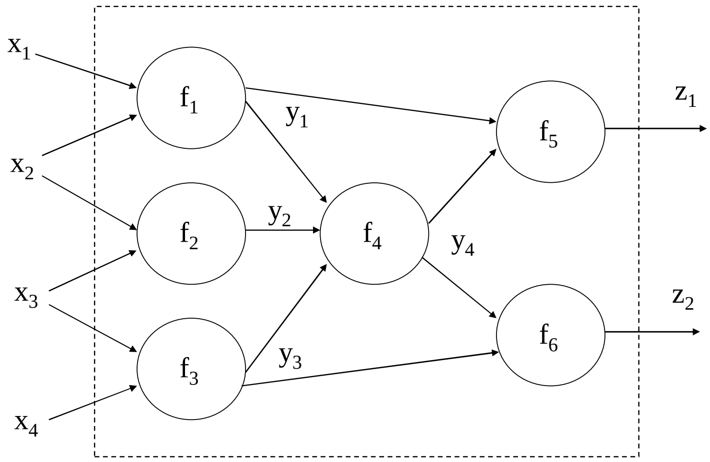

Fig. 1. A Boolean network, where $f_1 = x_1 \vee \neg x_2$, $f_2 = \neg x_2 \wedge x_3$, $f_3 = \neg x_3 \wedge x_4$, $f_4 = (\neg y_1 \wedge \neg y_2 \wedge y_3) \vee (\neg y_1 \wedge y_2 \wedge \neg y_3) \vee (y_1 \wedge \neg y_2 \wedge \neg y_3) \vee (y_1 \wedge y_2 \wedge y_3)$, $f_5 = y_1 \vee y_4$, and $f_6 = y_3 \wedge y_4$.

5 [Don't Cares in Local Variables]

(20%) Consider the Boolean network of Figure 1. Suppose the XDC for z_1 is $\neg x_1 \neg x_2 \neg x_3 x_4$ and that for z_2 is $x_1 x_2 \neg x_3 x_4$.

(a) Compute the don't cares D_4 of Node 4 in terms of its local input variables y_1, y_2, and y_3. (Note that in general the computation of ODC may be affected by XDC especially when there exist different XDCs for different primary outputs.)
(b) Based on the computed don't cares, what is the best implementable function for Node 4 (in terms of the literal count and cube count in SOP)?

6 [Complete Flexibility]

(25%) Consider the Boolean network of Figure 1. Let $Y = \{y_1, y_2, y_3\}$.

(a) Suppose the XDC for z_1 is $\neg x_1 \neg x_2 \neg x_3 x_4$ and that for z_2 is $x_1 x_2 \neg x_3 x_4$. Write down the specification relation $S(X, Z)$.
(b) What is the influence relation $I(X, y_4, Z)$ of Node 4?
(c) What is the environment relation $E(X, Y)$ of Node 4?
(d) What is the complete flexibility $CF_4(Y, y_4)$ of Node 4?
(e) Is the previously computed don't care set D_4 of Node 4 subsumed by CF_4?