Logic Synthesis & Verification, Fall 2014

National Taiwan University

Problem Set 6

Due on 2014/1/12 18:00. (Please turn in your solutions in the instructor's mailbox.)

1 [Technology Mapping]

(a) (10%) What are the criteria that make a collection of pattern graphs a legal cover of technology mapping?
(b) (10%) Given the subject graph of Figure 1, perform dynamic programming to find an optimum tree mapping solution using the pattern graphs of Figure 2. Show intermediate costs and the final optimum tree covering.

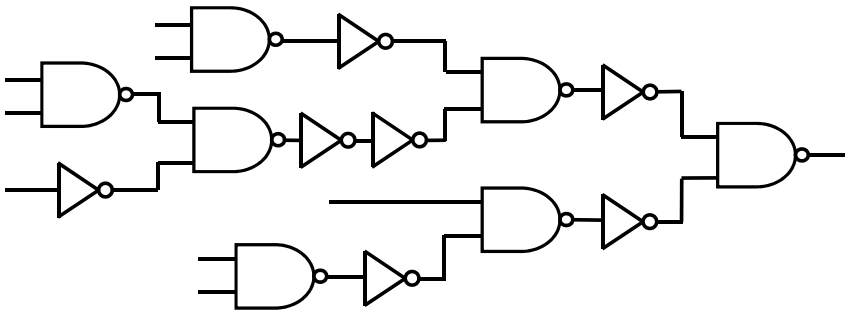

Fig. 1. Subject graph

2 [Timing Analysis]

(a) (10%) Given the circuit of Figure 3, compute the *arrival time*, *required time*, and *slack* of every net assuming the required times for the primary output are 8ns. Identify the critical region (consisting of gates and wires) with negative slacks.
(b) (10%) Prove that the region with slack less than or equal to some constant c for a given circuit must consist of paths from primary inputs to primary outputs.
(c) (10%) Given the circuit of Figure 3, perform the SAT-based functional timing analysis to compute the longest true delay.

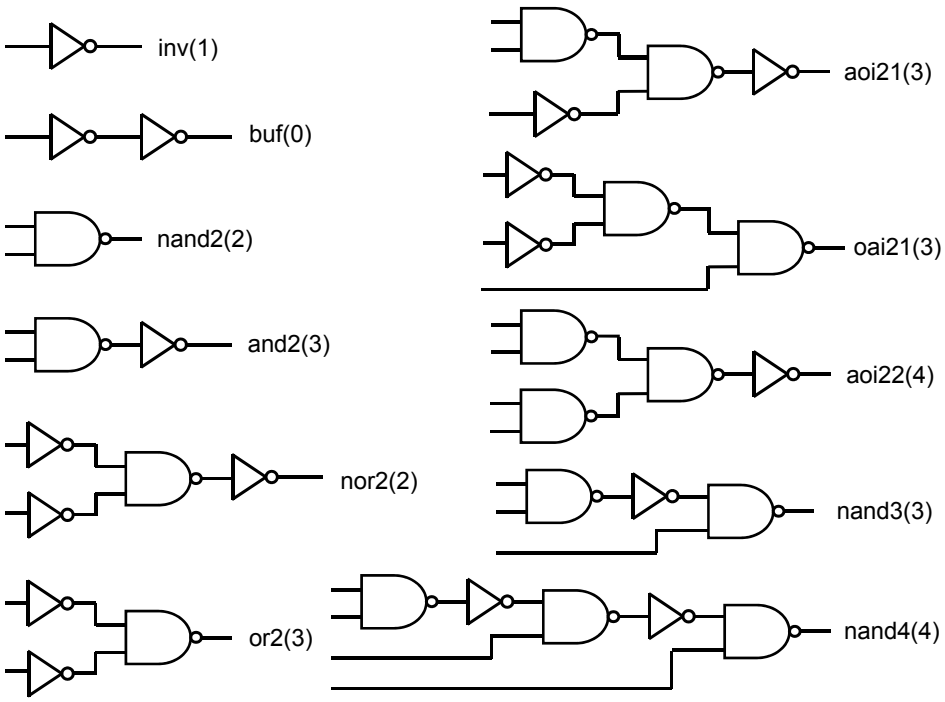

Fig. 2. Pattern graphs.

3 [Clock Skew Scheduling and Retiming]

Consider the circuit of Figure 4.

(a) (8%) What is the minimum clock period achievable by clock skew scheduling? What are the corresponding skews of r_2, r_3, and r_4 (with respect to the clock edge of r_1)?
(b) (4%) Draw the corresponding retiming graph. (You may need to create a dummy node for every fanout point.)
(c) (4%) What are the corresponding W and D matrices?
(d) (4%) Write down the inequality constraints of the integer linear program for a retime function r satisfying the condition that the clock period $c \leq 5$ ns.
(e) (4%) Draw the corresponding constraint graph for the set of inequality constraints in (c).
(f) (4%) Is there a negative-weighted cycle in the constraint graph? Derive a feasible retime function if it exists.

4 [Sequential Equivalence Checking]

Given two FSMs M_1 and M_2, the transition and output functions of M_1 are

$$\delta_1(x, s) = s, \text{ and}$$

$$\lambda_1(x, s) = x \oplus s,$$

respectively; those of M_2 are

$$\begin{aligned} \delta_{2,0}(x, t_0, t_1) &= t_0 \oplus t_1, \\ \delta_{2,1}(x, t_0, t_1) &= x \oplus \delta_{2,0}, \text{ and} \\ \lambda_2(x, t_0, t_1) &= \delta_{2,1}, \end{aligned}$$

respectively. (Note that x is the input variable, s is the state variable of M_1, and t_0, t_1 are the state variables of M_2.) Let $\neg s$ and $\neg t_0 \neg t_1$ be the characteristic functions of the initial states of M_1 and M_2, respectively.

(a) (4%) What are the transition and output functions of the product machine $M_{1\times 2}$ of M_1 and M_2? What is the initial state of $M_{1\times 2}$ in terms of a characteristic function?
(b) (4%) Let s', t_0', t_1' be the corresponding next-state variables of s, t_0, t_1, respectively. Write down the Boolean expression for the transition relation $T(s, t_0, t_1, s', t_0', t_1')$ of $M_{1\times 2}$.
(c) (7%) Perform **forward** reachability analysis using transition relation T. Show the reached state set at each iteration.
(d) (7%) Are M_1 and M_2 equivalent? Conclude the equivalence using the computed characteristic functions. What if the initial states of M_1 and M_2 are $\neg s$ and $t_0 t_1$, respectively, instead?

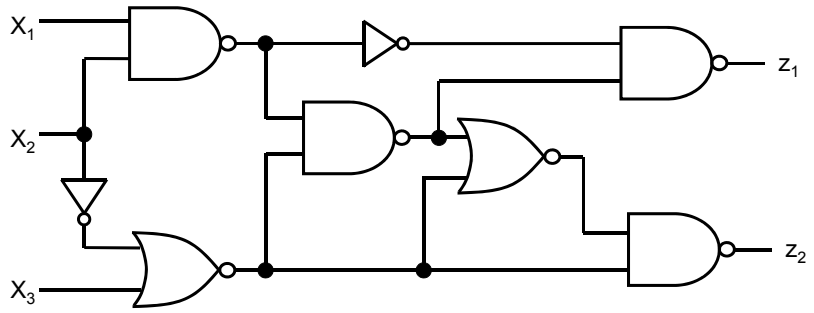

Fig. 3. A circuit under timing analysis. Assume the arrival times for all of the primary inputs are 0, the gate delay of an inverter is 1ns, a NAND gate is 2ns, and the gate delay of a NOR gate is 3ns.)

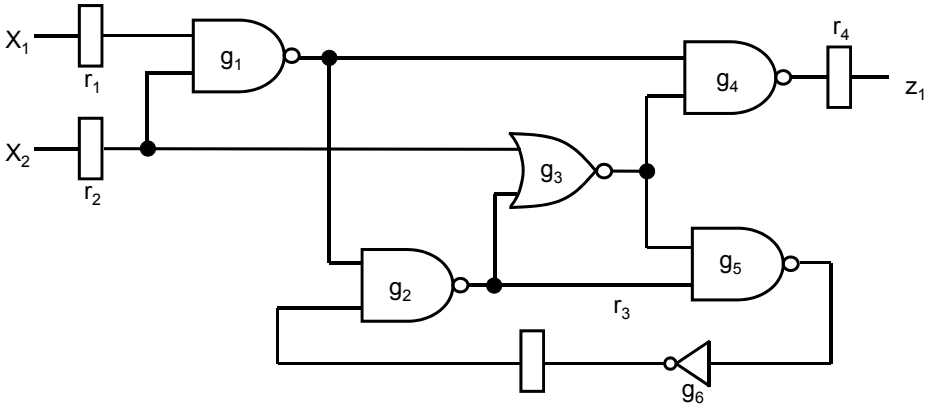

Fig. 4. A circuit under timing optimization, where NOR2, NAND2, and INV are of gate delays 3ns, 2ns and 1ns, respectively. Assume the setup and hold times of the registers are 0.