

Introduction to Electronic Design Automation

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Spring 2012

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Design Automation?



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Course Info (1/4)

Instructor

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Email contact list

NTU email addresses of enrolled students will be used for future contact

Course webpage

<http://cc.ee.ntu.edu.tw/~jhjiang/instruction/courses/spring12-eda/eda.html>
please look up the webpage frequently to keep updated

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Course Info (2/4)

Grading rules

- Homework 40%
- Midterm 25%
- Final exam or project (either option) 30%
- Course participation 5%

Homework

- discussions encouraged, but solutions should be written down individually and separately
- 4~5 assignments in total
- late homework (20% off per day)

Midterm/final exams

- in-class exam

Project

- Team or individual work on selected topics (paper reading / implementation / problem solving, etc.)

Academic integrity: no plagiarism allowed

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Course Info (3/4)

□ Prerequisite

- Switching circuits and logic design, or by instructor's consent

□ Main lecture basis

- Lecture slides and/or handouts

□ Textbook

- Y.-W. Chang, K.-T. Cheng, and L.-T. Wang (Editors). *Electronic Design Automation: Synthesis, Verification, and Test*. Elsevier, 2009.

□ Reference

- S. H. Gerez. *Algorithms for VLSI Design Automation*. John Wiley & Sons, 1999.

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Course Info (4/4)

□ Objectives:

- Peep into EDA
- Motivate interests
- Learn problem formulation and solving
- Have fun!

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FYI

- 2012 CAD Contest will be announced soon
 - It will be an international competition
 - Submission deadline in September(?)

- 九十九學年度大學校院積體電路電腦輔助設計 (CAD)軟體製作競賽
 - http://cad_contest.cs.nctu.edu.tw/cad11/

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FAQ

- What's EDA?
 - What are we concerned about?
 - What's unique in EDA compared to other EE/CS disciplines?

- What time is good to take *Intro to EDA*?
 - Am I qualified? Do I have enough backgrounds?

- How's the loading?
 - Program to death!?

- What kind of skills and domain knowledge can I learn? Other applications?

- What are the career opportunities?

- Yet another question?

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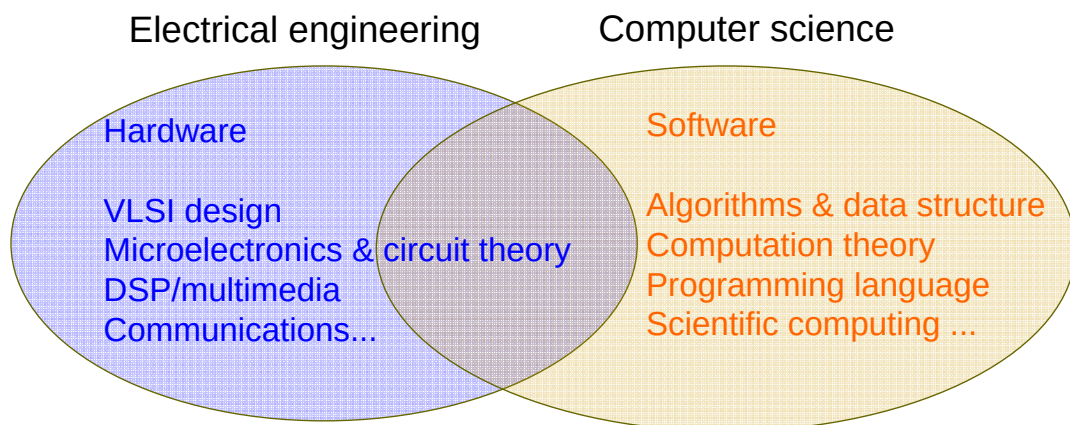
Course Outline

- Introduction
- Computation in a nutshell
- High-level synthesis
- Logic synthesis
- Formal verification
- Physical design
- Testing
- Simulation
- Advanced topics

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Introduction

- EDA, where HW and SW meet each other



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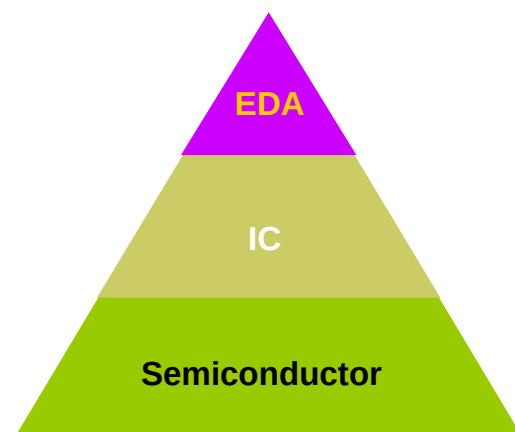
Introduction

- EDA is concerned about HW/SW design in terms of
 - Correctness
 - Productivity
 - Optimality
 - Scalability

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Introduction

- EDA (in a strict sense) and industries
 - Impact - solving a problem may benefit vast electronic designs



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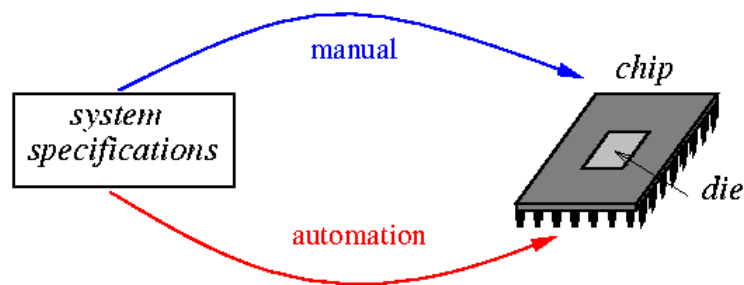
Introduction

□ Today's contents:

- Introduction to VLSI design flow, methodologies, and styles
- Introduction to VLSI design automation tools
- Semiconductor technology roadmap
- CMOS technology

□ Reading:

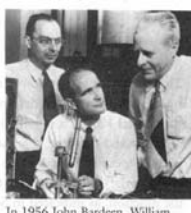
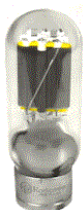
- Chapters 1, 2



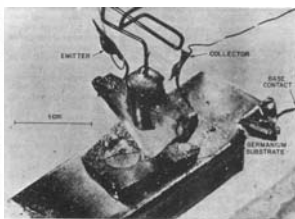
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Milestones of IC Industry

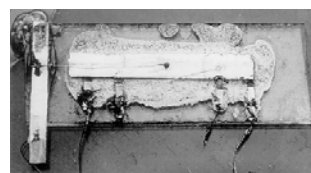
- **1947:** Bardeen, Brattain & Shockly invented the transistor, foundation of the IC industry.
- **1952:** SONY introduced the first transistor-based radio.
- **1958:** Kilby invented integrated circuits (ICs).
- **1965:** Moore's law.
- **1968:** Noyce and Moore founded Intel.
- **1970:** Intel introduced 1 K DRAM.



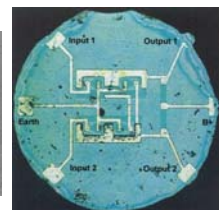
In 1956 John Bardeen, William Shockley and Walter Brattain shared the Nobel Prize in Physics for their discovery of the transistor.



First transistor



First IC by Kilby



First IC by Noyce

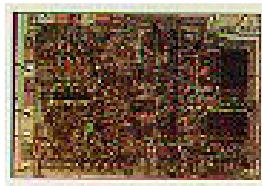
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Milestones of IC Industry

- ❑ **1971:** Intel announced 4-bit 4004 microprocessors (2250 transistors).
- ❑ **1976/81:** Apple II/IBM PC.
- ❑ **1985:** Intel began focusing on microprocessor products.
- ❑ **1987:** TSMC was founded (**fabless** IC design).
- ❑ **1991:** ARM introduced its first embeddable RISC IP core (**chipless** IC design).



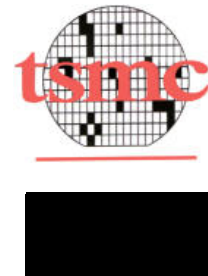
Intel founders



4004



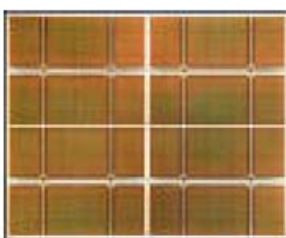
IBM PC



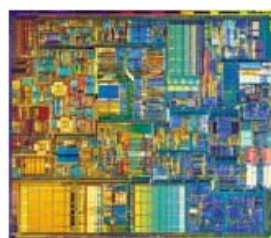
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Milestones of IC Industry

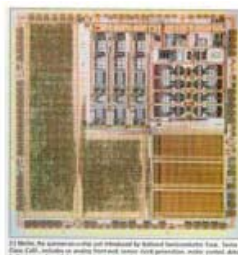
- ❑ **1996:** Samsung introduced 1G DRAM.
- ❑ **1998:** IBM announces 1GHz experimental microprocessor.
- ❑ **1999/earlier:** **System-on-Chip (SoC)** methodology applications.
- ❑ **2002/earlier:** **System-in-Package (SiP)** technology
- ❑ An Intel P4 processor contains 42 million transistors (1 billion by 2005)
- ❑ Today, we produce > 30 million transistors per person (1 billion/person by 2008).



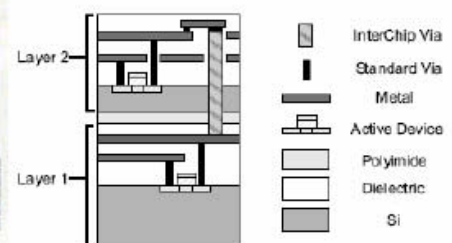
4GB DRAM (2001)



Pentium 4



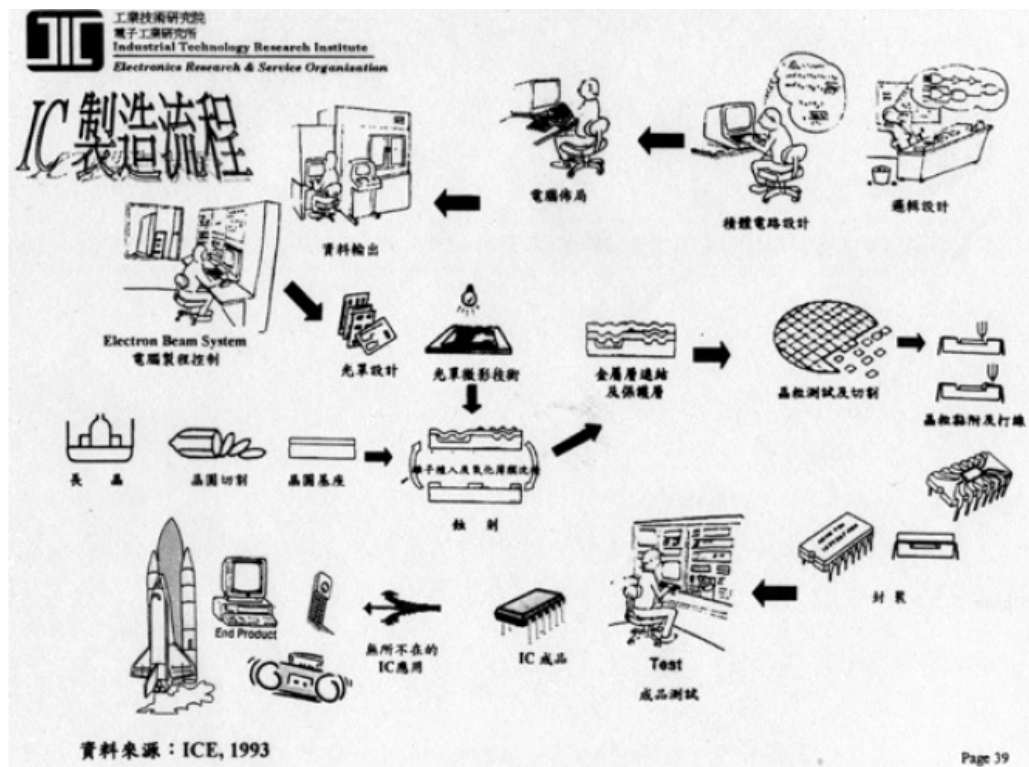
Scanner-on-chip



System in Package (SiP)

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IC Design & Manufacturing Process



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From Wafer to Chip

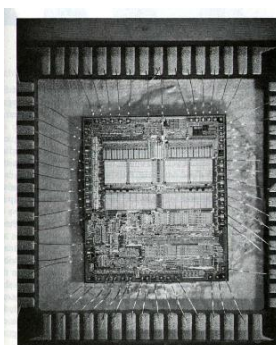
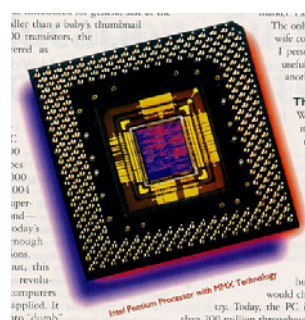


Figure 9.34
Attachment of leads
from the Al pads
on the periphery of
the chip to posts
on the package.
(Photograph
courtesy of
Motorola, Inc.)



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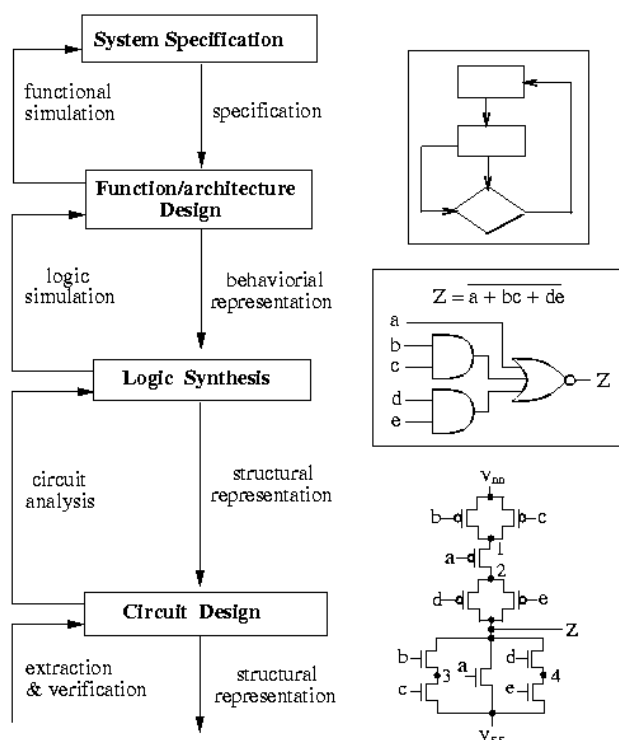
Standard VLSI Design Cycles

1. System specification
2. Functional design
3. Logic synthesis
4. Circuit design
5. Physical design and verification
6. Fabrication
7. Packaging

- Other tasks involved: testing, simulation, etc.
- Design metrics: area, speed, power dissipation, noise, design time, testability, etc.
- Design revolution: interconnect (not gate) delay dominates circuit performance in deep submicron era.
 - Interconnects are determined in physical design.
 - Shall consider interconnections in early design stages.

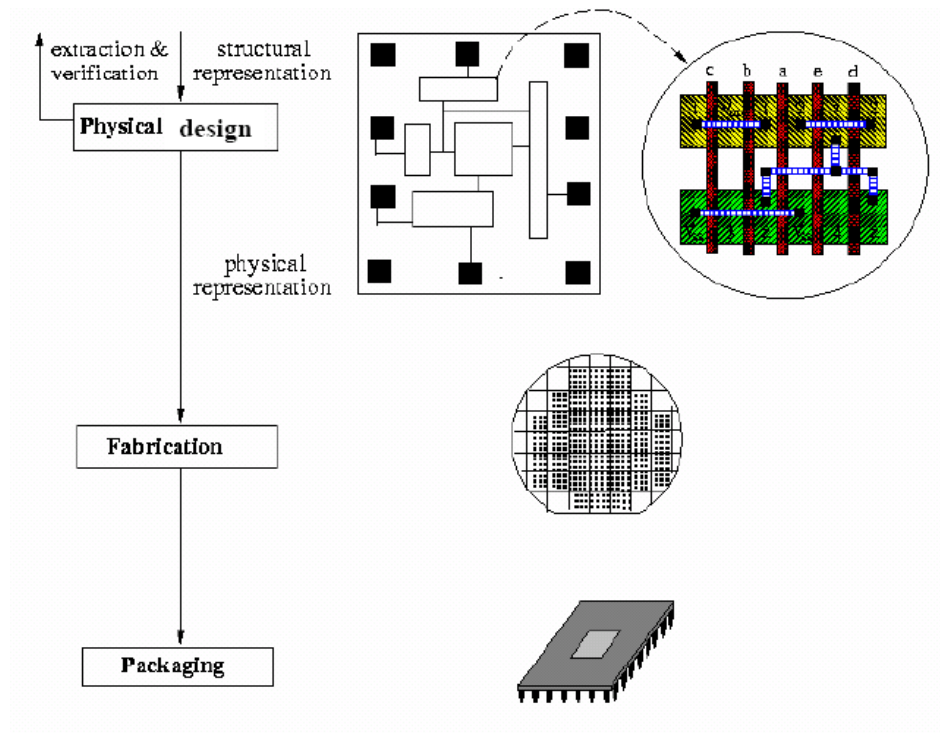
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VLSI Design Flow



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VLSI Design Flow



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Design Actions

- ❑ **Synthesis:** increasing information about the design by providing more detail (e.g., logic synthesis, physical synthesis).
- ❑ **Analysis:** collecting information on the quality of the design (e.g., timing analysis).
- ❑ **Verification:** checking whether a synthesis step has left the specification intact (e.g., function, layout verification).
- ❑ **Optimization:** increasing the quality of the design by rearrangements in a given description (e.g., logic optimizer, timing optimizer).
- ❑ **Design management:** storage of design data, cooperation between tools, design flow, etc. (e.g., database).

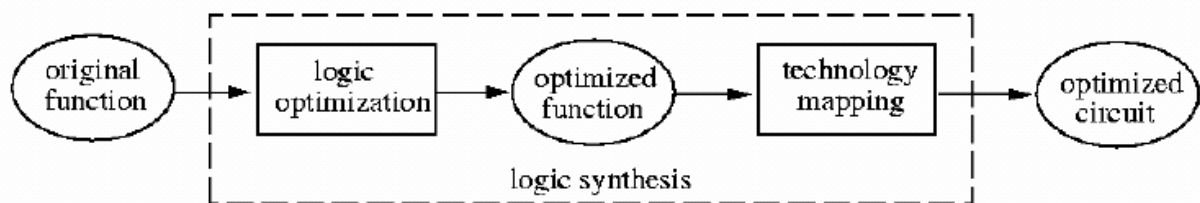
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Design Issues and Tools

- ❑ System-level design
 - Partitioning into hardware and software, co-design/simulation etc.
 - Cost estimation, design-space exploration
- ❑ Algorithmic-level design
 - Behavioral descriptions (e.g. in Verilog, VHDL)
 - High-level simulation
- ❑ From algorithms to hardware modules
 - High-level (or architectural) synthesis
- ❑ Logic design:
 - Register-transfer level and logic synthesis
 - Gate-level simulation (functionality, power, etc)
 - Timing analysis
 - Formal verification

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Logic Design/Synthesis



- ❑ **Logic synthesis** programs transform Boolean expressions into logic gate networks in a particular library.
- ❑ Optimization goals: minimize area, delay, power, etc
- ❑ **Technology-independent** optimization: logic optimization
 - Optimizes Boolean expression equivalent.
- ❑ **Technology-dependent** optimization: **technology mapping/library binding**
 - Maps Boolean expressions into a particular cell library.

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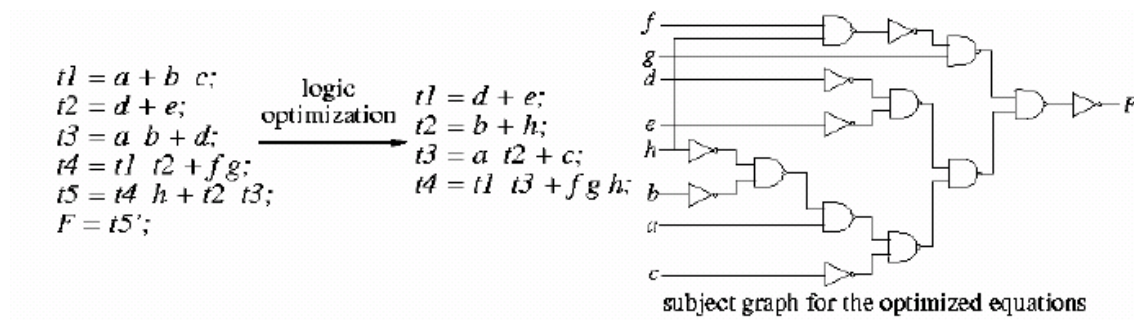
Logic Optimization Examples

- **Two-level:** minimize the # of product terms.

- $F = \bar{x}_1\bar{x}_2\bar{x}_3 + \bar{x}_1\bar{x}_2x_3 + x_1\bar{x}_2\bar{x}_3 + x_1\bar{x}_2x_3 + x_1x_2\bar{x}_3 \Rightarrow F = \bar{x}_2 + x_1\bar{x}_3.$

- **Multi-level:** minimize the #'s of literals, variables.

- E.g., equations are optimized using a smaller number of literals.



- Methods/CAD tools: Quine-McCluskey method (exponential-time exact algorithm), Espresso (heuristics for two-level logic), SIS (heuristics for multi-level logic), ABC, etc.

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Design Issues and Tools (cont'd)

- Transistor-level design
 - Switch-level simulation
 - Circuit simulation
- Physical (layout) design:
 - Partitioning
 - Floorplanning and placement
 - Routing
 - Layout editing and compaction
 - Design-rule checking
 - Layout extraction
- Design management
 - Data bases, frameworks, etc.
- **Silicon compilation:** *from algorithm to mask patterns*
 - The *idea* is approached more and more, but still far away from a single *push-button* operation

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Circuit Simulation

```
M1 3 2 0 0 nch W=1.2u L=0.6u AS=2.16p PS=4.8u AD=2.16p PD=4.8u
M2 3 2 1 1 pch W=1.8u L=0.6u AS=3.24p PS=5.4u AD=3.24p PD=5.4u
CL 3 0 0.2pF
```

```
VDD 1 0 3.3
```

```
VIN 2 0 DC 0 PULSE (0 3.3 0ns 100ps 100ps 2.4ns 5ns)
```

```
.LIB '../mod.06' typical
```

```
.OPTION NOMOD POST INGOLD=2 NUMDGT=6 BRIEF
```

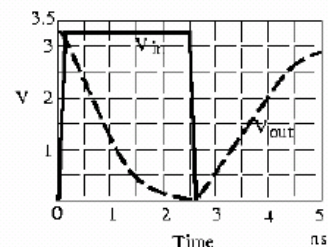
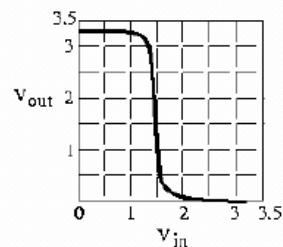
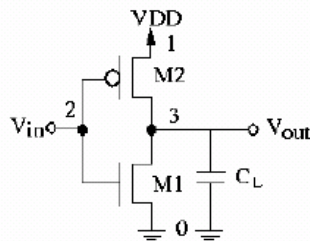
```
.DC VIN 0V 3.3V 0.001V
```

```
.PRINT DC V(3)
```

```
.TRAN 0.001N 5N
```

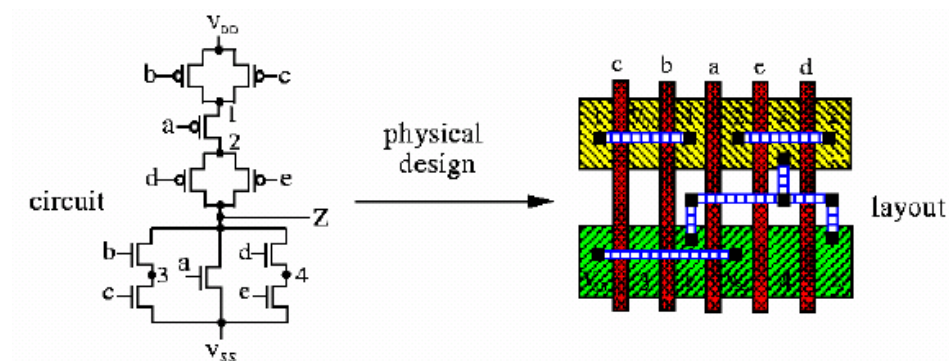
```
.PRINT TRAN V(2) V(3)
```

```
.END
```



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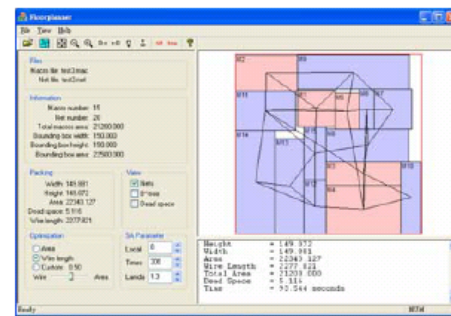
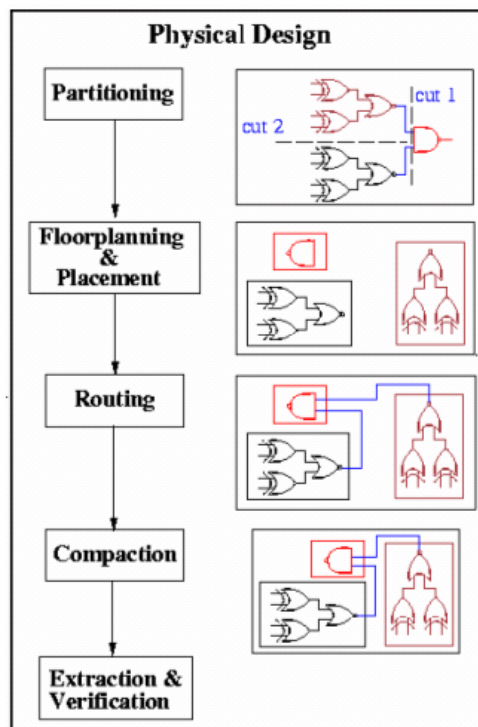
Physical Design



- Physical design converts a circuit description into a geometric description.
- The description is used to manufacture a chip.
- Physical design cycle:
 1. Logic partitioning
 2. Floorplanning and placement
 3. Routing
 4. Compaction
- Others: circuit extraction, timing verification and design rule checking

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Physical Design Flow



B*-tree based floorplanning system

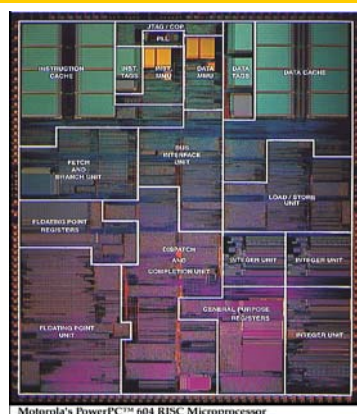


A routing system

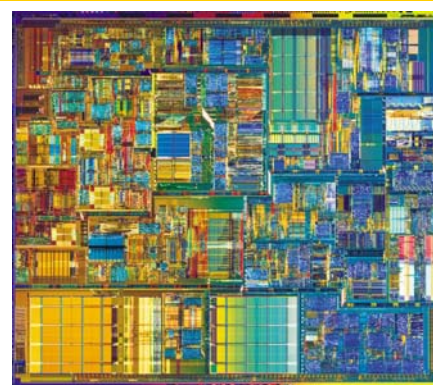
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Floorplan Examples

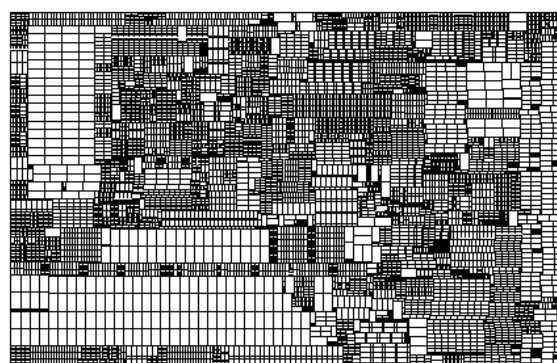
PowerPC 604



Pentium 4



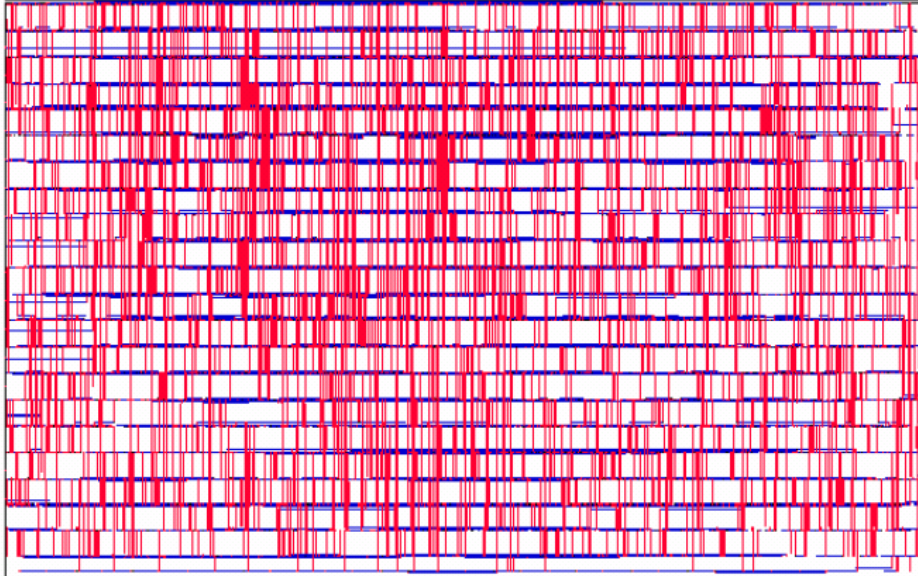
A floorplan with 9800 blocks



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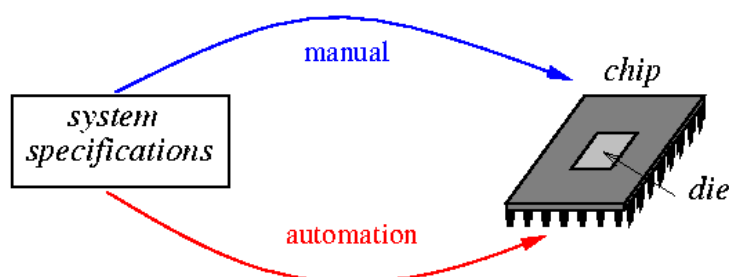
Routing Example

- 0.18um technology, two layers, pitch = 1 um, 8109 nets



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IC Design Considerations

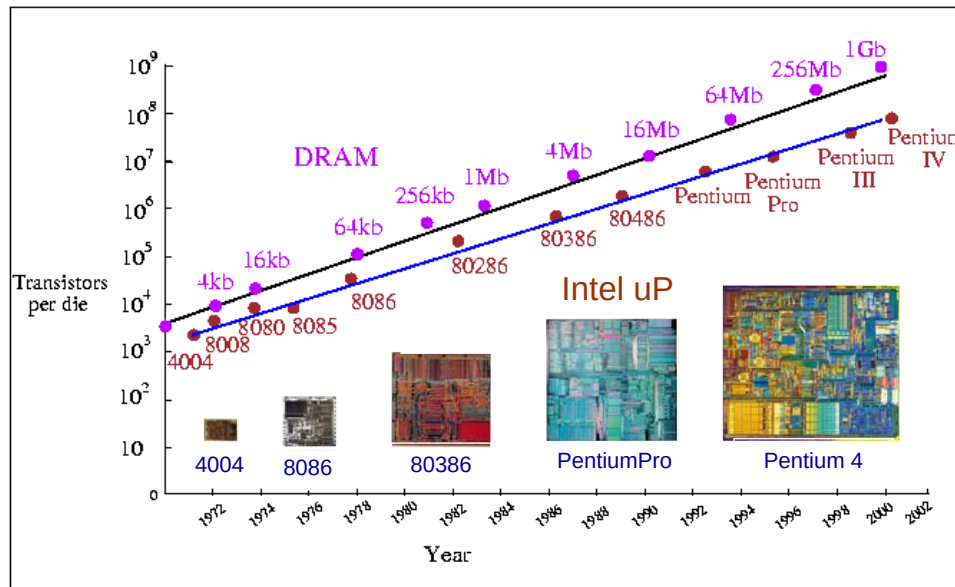


- Several conflicting considerations:
 - Design complexity:** large number of devices/transistors
 - Performance:** optimization requirements for high performance
 - Time-to-market:** about a 15% gain for early birds
 - Cost:** die **area**, packaging, testing, etc.
 - Others: power, signal integrity (noise, etc), testability, reliability, manufacturability, etc.

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Moore's Law: Driving Technology Advances

- Logic capacity doubles per IC at a regular interval
 - Moore: Logic capacity doubles per IC every two years (1975)
 - D. House: Computer performance doubles every 18 months (1975)



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Technology Roadmap for Semiconductors

Year	1997	1999	2002	2005	2008	2011	2014
Technology node (nm)	250	180	130	100	70	50	35
On-chip local clock (GHz)	0.75	1.25	2.1	3.5	6.0	10	16.9
Microprocessor chip size (mm ²)	300	340	430	520	620	750	901
Microprocessor transistors/chip	11M	21M	76M	200M	520M	1.40B	3.62B
Microprocessor cost/transistor ($\times 10^{-8}$ USD)	3000	1735	580	255	110	49	22
DRAM bits per chip	256M	1G	4G	16G	64G	256G	1T
Wiring level	6	6-7	7	7-8	8-9	9	10
Supply voltage (V)	1.8-2.5	1.5-1.8	1.2-1.5	0.9-1.2	0.6-0.9	0.5-0.6	0.37-0.42
Power (W)	70	90	130	160	170	175	183

- Source: International Technology Roadmap for Semiconductors, Nov, 2002. <http://www.itrs.net/ntrs/publntrs.nsf>
- Deep submicron technology: node (**feature size**) < $0.25 \mu\text{m}$
- Nanometer Technology: node < $0.1 \mu\text{m}$

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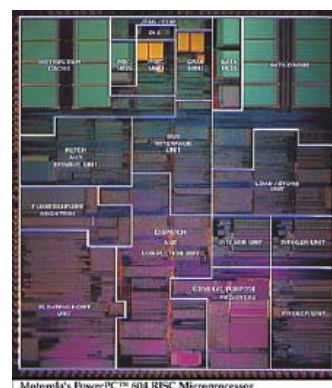
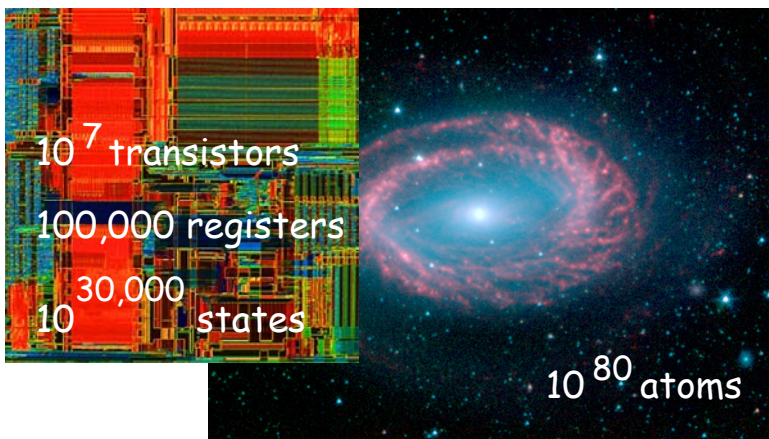
Nanometer Design Challenges

- ❑ In 2005, feature size $\approx 0.1 \mu m$, μP frequency ≈ 3.5 GHz, die size $\approx 520 \text{ mm}^2$, μP transistor count per chip $\approx 200M$, wiring level ≈ 8 layers, supply voltage ≈ 1 V, power consumption ≈ 160 W.
 - **Chip complexity**
 - ❑ effective design and verification methodology? more efficient optimization algorithms? time-to-market?
 - **Power consumption**
 - ❑ power & thermal issues?
 - **Supply voltage**
 - ❑ signal integrity (noise, IR drop, etc)?
 - **Feature size, dimension**
 - ❑ sub-wavelength lithography (impacts of process variation)? noise? wire coupling? reliability? manufacturability? 3D layout?
 - **Frequency**
 - ❑ interconnect delay? electromagnetic field effects? timing closure?

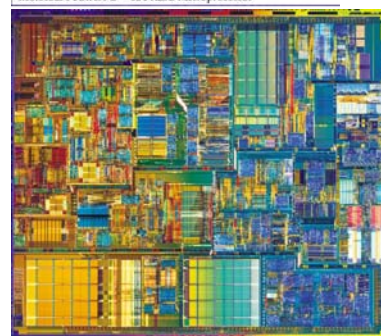
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Design Complexity Challenges

- ❑ Design issues
 - Design space exploration
 - More efficient optimization algorithms
- ❑ Verification issues
 - State explosion problem
 - For modern designs, about 60%-80% of the overall design time was spent on verification; 3-to-1 head count ratio between verification engineers and logic designers



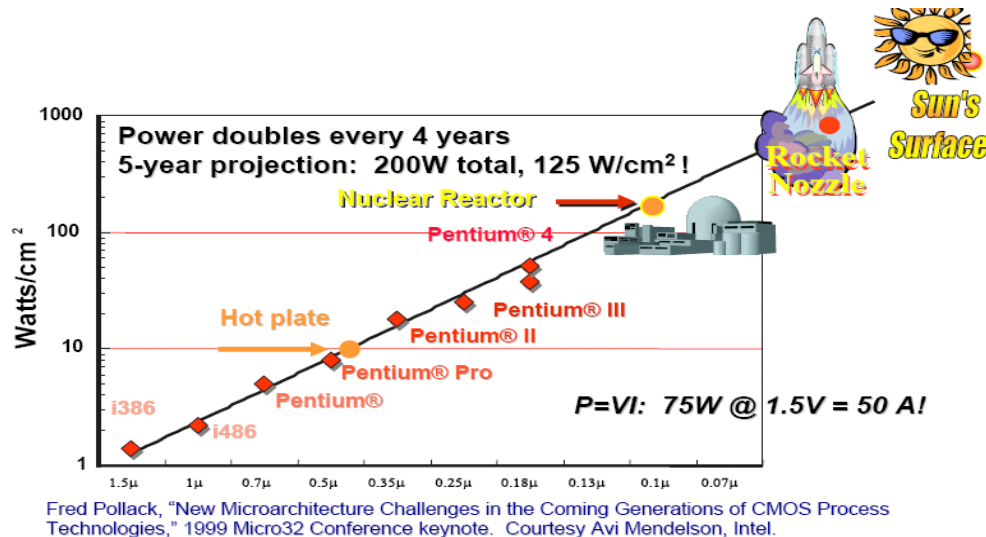
PowerPC 604



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Power Dissipation Challenges

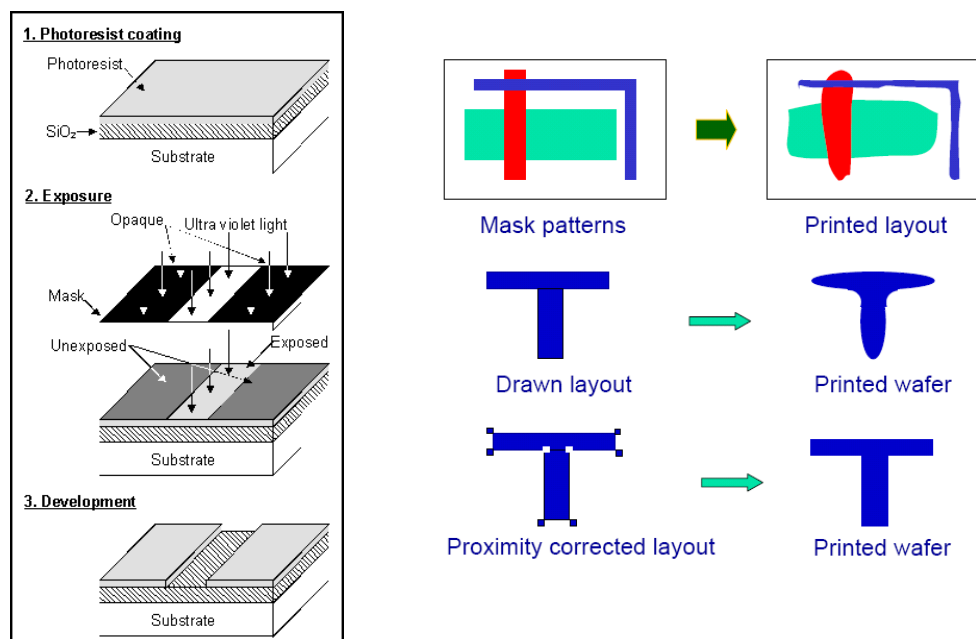
- Power density increases exponentially!



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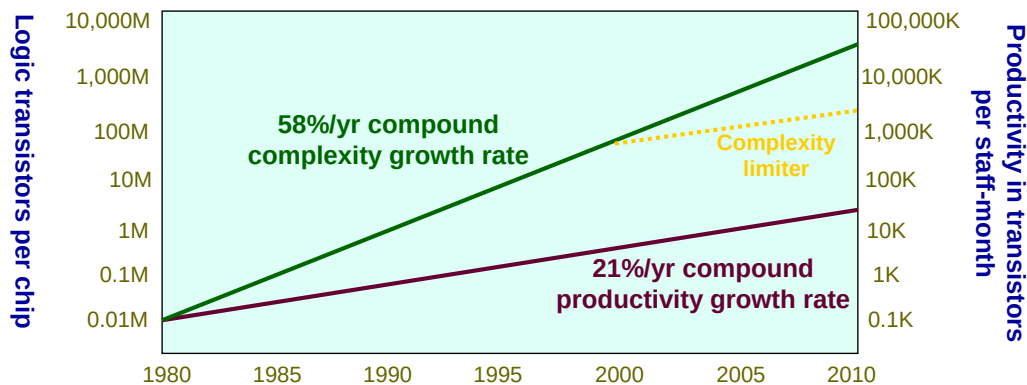
Semiconductor Fabrication Challenges

- Feature-size shrinking approaches physical limitation



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Design Productivity Challenges

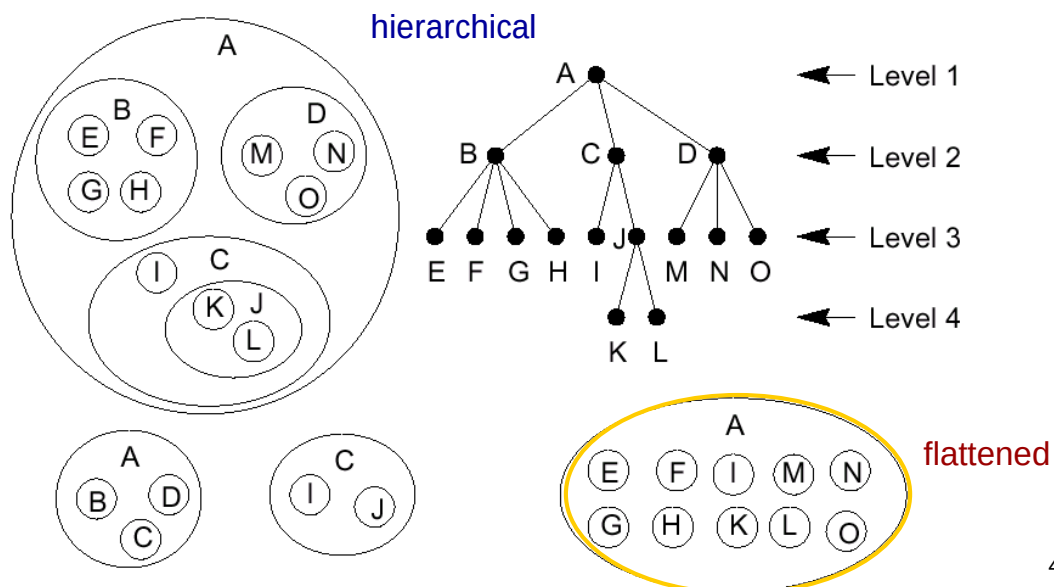


- Human factors may limit design more than technology
- Keys to solve the productivity crisis: **hierarchical design**, **abstraction**, **CAD (tool & methodology)**, IP reuse, etc.

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Cope with Complexity

- **Hierarchical design**
 - Design cannot be done in one step $\Rightarrow$ partition the design hierarchically
 - *Hierarchy*: something is composed of simpler things

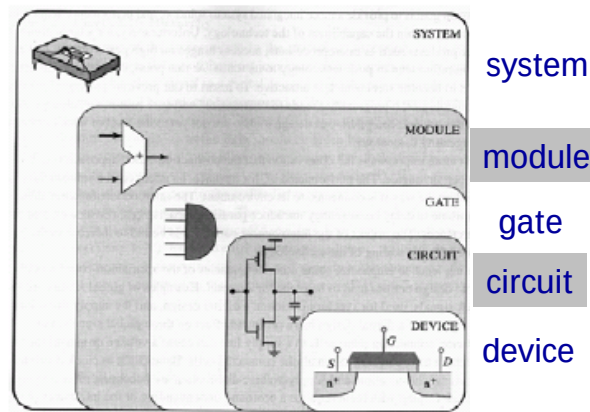


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Cope with Complexity

□ Abstraction

- Trim away unnecessarily detailed info at proper abstract levels
- Design domains:
 - *Behavioral*: black box view
 - *Structural*: interconnection of subblocks
 - *Physical*: layout properties
 - Each design domain has its own hierarchy



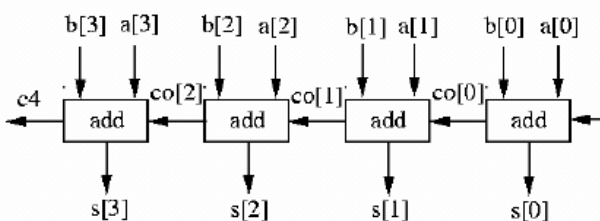
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Three Design Views

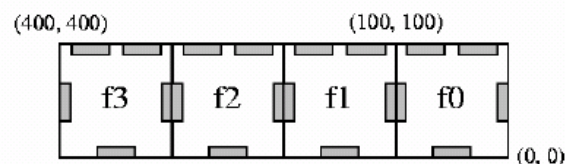
Behavior

```
module add4 (s, c4, ci, a, b);
  input [3:0] a, b;
  input ci;
  output [3:0] s;
  output c4;
  wire [2:0] co;
  add f0 (co[0], s[0], a[0], b[0], ci);
  add f1 (co[1], s[1], a[1], b[1], co[0]);
  add f2 (co[2], s[2], a[2], b[2], co[1]);
  add f3 (c4, s[3], a[3], b[3], co[2]);
endmodule
```

Structural

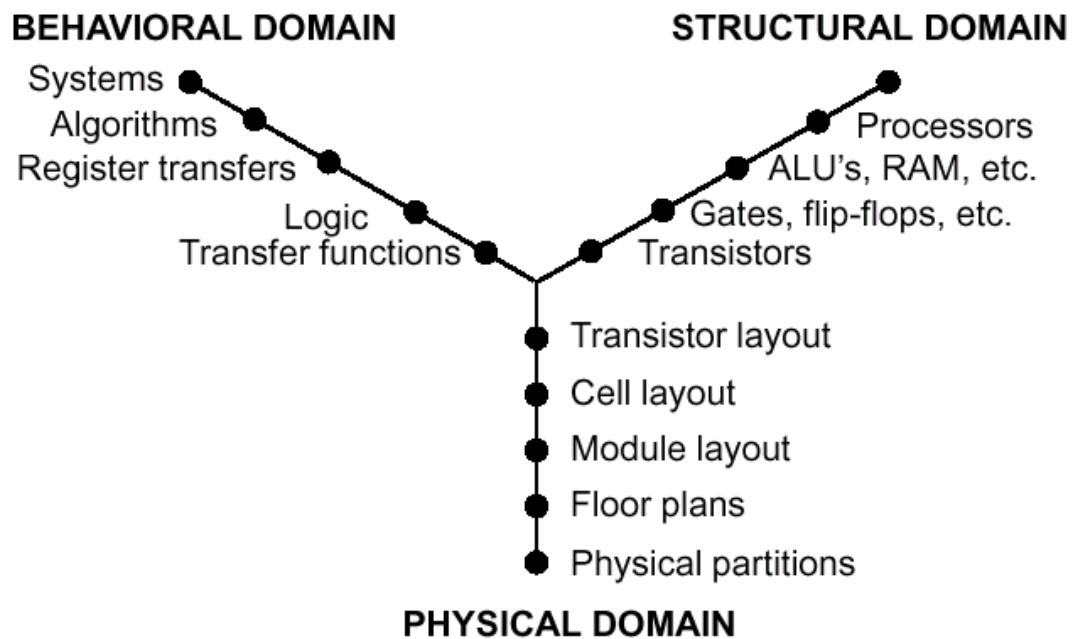


Physical



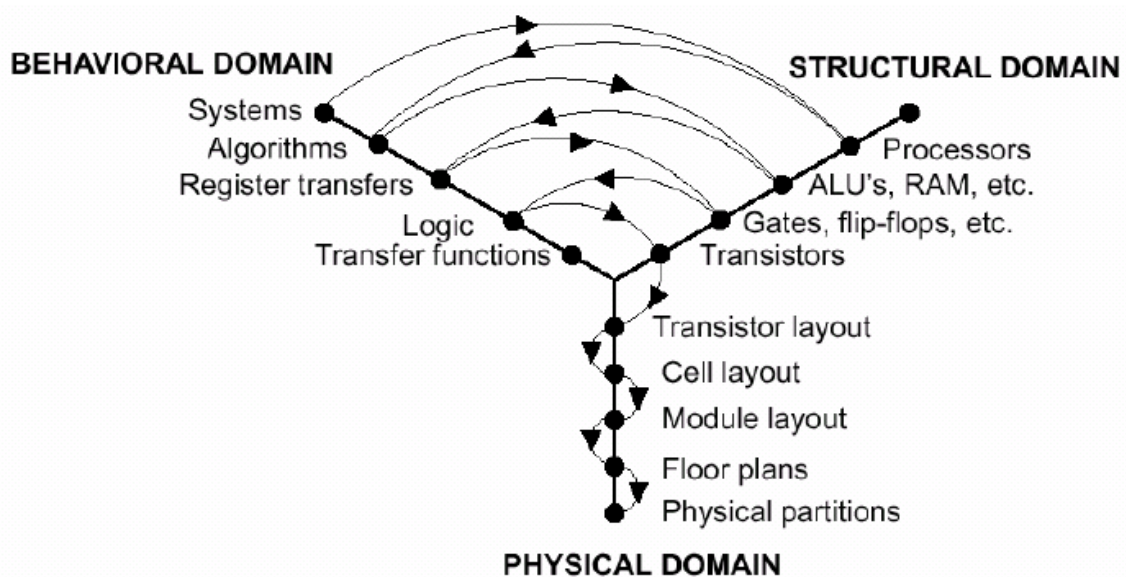
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Gajski's Y-Chart



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Top-Down Structural Design



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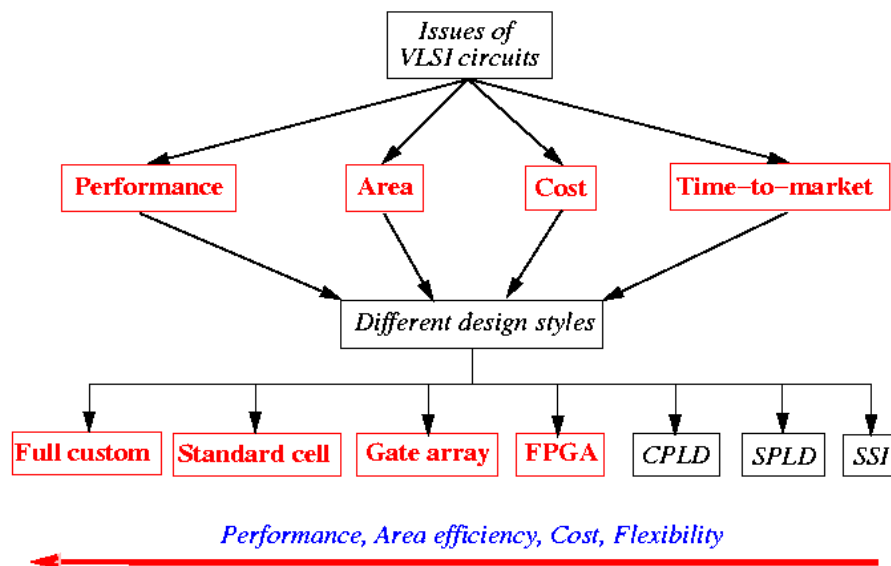
Design Styles

- There are various design styles:
 - Full custom, standard cell, sea of gates, FPGA, etc.
- Why having different design styles?

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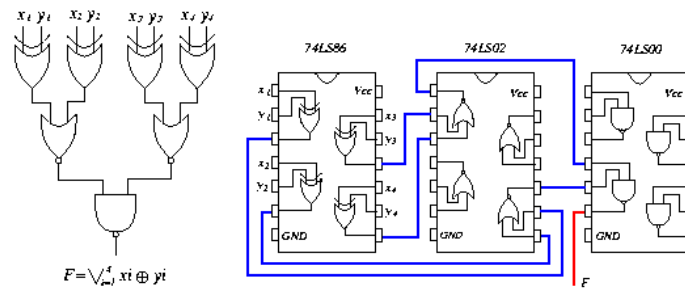
Design Styles

- Specific design styles shall require specific CAD tools



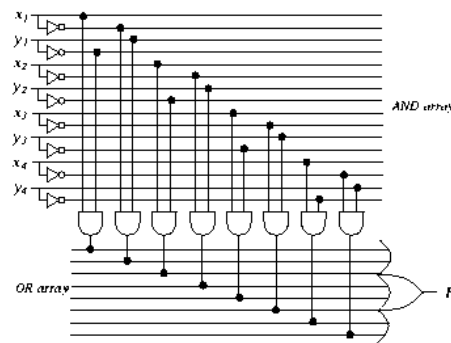
46

SSI/SPLD Design Style



(a) 4-bit comparator.

(b) SSI implementation.

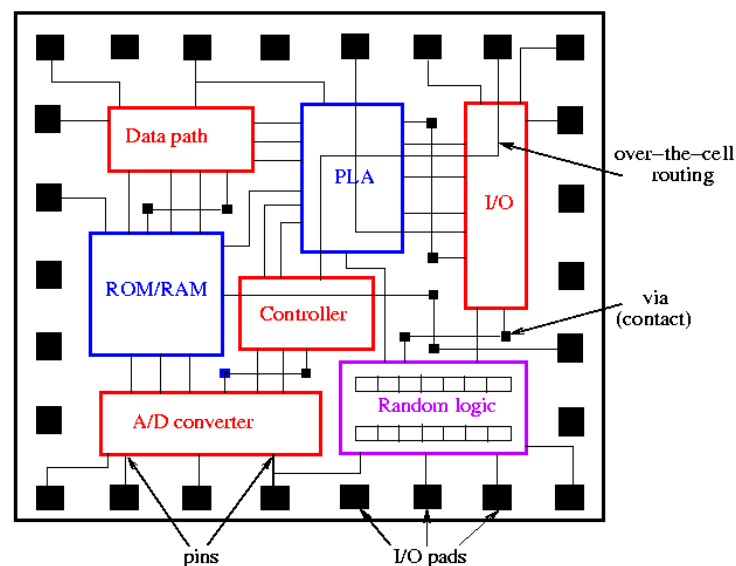


(c) SPLD (PLA) implementation.

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Full Custom Design Style

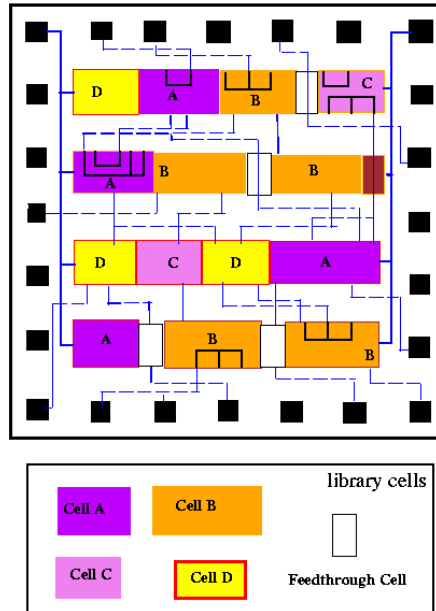
- Designers can control the shape of all mask patterns
- Designers can specify the design up to the level of individual transistors



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Standard Cell Design Style

- ❑ Selects pre-designed cells (of same height) to implement logic



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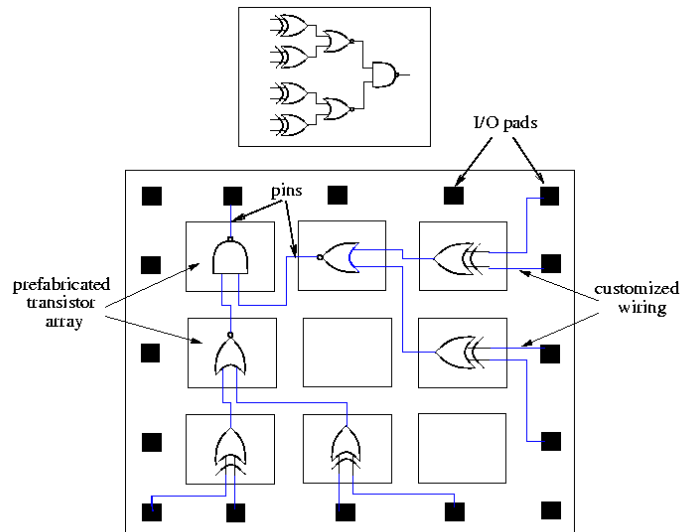
Standard Cell Example



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Gate Array Design Style

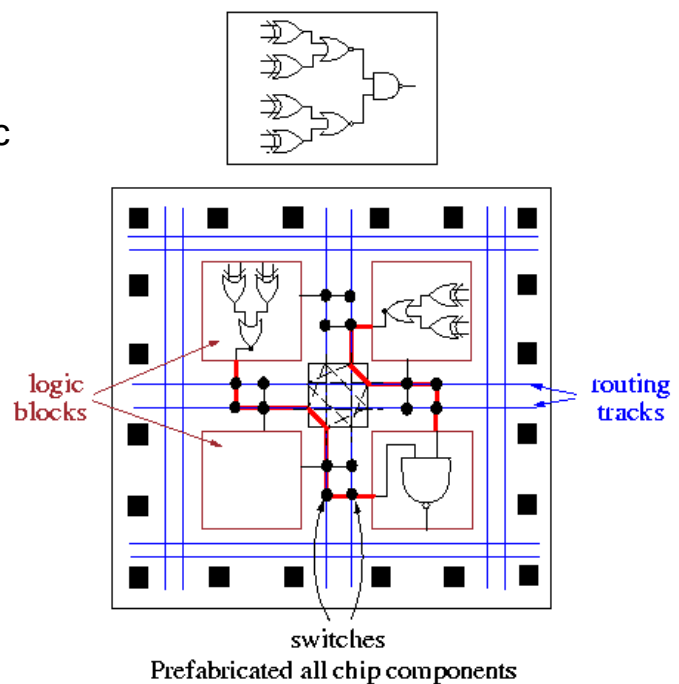
- ❑ Prefabricates a transistor array
- ❑ Needs wiring customization to implement logic



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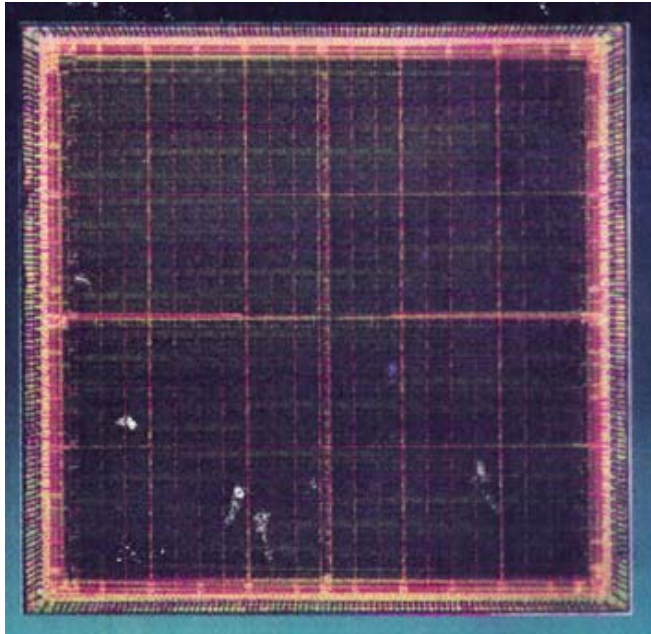
FPGA Design Style

- ❑ Logic and interconnects are both prefabricated
- ❑ Illustrated by a symmetric array-based FPGA



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Array-Based FPGA Example



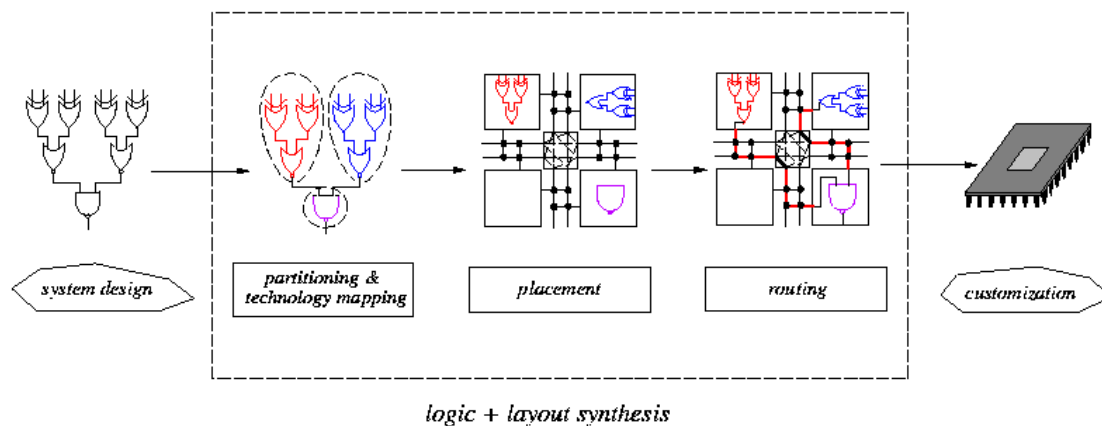
Lucent 15K ORCA FPGA

- 0.5 μm 3LM CMOS
- 2.45 M Transistors
- 1600 Flip-flops
- 25K bit user RAM
- 320 I/Os

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FPGA Design Process

- Illustrated by a symmetric array-based FPGA
- No fabrication is needed



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Comparisons of Design Styles

	Full custom	Standard cell	Gate array	FPGA	SPLD
Cell size	variable	fixed height*	fixed	fixed	fixed
Cell type	variable	variable	fixed	programmable	programmable
Cell placement	variable	in row	fixed	fixed	fixed
Interconnections	variable	variable	variable	programmable	programmable

* Uneven height cells are also used.

55

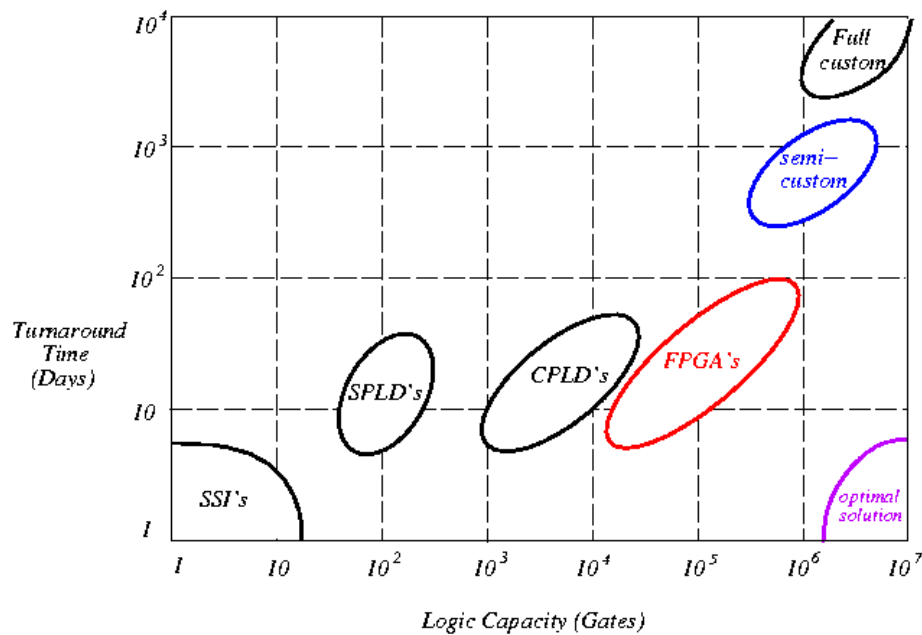
Comparisons of Design Styles

	Full custom	Standard cell	Gate array	FPGA	SPLD
Fabrication time	---	--	+	+++	++
Packing density	+++	++	+	--	---
Unit cost in large quantity	+++	++	+	--	-
Unit cost in small quantity	---	--	+	+++	++
Easy design and simulation	---	--	-	++	+
Easy design change	---	--	-	++	++
Accuracy of timing simulation	-	-	-	+	++
Chip speed	+++	++	+	-	--

+ desirable; - not desirable

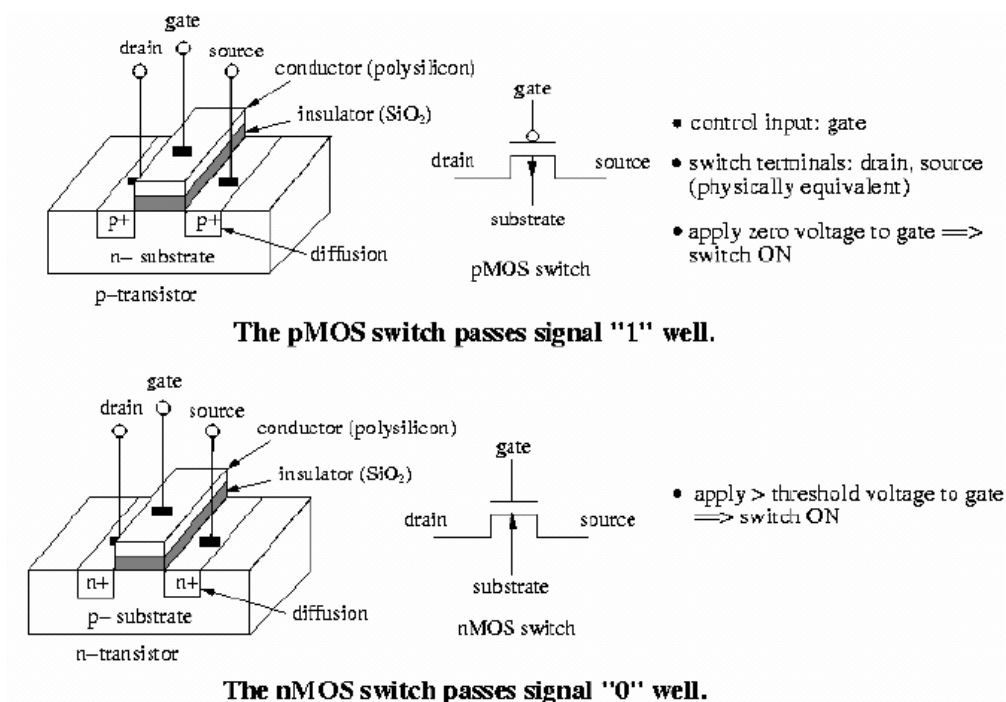
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Design Style Trade-offs



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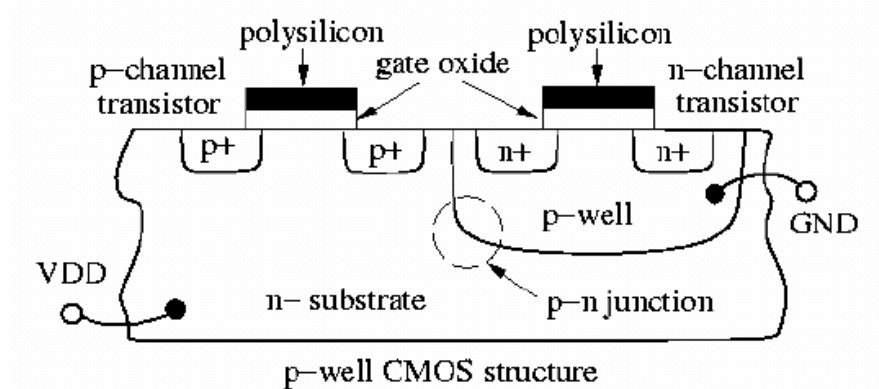
MOS Transistors



58

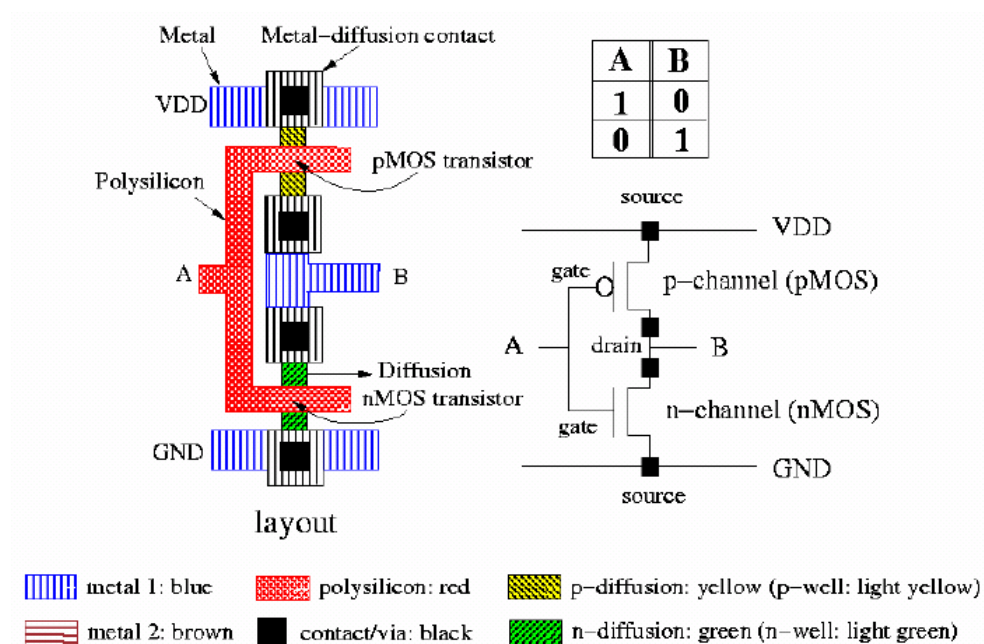
Complementary MOS (CMOS)

- The most popular VLSI technology (v.s. BiCMOS, nMOS)
- CMOS uses both *n*-channel and *p*-channel transistors
- Advantages: lower power dissipation, higher regularity, more reliable performance, higher noise margin, larger fanout, etc.
- Each type of transistor must sit in a material of the complementary type (the reverse-biased diodes prevent unwanted current flow)



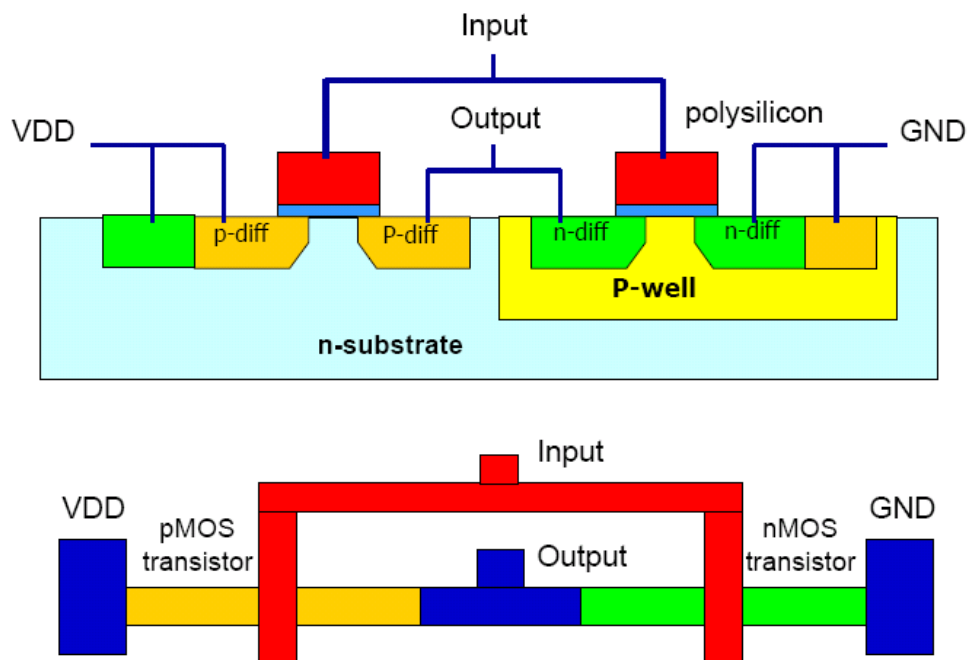
59

CMOS Inverter



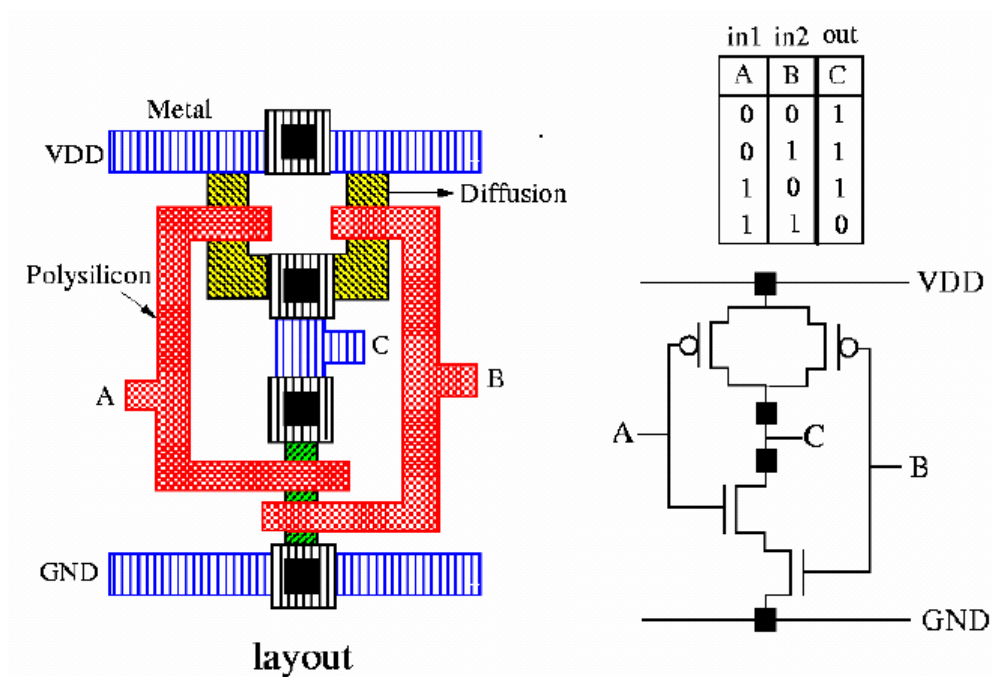
60

CMOS Inverter Cross Section



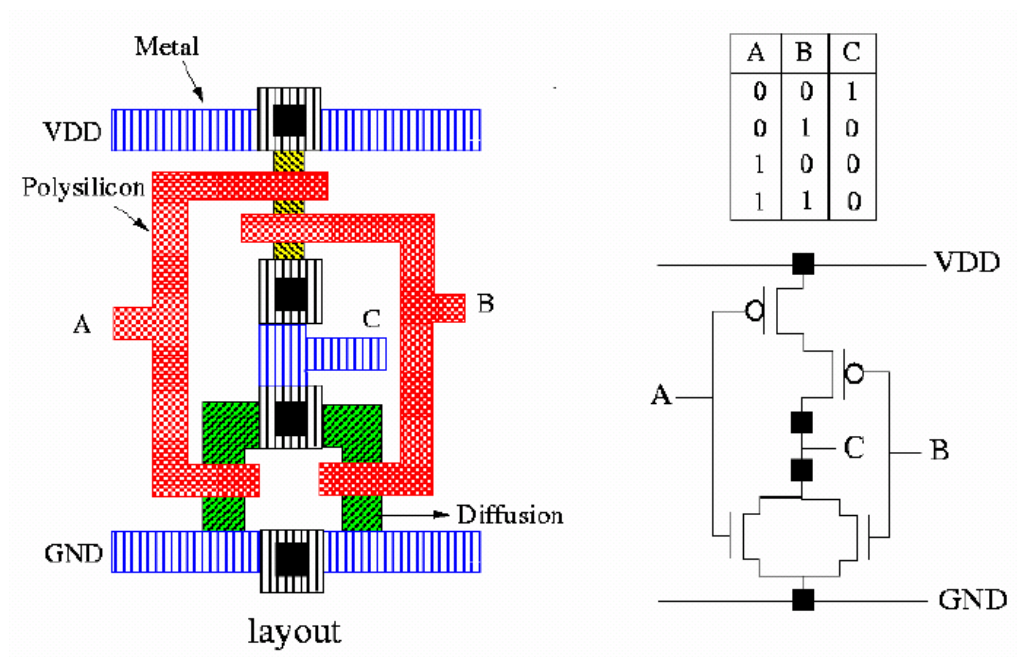
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CMOS NAND Gate



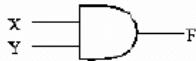
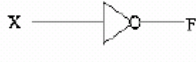
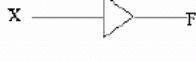
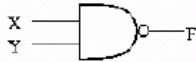
62

CMOS NOR Gate



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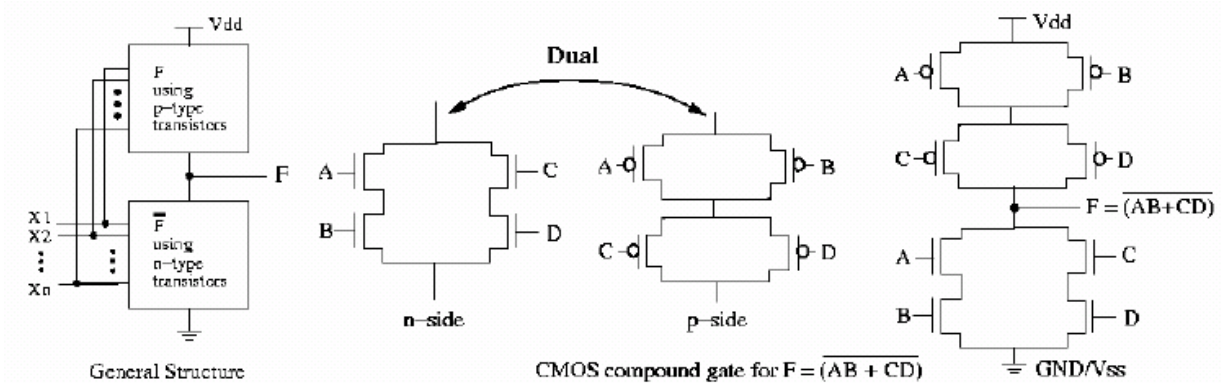
Basic CMOS Logic Library

Name	Distinctive shape	Algebraic equation	Cost (# of transistors)	Scaled gate delay (ps)
AND		$F = XY$	6	24
OR		$F = X + Y$	6	24
NOT (inverter/ repeater)		$F = \overline{X}$	2	10
Buffer (driver/ repeater)		$F = X$	4	20
NAND		$F = \overline{XY}$	4	14
NOR		$F = \overline{X + Y}$	4	14
Exclusive-OR (XOR)		$F = X\overline{Y} + \overline{X}Y$ $= X \oplus Y$	14	42

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Construction of Compound Gates (1/2)

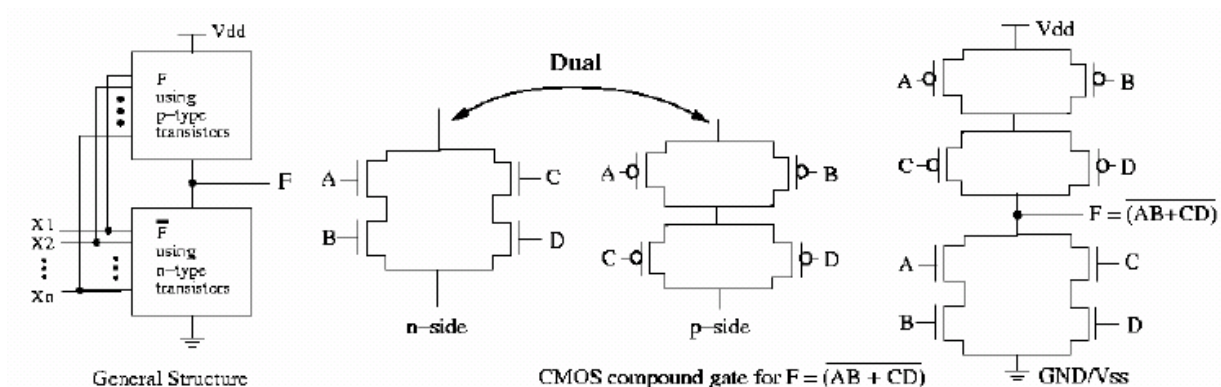
- Example: $F = \overline{A \cdot B + C \cdot D}$
- Step 1 (**n**-network): **Invert** F to derive n -network
 - $(\overline{F} = A \cdot B + C \cdot D)$
- Step 2 (**n**-network): Make connections of transistors:
 - AND $\Leftrightarrow$ Series connection
 - OR $\Leftrightarrow$ Parallel connection



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Construction of Compound Gates (2/2)

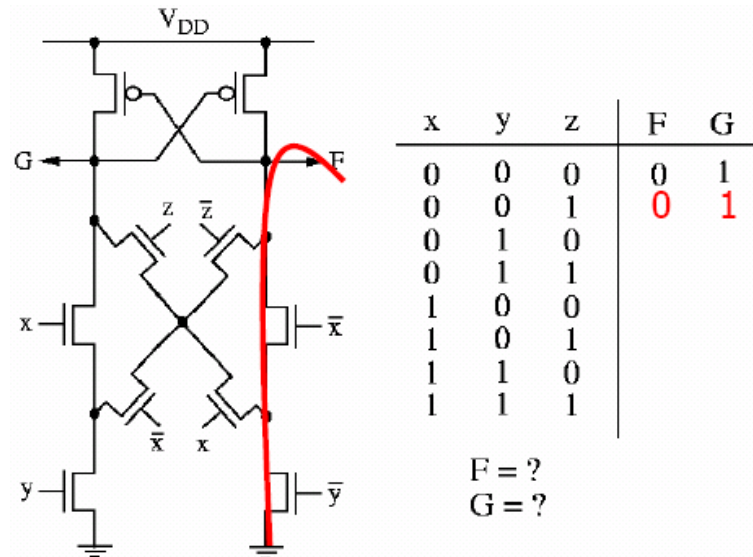
- Step 3 (**p**-network): Expand F to derive p -network
 - $(F = \overline{A \cdot B + C \cdot D} = \overline{A \cdot B} \cdot \overline{C \cdot D} = (\overline{A} + \overline{B}) \cdot (\overline{C} + \overline{D}))$
 - **each input is inverted**
- Step 4 (**p**-network): Make connections of transistors (same as Step 2).
- Step 5: Connect the n -network to GND (typically, 0V) and the p -network to VDD (5V, 3.3V, or 2.5V, etc).



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Complex CMOS Gate

- The functions realized by the n and p networks must be complementary, and one of the networks must conduct for every input combination
- Duality is not necessary



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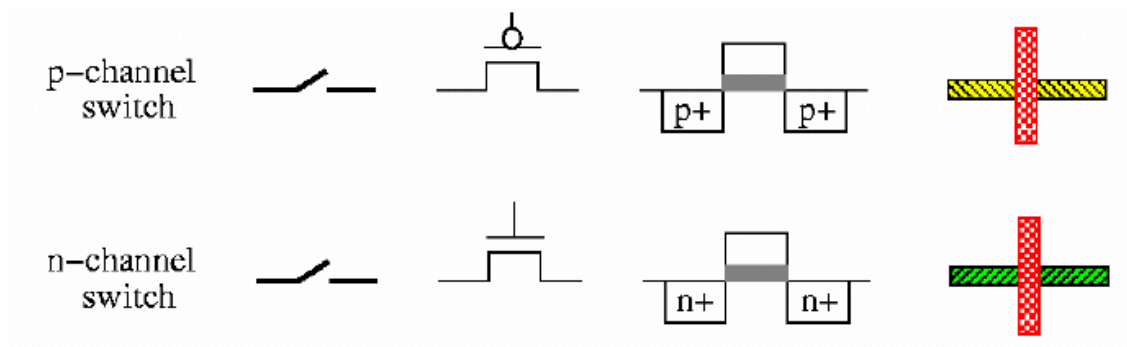
CMOS Properties

- There is always a path from one supply (V_{DD} or GND) to the output.
- There is never a path from one supply to the other. (This is the basis for the low power dissipation in CMOS--virtually no static power dissipation.)
- There is a momentary drain of current (and thus power consumption) when the gate switches from one state to another.
 - Thus, CMOS circuits have dynamic power dissipation.
 - The amount of power depends on the switching frequency.

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Stick Diagram

- Intermediate representation between the transistor level and the mask (layout) level.
- Gives topological information (identifies different layers and their relationship)
- Assumes that wires have no width.
- Possible to translate stick diagram automatically to layout with correct **design rules**.



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Stick Diagram

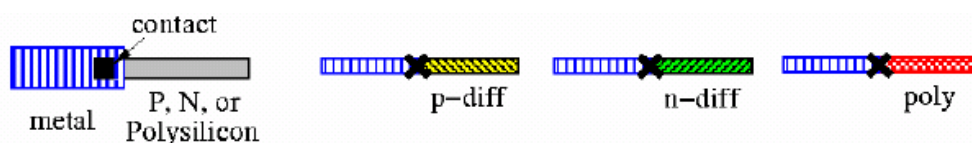
- When the same material (on the same layer) touch or cross, they are connected and belong to the same electrical node.



- When **polysilicon** crosses N or P **diffusion**, an N or P transistor is formed.
 - Polysilicon is drawn on top of diffusion.
 - Diffusion must be drawn connecting the source and the drain.
 - Gate is automatically self-aligned during fabrication.



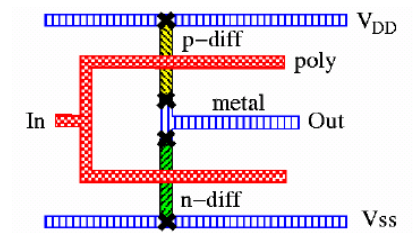
- When a metal line needs to be connected to one of the other three conductors, a **contact** cut (**via**) is required.



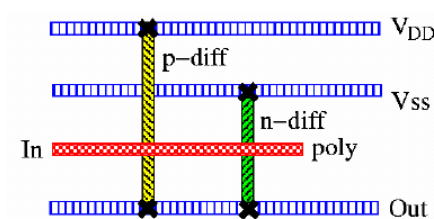
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CMOS Inverter Stick Diagram

Basic layout

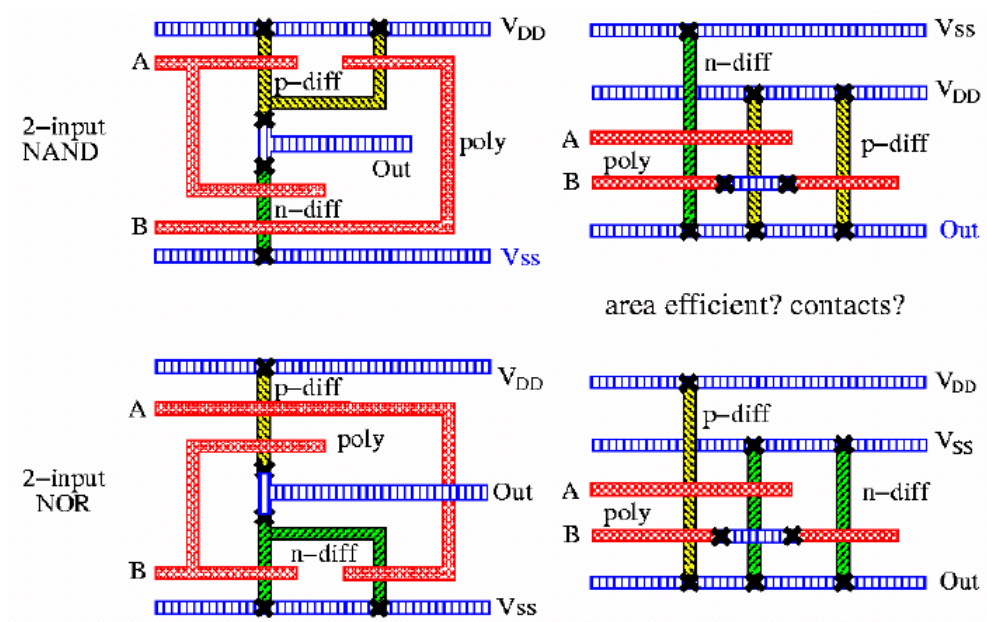


More area efficient layout



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CMOS NAND/NOR Stick Diagram



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Design Rules

- ❑ Layout rules are used for preparing the masks for fabrication.
- ❑ Fabrication processes have inherent limitations in accuracy.
- ❑ Design rules specify geometry of masks to optimize yield and reliability (trade-offs: area, yield, reliability).
- ❑ Three major rules:
 - **Wire width:** Minimum dimension associated with a given feature.
 - **Wire separation:** Allowable separation.
 - **Contact:** overlap rules.
- ❑ Two major approaches:
 - **“Micron” rules:** stated at micron resolution.
 - **λ rules:** simplified micron rules with limited **scaling** attributes.
- ❑ λ may be viewed as the size of minimum feature.
- ❑ Design rules represents a tolerance which insures very high probability of correct fabrication (not a hard boundary between correct and incorrect fabrication).
- ❑ Design rules are determined by experience.

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MOSIS Layout Design Rules

- ❑ MOSIS design rules (SCMOS rules) are available at <http://www.mosis.org>
- ❑ 3 basic design rules: Wire width, wire separation, contact rule.
- ❑ MOSIS design rule examples

R1	Min active area width	3 λ
R3	Min poly width	2 λ
R4	Min poly spacing	2 λ
R5	Min gate extension of poly over active	2 λ
R8	Min metal width	3 λ
R9	Min metal spacing	3 λ
R10	Poly contact size	2 λ
R11	Min poly contact spacing	2 λ

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SCMOS Design Rules

