# A Statistical Approach to the Timing-Yield Optimization of Pipeline Circuits

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# Outline

- Introduction
- Statistical timing models and analysis
- Problem formulation
- Statistical latch replacement
- Experimental results
- Conclusions and future work

# Introduction

- Problematic process variation in nanometer IC design
  - Circuits are more and more sensitive to process variation
  - Design for yield becomes the consensus

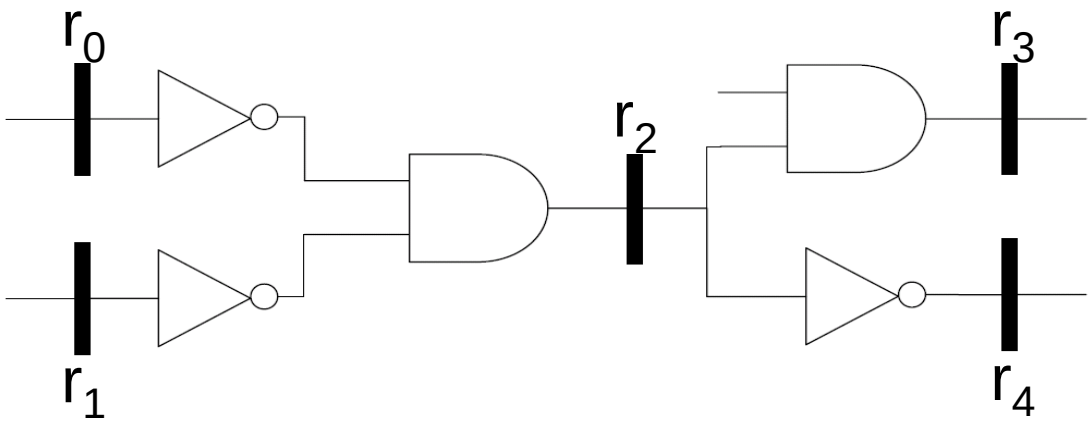
- Prior work
  - Statistical static timing analysis (SSTA)
  - Statistical optimization based on gate sizing

# Introduction (cont'd)

- Replacing D-FFs with level-sensitive latches:
  - Allow time barrowing
  - Improve timing yield

- Quantifying the improvement:
  - Calculate statistical timing yield based on SSTA and Monte Carlo simulation

# A Motivating Example

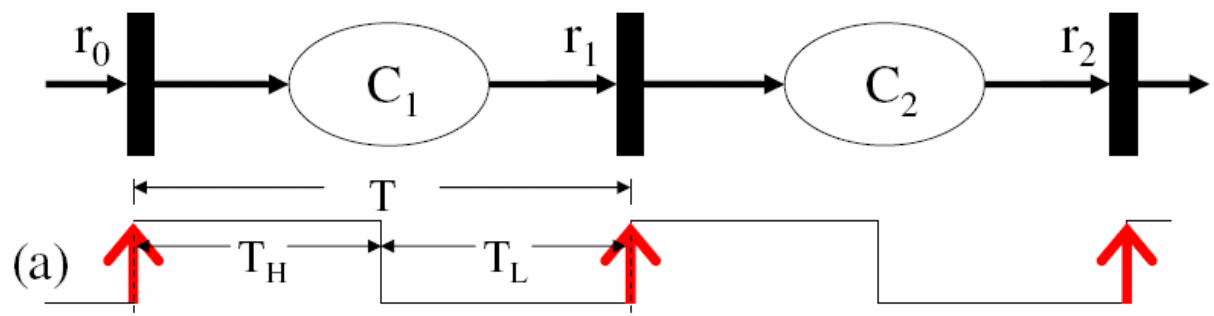



- Assume delay distributions N(5,1), N(3,1), and N(0,0) for ANDs, INVs, and wires, respectively. For 8ns clock period,
  - All registers in D-FFs:
    - Yield 33.19%
  - Replacing register $r_2$ with an active-low latch:
    - Yield 93.02%

# Statistical Timing Models and Analysis

- Statistical static timing analysis (SSTA)
  - $\Delta(r_i, r_j)$: longest path delay distribution
  - $\delta(r_i, r_j)$: shortest path delay distribution

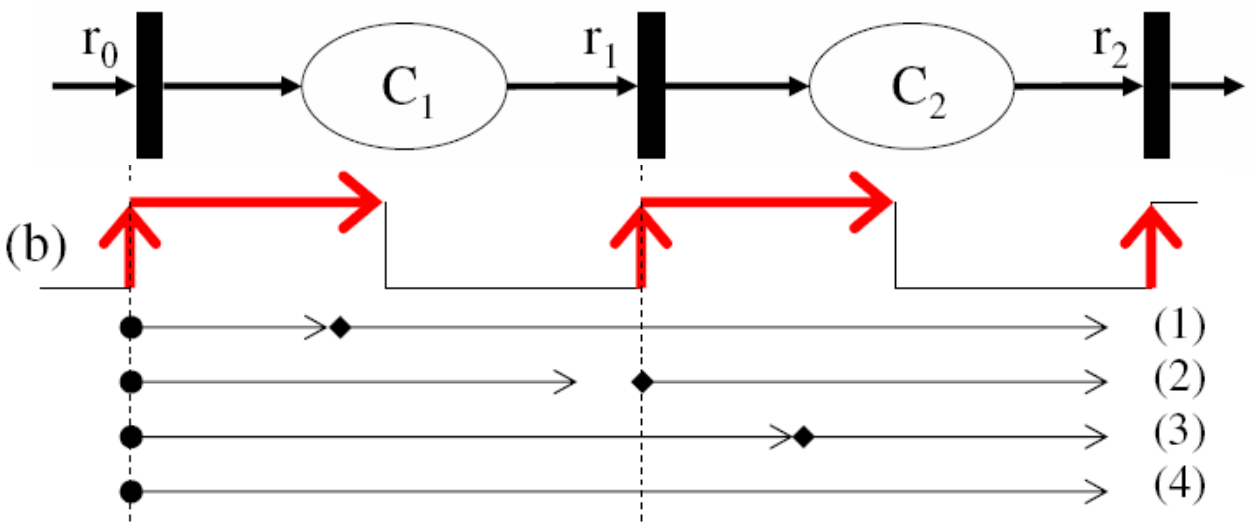
- Timing yield of circuits with D-FFs:
  - $\Pr[\bigwedge_{(r_i,r_j)} (\Delta(r_i, r_j) \leq T)]$




- Yield changed by latch replacement

# Timing Yield for Active-High Latch

$$
\begin{aligned}
&\Pr[\text{case 2}] + \Pr[\text{case 3}] \\
&= \Pr[(T_H \le \Delta(r_0, r_1) < T) \wedge (\delta(r_0, r_1) > T_H) \wedge (\Delta(r_1, r_2) \le T)] + \\
&\quad \Pr[(T \le \Delta(r_0, r_1) < T + T_H) \wedge (\delta(r_0, r_1) > T_H) \wedge \\
&\quad (T < \Delta(r_0, r_1) + \Delta(r_1, r_2) \le 2T)] \\
&= \Pr[(T_H \le \Delta(r_0, r_1) < T + T_H) \wedge (\delta(r_0, r_1) > T_H) \wedge \\
&\quad (\max\{\Delta(r_0, r_1), T\} + \Delta(r_1, r_2) \le 2T)].
\end{aligned}
$$



# Timing Yield for Active-High Latch (cont'd)

$$\Pr[\text{case 2}] + \Pr[\text{case 3}]$$

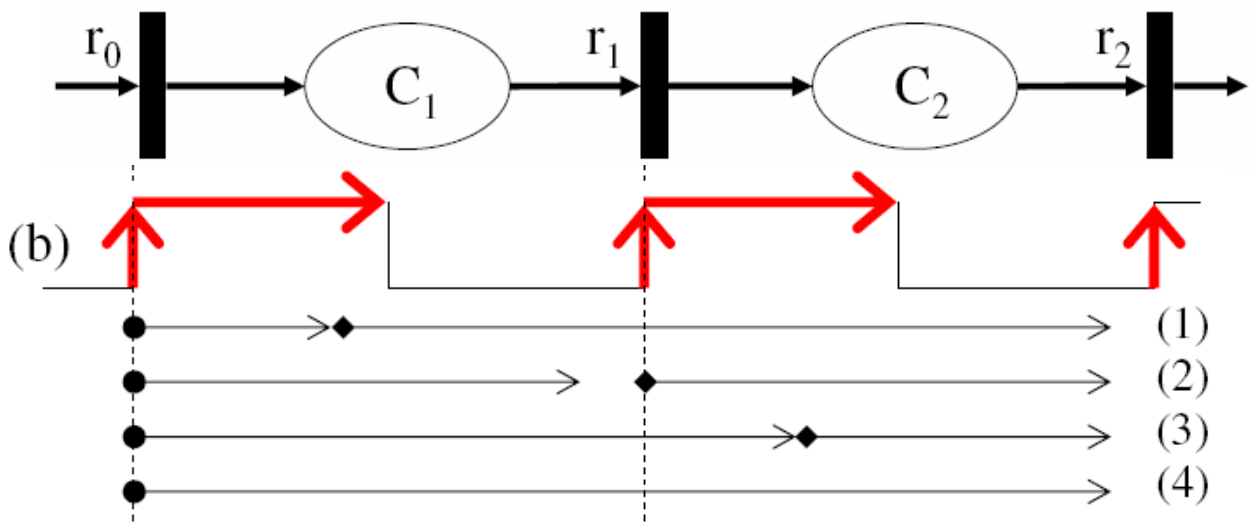
$$= \Pr[(\Delta_{\text{shift}}(r_0, r_1) < T) \wedge (\delta_{\text{shift}}(r_0, r_1) > 0) \wedge (\Delta_{\text{shift}}(r_1, r_2) < T) \wedge (\delta_{\text{shift}}(r_1, r_2) > 0)].$$

$$\Delta_{\text{shift}}(r_0, r_1) \equiv \Delta(r_0, r_1) - T_H,$$

$$\delta_{\text{shift}}(r_0, r_1) \equiv \delta(r_0, r_1) - T_H,$$

$$\Delta_{\text{shift}}(r_1, r_2) \equiv \max\{\Delta(r_0, r_1) - T, 0\} + \Delta(r_1, r_2), \text{ and}$$

$$\delta_{\text{shift}}(r_1, r_2) \equiv \delta(r_1, r_2),$$

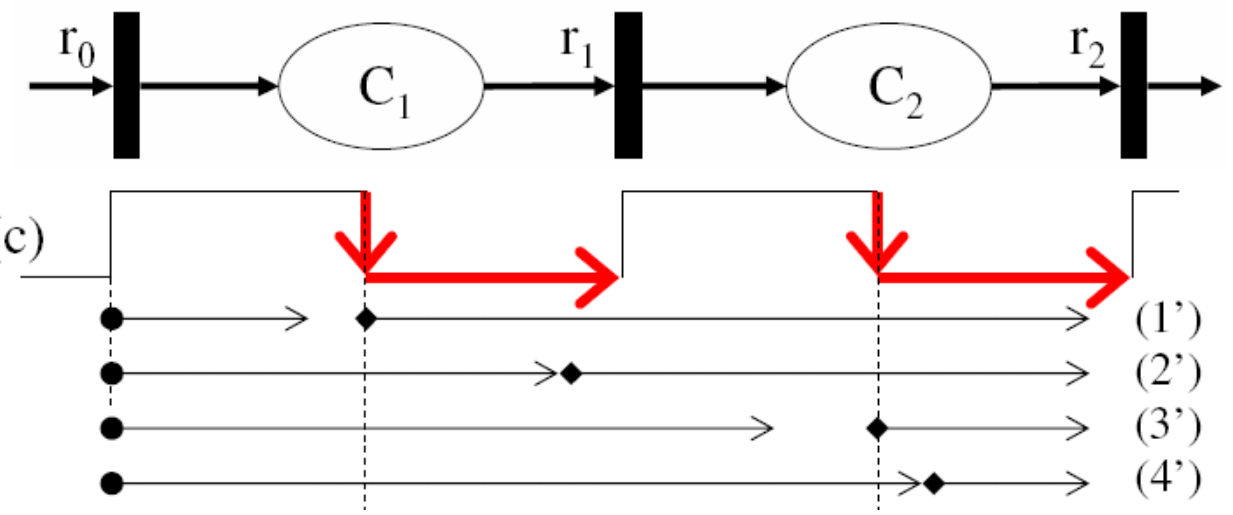


# Timing Yield for Active-Low Latch

$$\Pr[\text{case } 1'] + \Pr[\text{case } 2']$$

$$= \Pr[(\Delta_{\text{shift}}(r_0, r_1) < T) \wedge (\delta_{\text{shift}}(r_0, r_1) > 0) \wedge$$
$$(\Delta_{\text{shift}}(r_1, r_2) < T) \wedge (\delta_{\text{shift}}(r_1, r_2) > 0)].$$

$$\Delta_{\text{shift}}(r_0, r_1) \equiv \Delta(r_0, r_1),$$
$$\delta_{\text{shift}}(r_0, r_1) \equiv \delta(r_0, r_1),$$
$$\Delta_{\text{shift}}(r_1, r_2) \equiv \max\{\Delta(r_0, r_1) - T, -T_L\} + \Delta(r_1, r_2), \text{and}$$
$$\delta_{\text{shift}}(r_1, r_2) \equiv \max\{\delta(r_0, r_1) - T, -T_L\} + \delta(r_1, r_2),$$



# Problem Description

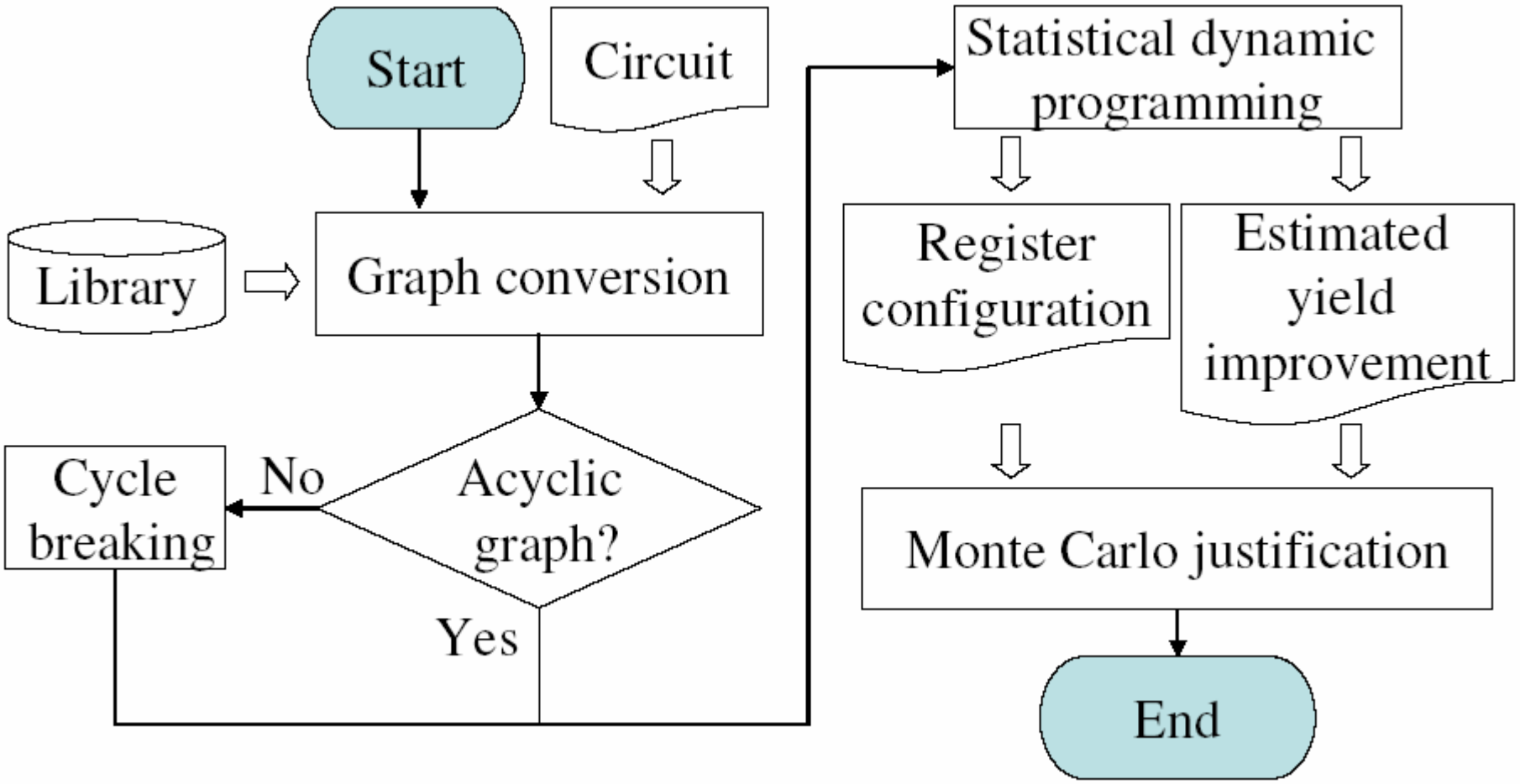
- Given:
  - A sequential circuit with register set $R$
  - Delay distributions of gates and wires

- Find a register configuration

  $\rho : R \rightarrow \{D, L, H\}$

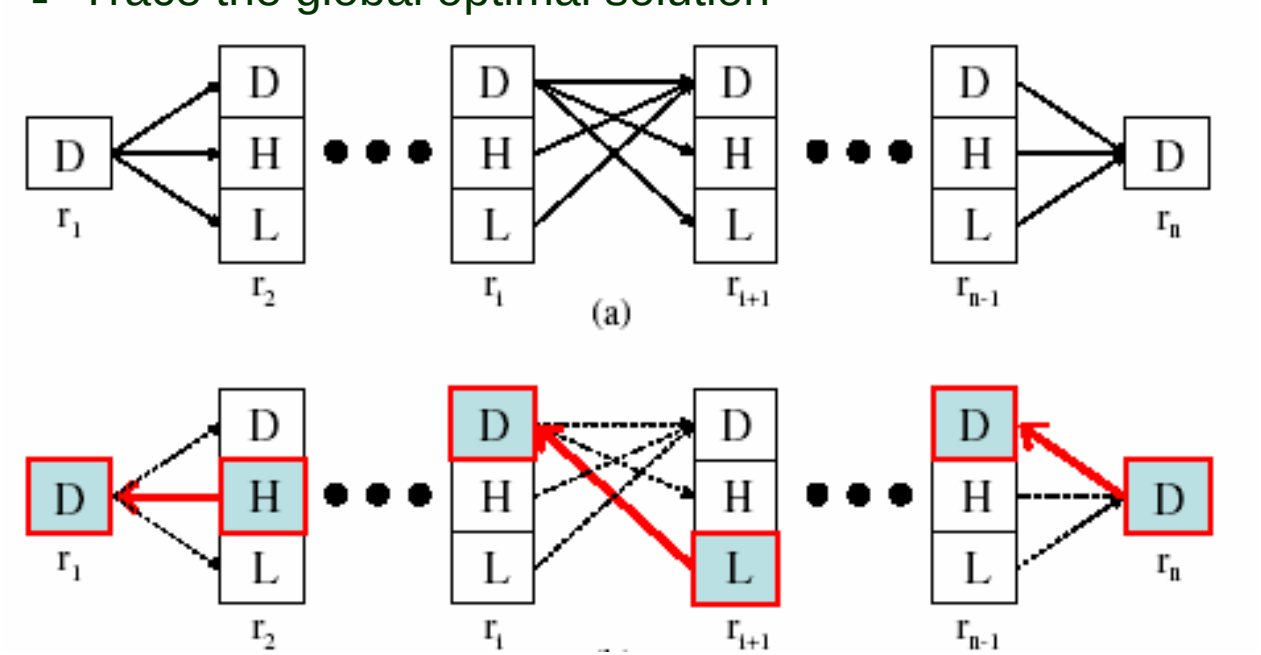
  such that timing yield is maximally improved under the condition that the fan-in and fan-out registers of a latch are D-FFs

# Flowchart


Start
Circuit
Library
Graph conversion
Acyclic graph?
No
Cycle breaking
Yes
Statistical dynamic programming
Register configuration
Estimated yield improvement
Monte Carlo justification
End

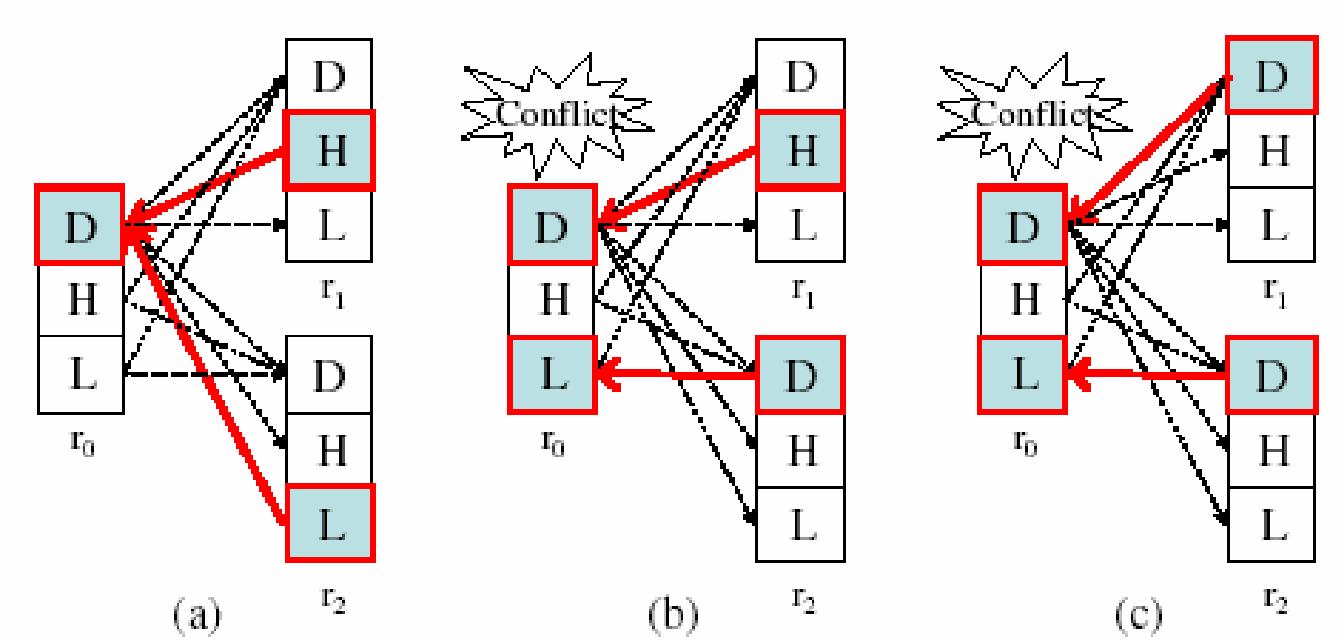
# Statistical Dynamic Programming

- Levelization:
  - Level of a register is the topological longest distance from PIs
- Dynamic programming:
  - Forward phase (from PIs to POs)
    - Compute all local optimal configurations at each level
  - Backward phase (from POs to PIs)
    - Trace the global optimal solution



# Redundant Solutions Reduction

- General pipeline width:
  - Exponential configurations
  - Simplification by preprocessing and interleaving latches with FFs
  - Resolving conflicts in backward tracing

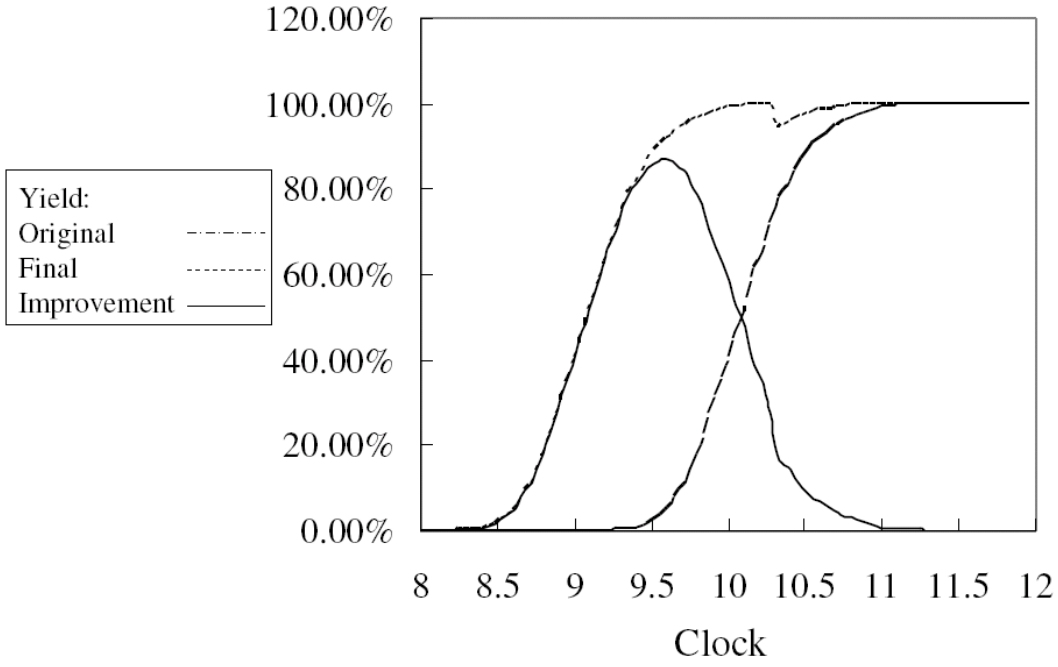


# Experimental Results

| Circuit | # of stages | Total reg. | Clock period | | Replaced reg. | | Original yield (%) | | Final yield (%) | | Impv. (%) | | CPU time (s) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 10% | 20% | 10% | 20% | 10% | 20% | 10% | 20% | 10% | 20% | 10% | 20% |
| ISCAS85 | Pipeline circuits with clock minimization | | | | | | | | | | | | | |
| c432 | 5 | 214 | 8.13 | 8.58 | 18 | 28 | 64.4 | 63.2 | 100.0 | 97.2 | 35.6 | 34.0 | 0.21 | 0.20 |
| c499 | 5 | 186 | 8.65 | 9.37 | 13 | 8 | 65.0 | 62.2 | 100.0 | 100.0 | 35.0 | 37.8 | 0.11 | 0.11 |
| c880 | 5 | 242 | 7.36 | 7.74 | 14 | 16 | 61.5 | 62.7 | 67.0 | 98.7 | 5.5 | 36.0 | 0.14 | 0.13 |
| c1355 | 5 | 218 | 9.42 | 10.18 | 9 | 10 | 60.3 | 62.3 | 100.0 | 99.8 | 39.7 | 37.5 | 0.16 | 0.16 |
| c1908 | 5 | 240 | 13.44 | 14.26 | 19 | 19 | 62.5 | 64.0 | 100.0 | 98.1 | 37.5 | 34.1 | 0.19 | 0.19 |
| c3540 | 5 | 278 | 11.14 | 11.96 | 78 | 62 | 64.0 | 62.3 | 94.1 | 93.9 | 30.1 | 31.6 | 0.42 | 0.40 |
| c5315 | 5 | 867 | 11.88 | 12.60 | 0 | 0 | 60.1 | 61.7 | 60.1 | 61.7 | 0.0 | 0.0 | 0.61 | 0.63 |
| c7552 | 5 | 879 | 11.26 | 12.12 | 56 | 69 | 63.7 | 63.5 | 99.6 | 99.9 | 35.9 | 36.4 | 0.71 | 0.68 |
| Average | | | | | | | | | | | 27.41 | 30.93 | 0.284 | 0.313 |
| ISCAS89 | Sequential circuits | | | | | | | | | | | | | |
| s1196 | - | 18 | 50.24 | 53.54 | 3 | 4 | 62.9 | 59.7 | 67.2 | 62.4 | 4.3 | 2.7 | 0.04 | 0.05 |
| s5378 | - | 179 | 47.79 | 52.98 | 10 | 10 | 65.2 | 61.1 | 71.9 | 65.2 | 6.7 | 4.1 | 0.44 | 0.45 |
| s9234 | - | 211 | 108.57 | 118.86 | 8 | 8 | 54.7 | 57.8 | 56.0 | 59.3 | 1.3 | 1.5 | 0.90 | 0.89 |
| Average | | | | | | | | | | | 4.10 | 2.77 | 0.460 | 0.463 |

# Case Study of Circuit C1355

- Yield before latch replacement tends to vanish quickly from 100% to 0% when reducing clock period from 10.5 to 9.5
- Yield after latch replacement remains high and stable for another 1 time unit
- The glitch is due to different configurations for different clock constraints



# Conclusions and Future Work

- Timing yield optimization for pipeline circuits by statistical dynamic programming
  - Robust against clock variation, and suitable for high-speed designs
  - Need to take care of the shortest path problem (unlike D-FF based designs)

- Future work:
  - Path delay balancing in logic synthesis
  - Optimize general sequential circuits

***Thanks for your attention***