

4×25 Gb/s Transceiver With Optical Front-end for 100 GbE System in 65 nm CMOS Technology

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Abstract—This paper presents a fully-integrated chipset for 4×25 Gb/s transceiver gearbox along with laser driver and photo detector front-ends. The transceiver provides 10:4 multiplexing and 4:10 demultiplexing conversion, with built-in clock generation, equalization, and amplification. The optical front-ends are realized as 4-element arrays, presenting remarkable performance with commercial vertical-cavity surface-emitting lasers and photodiodes. Feedforward equalizers and continuous-time linear equalizers are employed to compensate for loss and distortion in both electrical and optical domains. Fabricated in 65 nm CMOS technology, these chips can be lumped together as a compact module with performance exceeding typical 100 GbE standards.

Index Terms—100 Gb/s Ethernet, clock and data recovery (CDR), demultiplexer, gearbox TRX, laser diode driver, limiting amplifier, multiplexer, transceiver, transimpedance amplifier (TIA).

I. INTRODUCTION

THE ever-growing volume of Ethernet has pushed the backbone network data rate from Mb/s to tens or hundreds of Gb/s in past decades [1]. As illustrated in Fig. 1, the core network data rate in backbone averagely doubles every 1.5 years, which is even faster than the data rate improvement of server I/Os (2× every two years). Modern standards such as 100 Gb/s Ethernet (100GbE) will soon become mainstream products.

The 100 GbE must deal with several difficulties, which are less serious or do not exist at all in older standards: 1) the transceiver must provide bandwidth of at least 25 GHz (some standards such as OIF 28G-VSR [2] and 32G-FC [3] need more) with reasonable power consumption; 2) vertical-cavity surface-emitting laser (VCSEL) driver need to pull large current and perform fractional-bit pre-emphasis [4] at 25 Gb/s; 3) transimpedance amplifier (TIA) has to overcome the input capacitance introduced by photo-diode [5]; 4) interference, noise, and inter-lane coupling must be minimized. In addition, modern commercial optical components (i.e., VCSELs and

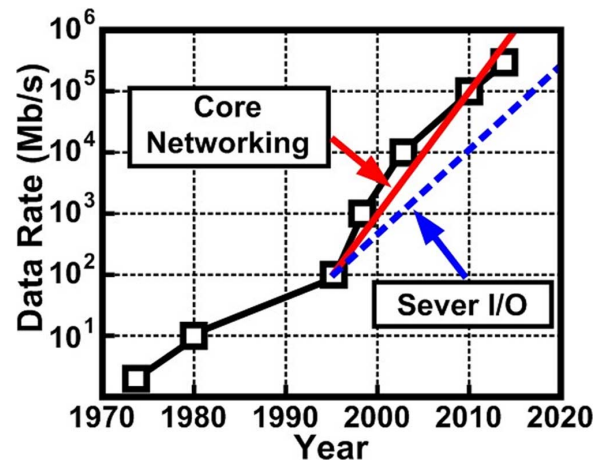


Fig. 1. Ethernet revolution.

photodiodes) are reaching their bandwidth limits around 25 GHz [6]. Overall speaking, a cost-efficient solution for 100GbE transceiver (TRX) is challenging in many aspects [7]–[11].

This paper provides a broad and deep description of the 100GbE chipset in transistor level with theoretical analysis. It consists of a 10:4 serializer (gearbox TX), a 4:10 deserializer (gearbox RX), a 4-lane laser-diode driver (LDD) array, and a 4-lane transimpedance amplifier/limiting amplifier (TIA/LA) array. Optical components are characterized and modeled as well. This prototype incorporates various circuit techniques to eliminate or at least relax the foregoing challenges, arriving at remarkable results. All circuits are designed and fabricated in 65 nm CMOS technology. A thorough testing result for individual blocks and the whole integrated system has been reported with explanation and discussion.

This paper is organized as follows. Section II introduces the overall architecture of a 100 Gb/s Ethernet, including gearbox physical layer (PHY) and optical front-ends. Sections III–VII present the design details of gearbox TX, gearbox RX, LDD array, and TIA/LA array, comparing pros and cons if more than one structure is described. Section VIII discloses the model and behavior of the optical components, and Section IX reveals the measurement results.

II. 100 GbE ARCHITECTURE

Fig. 2 shows the architecture of a typical 100 Gb/s Ethernet transceiver, where 10×10 Gb/s input data is serialized into 4×25 Gb/s bit stream by a 10:4 serializer. A 4-element LDD array subsequently drives four laser diodes, emitting 850 nm

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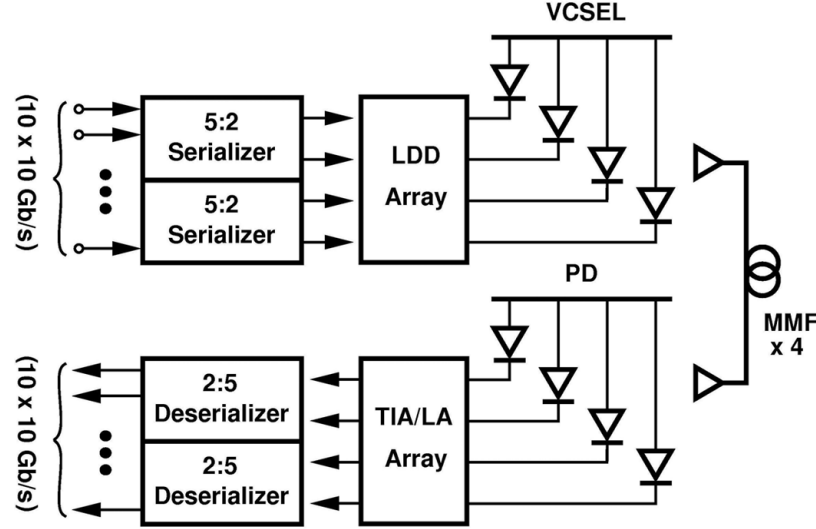


Fig. 2. 100GbE architecture.

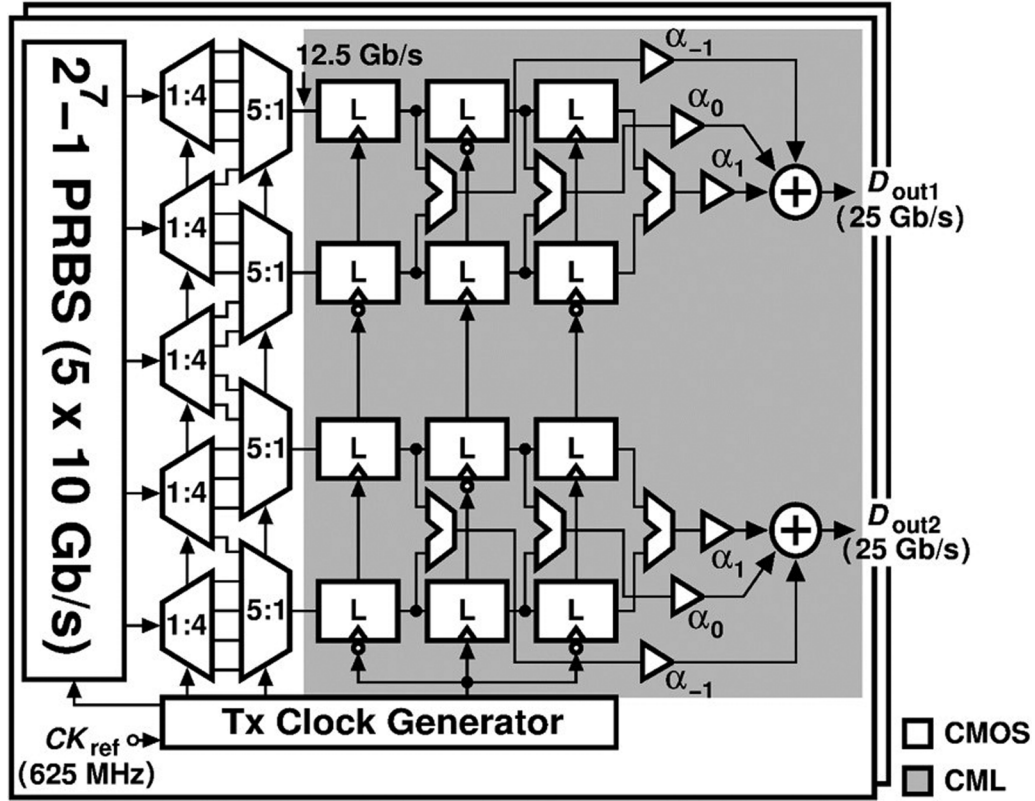


Fig. 3. Gearbox TX architecture.

light into four multimode fibers (MMFs). After traveling over a few hundred meters, these optical signals are captured and transformed into electrical domain by means of photo diodes and the TIA/LA array. A 4:10 deserializer recovers the clock and data, and restores the data sequences into 10×10 Gb/s outputs. In real applications, gearbox TRX and optical front-ends (i.e., LDD and TIA/LA arrays) may be separated by several inches in order to fulfill system-level integration. Thus, 50Ω termination, sufficient driving force, and loss compensation (equalization) must be taken into consideration in each blocks. Due to the non-power-of-2 multiplexing (MUXing) and demul-

tiplexing (DMUXing), the serializer and deserializer are actually composed of two identical 5:2 and 2:5 mapping blocks. We describe each function block in the following sections.

III. GEARBOX TX

A serializer unit must accomplish data multiplexing from 5×10 Gb/s to 2×25 Gb/s and pre-emphasis output driving. These functions necessitate clocks at different frequencies and phases, which have to be created on chip as well. Fig. 3 depicts the proposed gearbox TX. It consists of a multi-frequency multi-phase

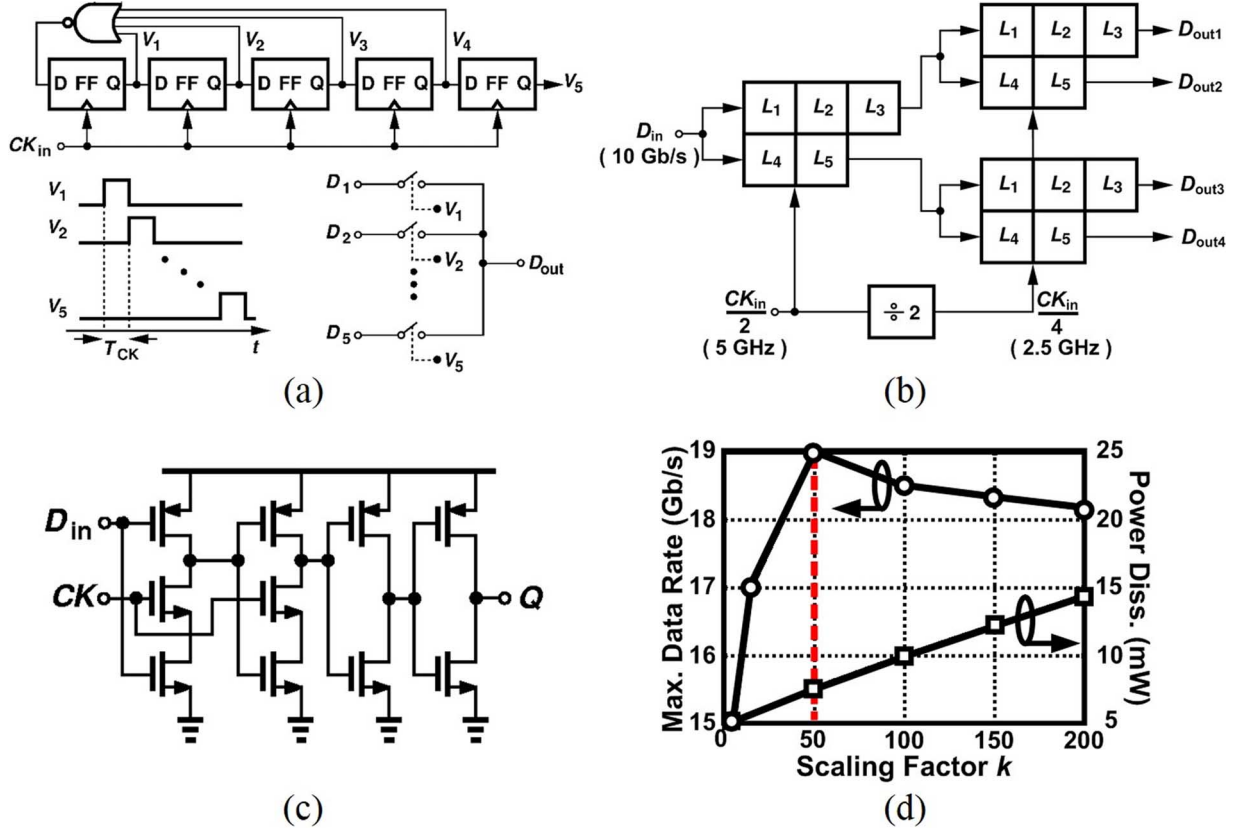


Fig. 4. Gearbox TX building blocks: (a) 5:1 MUX, (b) 1:4 DMUX, (c) TSPC latch, (d) maximum data rate and power consumption as a function of scaling factor k .

clock generator and two identical sets of 5:2 serializer. Each serializer includes five 1:4 DMUXes and four 5:1 MUXes. Modified from [12] with even larger bandwidth, the feedforward equalizer (FFE) utilizes a half-rate structure. A built-in pseudo-random binary sequence (PRBS) generator is introduced to facilitate testing, which provides five independent 10 Gb/s data inputs with length $2^7 - 1$.

The 5:1 MUX circuit is illustrated in Fig. 4(a), which is realized as a 5-input transmission-gate sampler operated by rail-to-rail data and clocks. Five true-single-phase-clock (TSPC) flipflops with a NOR gate feedback produce five 20% duty-cycle clocks $CK_{1\sim5}$ for proper sampling. The 1:4 DMUX is realized as a typical tree structure [Fig. 4(b)], which employs TSPC latches [Fig. 4(c)] to minimize power consumption. In 65 nm CMOS technology, the minimum device size for NMOS and PMOS is $W/L = 120 \text{ nm}/60 \text{ nm}$. Equivalent NMOS and PMOS devices are ratioed to be around 1:2 to compensate different mobilities as typical digital circuits. However, to increase the bandwidth, we choose actual NMOS and PMOS devices in Fig. 4(c) to be k times larger than their minimum sizes. With balanced pull-up and pull-down strength, we obtain the bandwidth and power consumption of the TSPC latch for different scaling factor k as shown in Fig. 4(d). It is not surprising that the maximum data rate ramps up as devices become larger, since the parasitic capacitance increases in a way slower than the driving force. We select scaling factor $k = 50$ to reach 19 Gb/s operation [Fig. 4(d)]. Here, Fig. 4(d) is obtained under the loading condition of fan-out-of-1 ($FO = 1$). Two DMUX stages are properly sized to further save

power. It is worth noting that the allowable data rate eventually degrades slightly for $k > 50$, primarily because the routing capacitance and other parasitics in bigger devices are no longer insignificant. Note that the final inverter stage in Fig. 4(c) could be possibly omitted to further save power. The inverted logic would be corrected in the CMOS to CML converter if we do so.

The built-in phase-locked loop (PLL) in gearbox TX plays an important role in output data jitter performance, since the clock jitter is imposed onto the data output directly. To minimize clock phase noise, we realize TX clock generator as a two-stage subharmonically-injection-locking PLL [13] as depicted in Fig. 5. To keep the two locking forces (i.e., loop locking and injection locking) coexisting in a harmonic way, certain delays must be added to make sure the phase difference between VCO's core current and injection current is within the maximum tolerable phase error [14]. Fortunately, fixed delays are sufficient even for severe temperature variations, as demonstrated in [14]. Here, fixed delays $\Delta T_1 \sim \Delta T_4$ are inserted to ensure that injections always locate at save zone (approximately 187°) over process, supply voltage, and temperature (PVT) variations. Simulation shows that no “pseudo locking phenomenon” would occur for $-20 \sim 50^\circ\text{C}$, $\pm 10\%$ supply, and all corners variations. More details can be found in [14]. Note that a two-stage structure is necessary in such an injection-locking PLL because 12.5, 10 and 2.5 GHz clocks have to be produced.

IV. GEARBOX RX

Gearbox RX design (Fig. 6) follows the basic structure of our previous work [15], which incorporates pre-amplifier (with gain

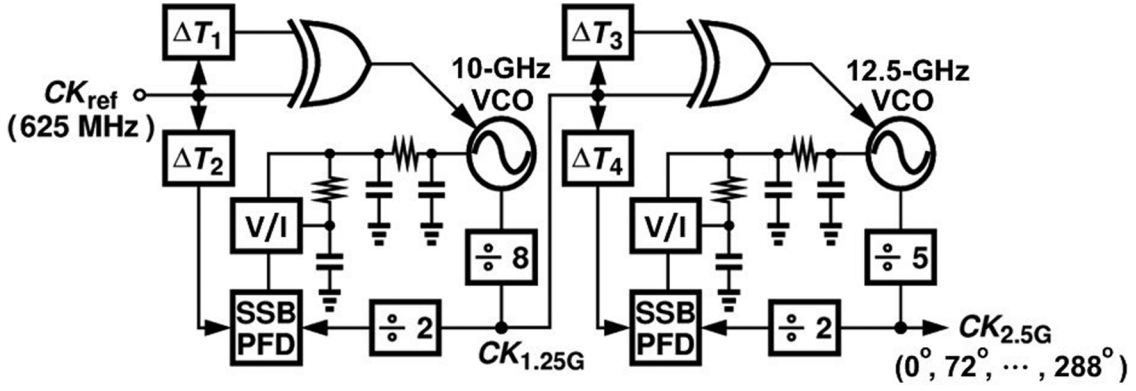


Fig. 5. Clock generator in gearbox TX.

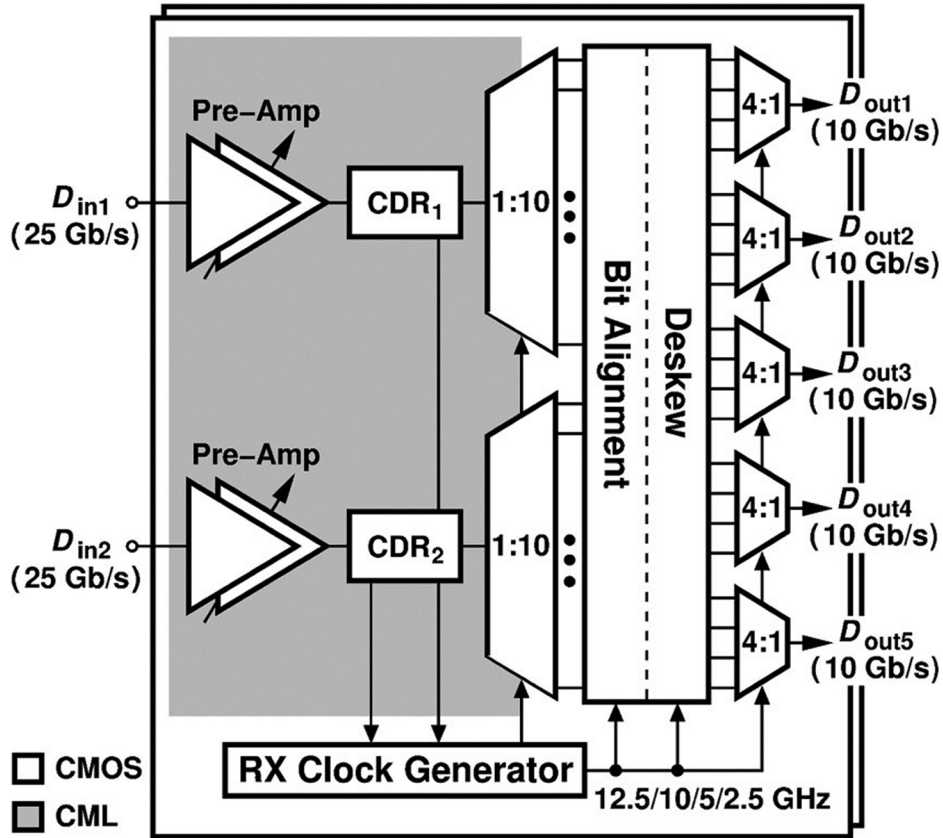


Fig. 6. Gearbox RX architecture.

of 0 ~20 dB), mixer-based clock and data recovery (CDR) circuits [16], 1:10 DMUXes and 4:1 MUXes. The CDR adopts a full-rate linear phase detection structure, which has been proven in silicon [15]. In this modified version, we employ equalizers along with pre-amplifiers to overcome possible channel loss at input.

The limiting amplifier/equalizer combination is depicted in Fig. 7(a), where stages with different boosting techniques are placed alternately to avoid early saturation or invalid switching. Conventional RC degenerated filter fails to provide large tunable range for boosting, even with the help of inductive peaking. Therefore, we need a novel structure for the boosting cells. It is well known that both series and shunt peaking can be used in a broadband amplifier to increase the bandwidth [17], but the

peaking is subject to PVT variations and is hard to control. As a result, we come up with a tunable gain/boosting stage as shown in Fig. 7(b). Here, depending on the ratio of I_1 and I_2 , part of the data goes through the peaking of L_2 whereas the rest does not. Since the total amount of I_1 and I_2 is a constant ($I_1 + I_2 = I_{SS}$) and their tuning is continuous, we arrive at a gain stage with tunable peaking. It is worth noting that the small-signal gain of Fig. 7(b) reaches a maximum as $I_1 \approx I_2$. This gain variation could be compromised in circuits such as limiting amplifiers. The filter stage is shown in Fig. 7(c), which employs inductive peaking to sustain the bandwidth along the data path. The current tuning is accomplished by using a differential pair with two diode-connected current mirrors to copy I_1 and I_2 . The overall boosting behavior is also shown in Fig. 7(a). With tunable gain

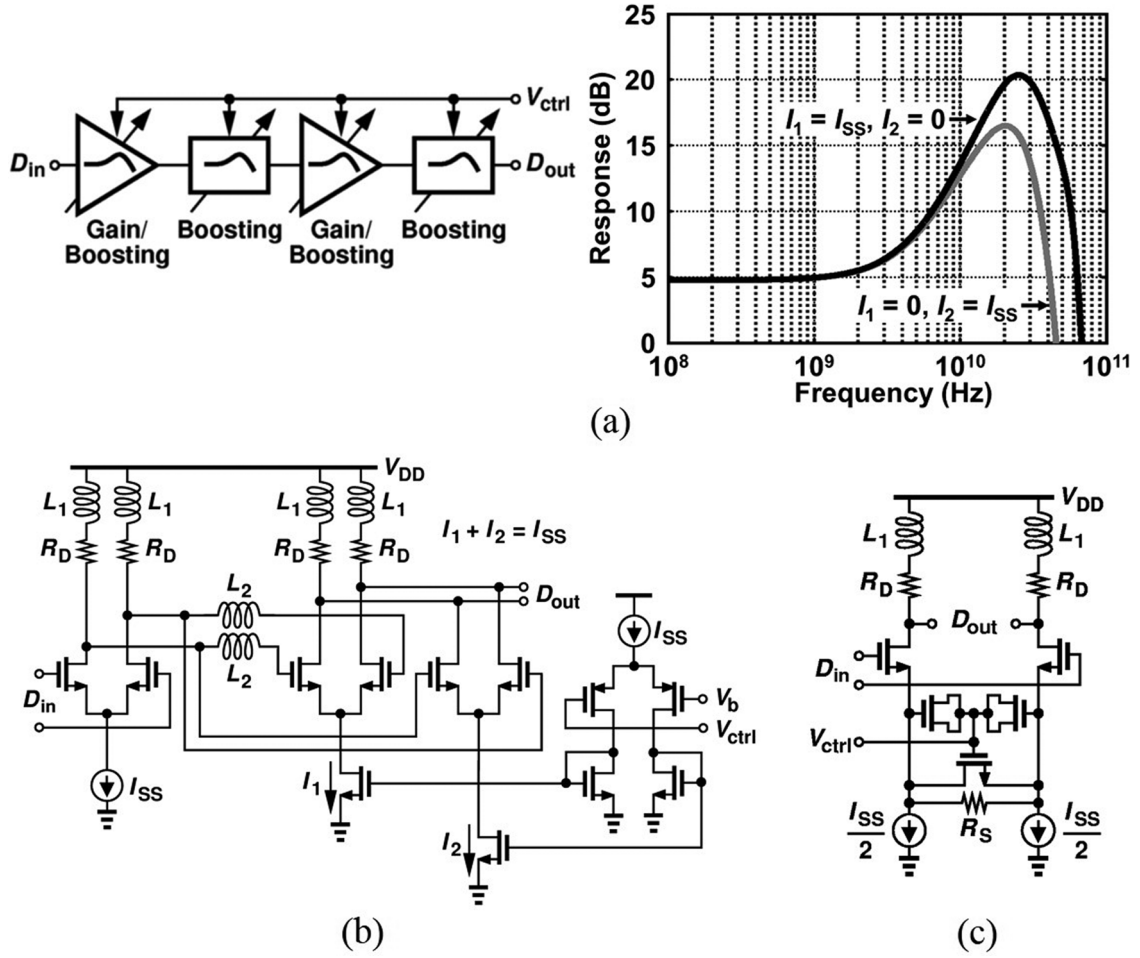


Fig. 7. (a) Simplified limiting amplifier/equalizer structure; (b) gain/boosting stage; (c) boosting stage.

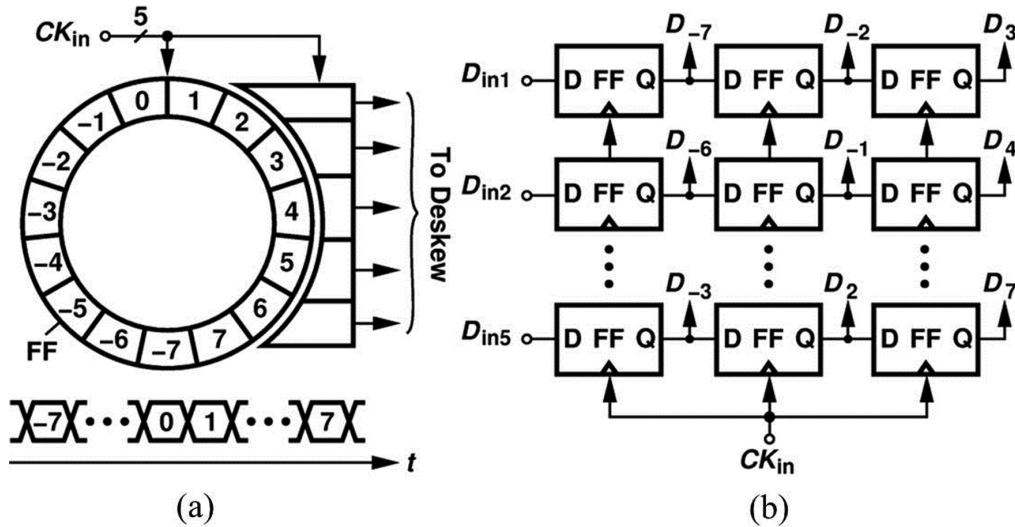


Fig. 8. (a) Bit alignment circuit, (b) shift register.

stage, we extend the overall range from 11 to 15 dB. No dc gain is sacrificed by doing so.

In addition to the existing deskew circuit that removes phase offset within 1 bit, we further introduce a bit alignment circuit in front to fix up to ± 7 bits of misalignment due to optical length difference. Fig. 8(a) reveals the bit alignment design, where a

15 bit shift register [Fig. 8(b)] governed by 4 bit control logic stores data stream. Based on the control signal, 5 consecutive bits out of $[-7, \dots, 0, \dots, 7]$ can be taken as data output and can be set to the subsequent circuit for processing. Since 100GbE only needs fiber channel of 100 ~ 300 m, a 15 bit phase shifter is sufficient in most cases.

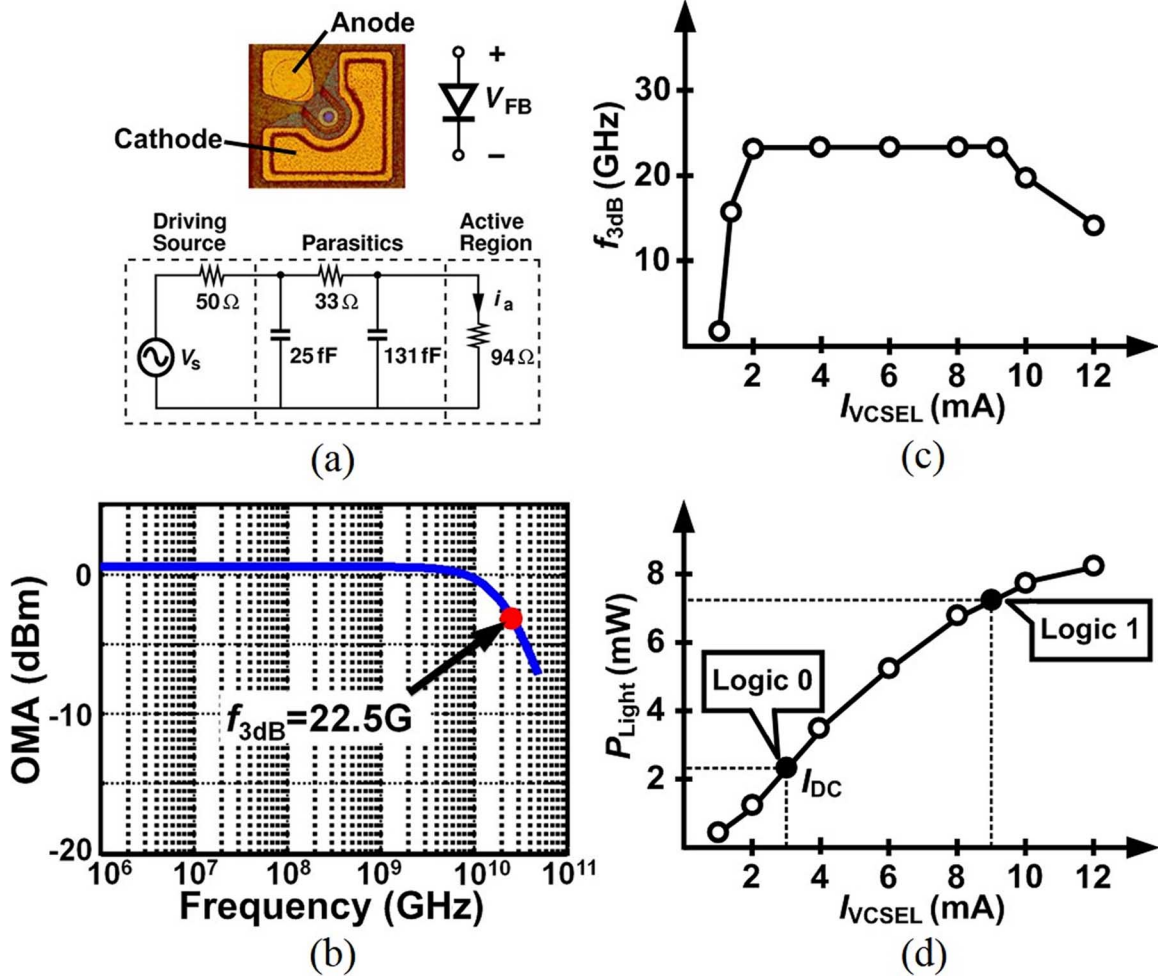


Fig. 9. (a) Typical VCSEL and its small-signal model, (b) measured frequency response as bias current = 6 mA, (c) -3 dB bandwidth as a function of bias current, (d) VCSEL transfer function.

V. OPTICAL COMPONENTS

The optical front-end also involves considerable circuit techniques. Before looking at LDD and TIA/LA array design, we need to investigate the behavior of VCSEL and photo detector (PD).

A typical VCSEL is shown in Fig. 9(a), where the cathode is connected to chip for current pulling due to its smaller parasitic capacitance [18]. A small-signal model is established for transient simulation, which tightly matches the measured frequency response as shown in Fig. 9(b). With bias current of 6 mA, the bandwidth is barely enough for 25 Gb/s operation.¹ In addition, the -3 dB bandwidth of a VCSEL increases as bias current increases and saturates as it becomes larger than 2 mA. We plot the -3 dB bandwidth for a VCSEL as a function of bias current in Fig. 9(c). A high-speed VCSEL needs a dc (standby) current (I_{DC}) as large as 3 mA to ensure fast switching time between on and off [Fig. 9(d)]. Otherwise, the VCSEL deviates from linear operation and begins to cause errors. A constant pulling current over PVT variations becomes essential here.

¹As we will see in the following paragraphs, the whole optical link including VCSEL + Fiber + PD is only 15.33 GHz.

Other than the above issues, the VCSEL driver needs to overcome the VCSEL's relaxation oscillation phenomenon at large signals. As illustrated in Fig. 10(a), a high-speed VCSEL presents quite significant ringing effect at rising and falling edges due to the exchange of energy between photons and electrons [19]. Unlike regular signal distortion caused by channel loss or reflection, these sharp humps and dents need fractional-bit pre-emphasis. For a two-tap fractional FFE with tunable delay ΔT and pre-emphasis factor α [Fig. 10(b)], we arrive at magnitude and phase response as

$$|H(j\omega)| = \sqrt{1 + \alpha^2 - 2\alpha \cos(\omega\Delta T)} \quad (1)$$

$$\angle H(j\omega) = \tan^{-1} \left[\frac{\alpha \sin(\omega\Delta T)}{1 - \alpha \cos(\omega\Delta T)} \right] \quad (2)$$

Typical VCSEL requires a compensation of approximately 2 dB, i.e., $\alpha = 0.25$. Considering boosting efficiency and phase concordance, we set $\Delta T = 20$ ps in this prototype.

The high-speed PD must be studied before developing a TIA/LA front-end. Like other discrete components, PD inevitably introduces parasitic capacitance. For modern PDs [Fig. 11(a)] with 20~30 GHz bandwidth, the capacitance is around 100~200 fF, which still causes significant bandwidth

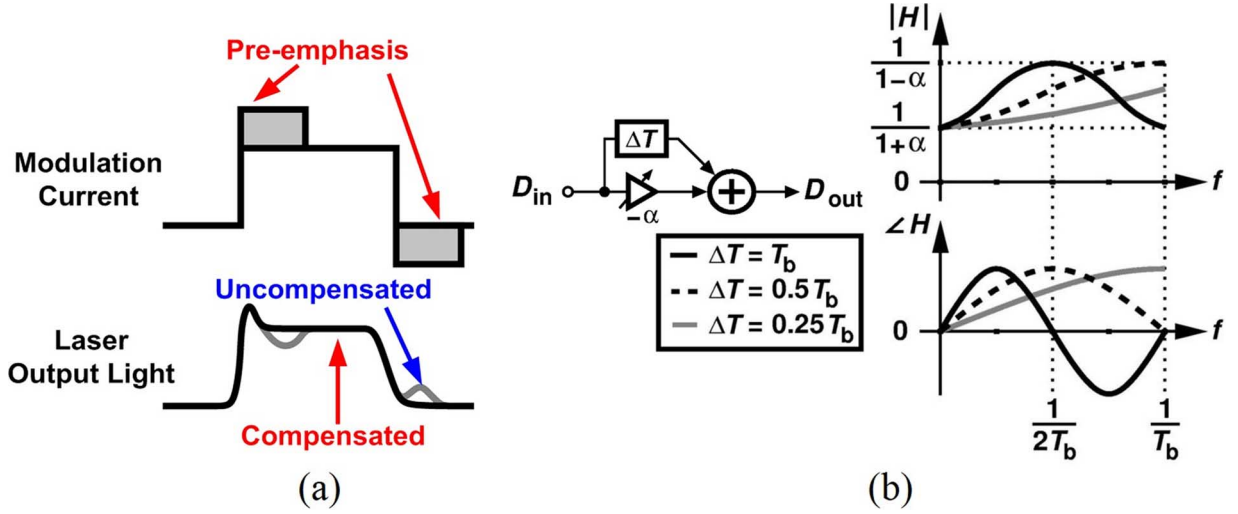


Fig. 10. (a) Relaxation oscillation, (b) two-tap fractional-bit boosting.

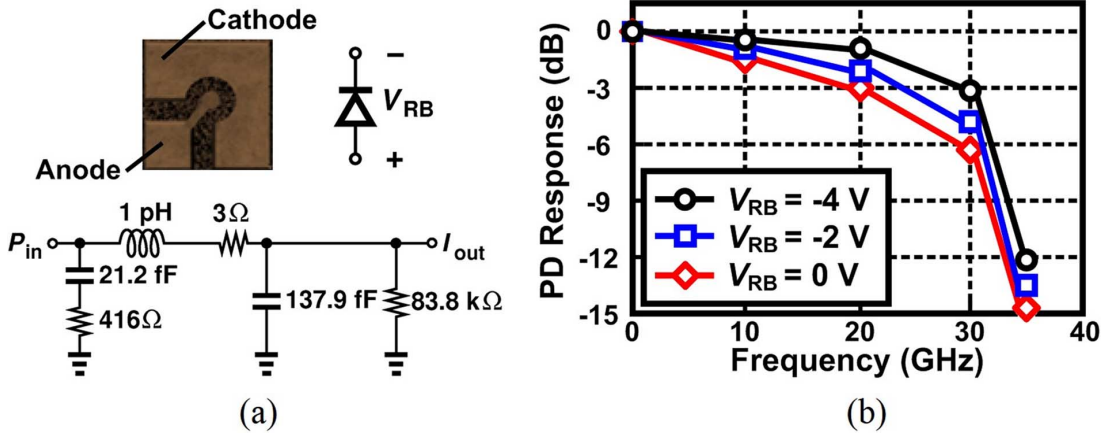
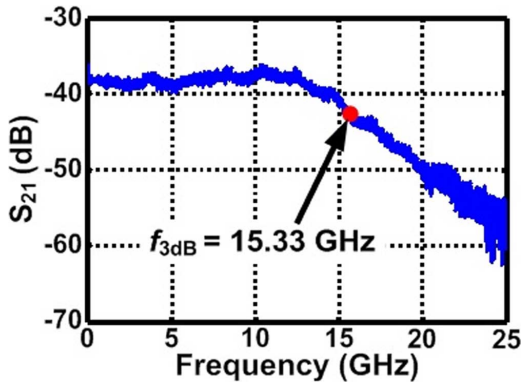


Fig. 11. (a) Photo detector and its small-signal model, (b) measured frequency response.

Fig. 12. Measured S_{21} of optical link (VCSEL + MMF + PD).

degradation. As depicted in Fig. 11(b), the -3 dB bandwidth improves from 20 to 30 GHz as the reverse-biased voltage (V_{RB}) moves from 0 to -4 V. It is worth noting that the breakdown voltage of the PD is around -5 V. As a result, a bandgap reference is mandatory on chip to provide a stable input common-mode level.

To accurately model the optical channel, we measure the frequency response of VCSEL + 10 m multimode fiber + PD (Fig. 12). Here, the VCSEL bias current = 6 mA and PD reverse bias voltage = -3 V. The E-O-E transforming link indicates channel loss as -1.1 dB and the -3 dB bandwidth is only 15.33 GHz. It suggests the use of limiting amplifier and equalizer in the RX.

VI. LDD ARRAY

Fig. 13 shows the LDD array design. To facilitate testing, we have four identical drivers sharing one 12.5 GHz PLL to deliver 4×25 Gb/s output data. Each driver has a built-in $2^7 - 1$ PRBS generator. In real system integration, these blocks can be removed. The two-tap fractional FFE is realized as two tail currents I_0 (main cursor) and I_{-1} (pre-cursor), and the latter is governed by a 2 bit DAC for tuning. A bandgap reference is included to ensure precise current generation. To match 50-Ω input impedance of the VCSEL, the final output stage has one end terminated on chip and the other dc-coupled through bonding wire to VCSEL. A 3 mA standby current

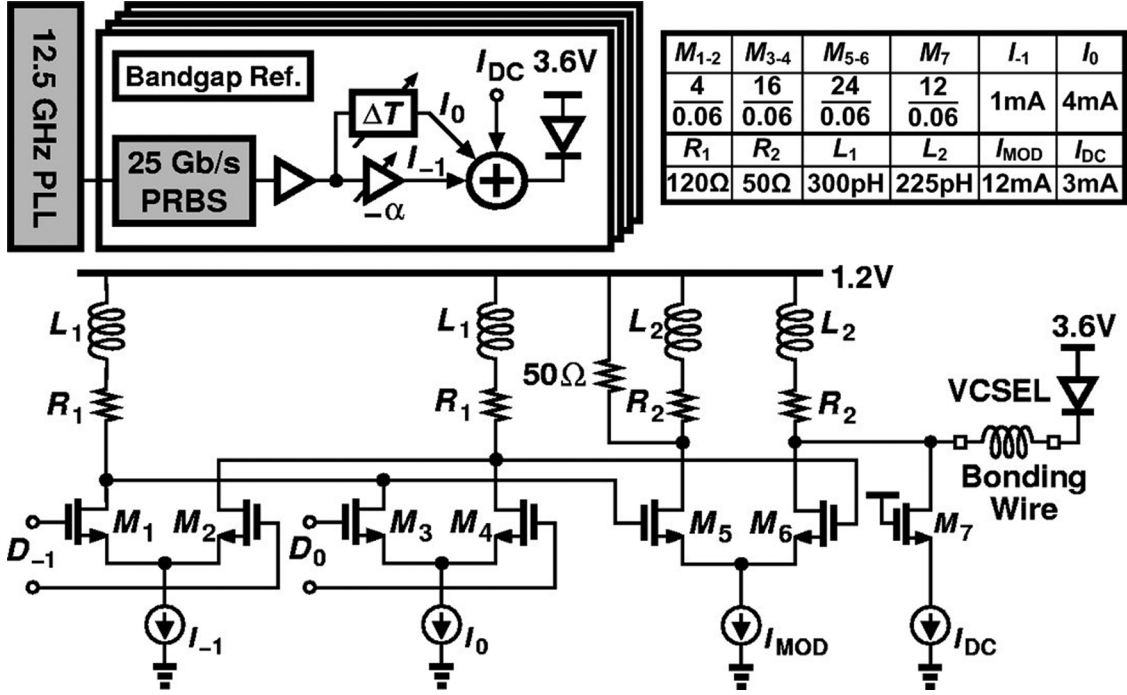
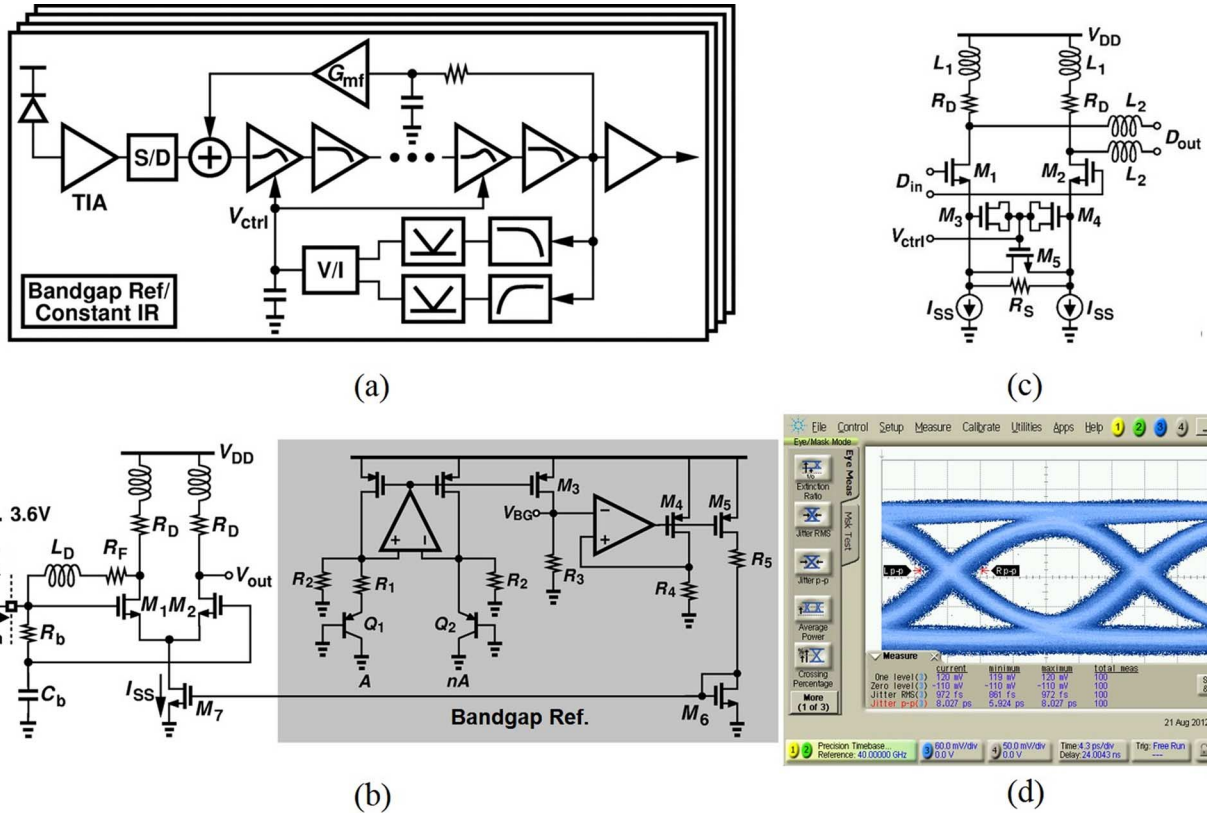


Fig. 13. LDD array.

Fig. 14. (a) TIA/LA array architecture, (b) TIA design with constant IR drop biasing, (c) boosting stage, (d) 40 Gb/s output eye @ $V_{in} = 47$ mV.

(I_{DC}) has been pulled through M_7 for proper operation. M_7 is thick oxide device which can accommodate higher voltages.

VII. TIA/LA ARRAY

The TIA/LA array employs TIAs, adaptive analog equalizers, and limiting amplifiers, as shown in Fig. 14(a). TIA must present

a well-defined input level for direct dc-coupling from photo diode as well as 50 Ω input impedance matching.² The proposed TIA is depicted in Fig. 14(b), where a differential pair $M_{1,2}$

²The 50 Ω matching is not necessary if the PD is wire bonded to TIA directly. However, for discrete components or purely electrical testing, it is still useful to include it.

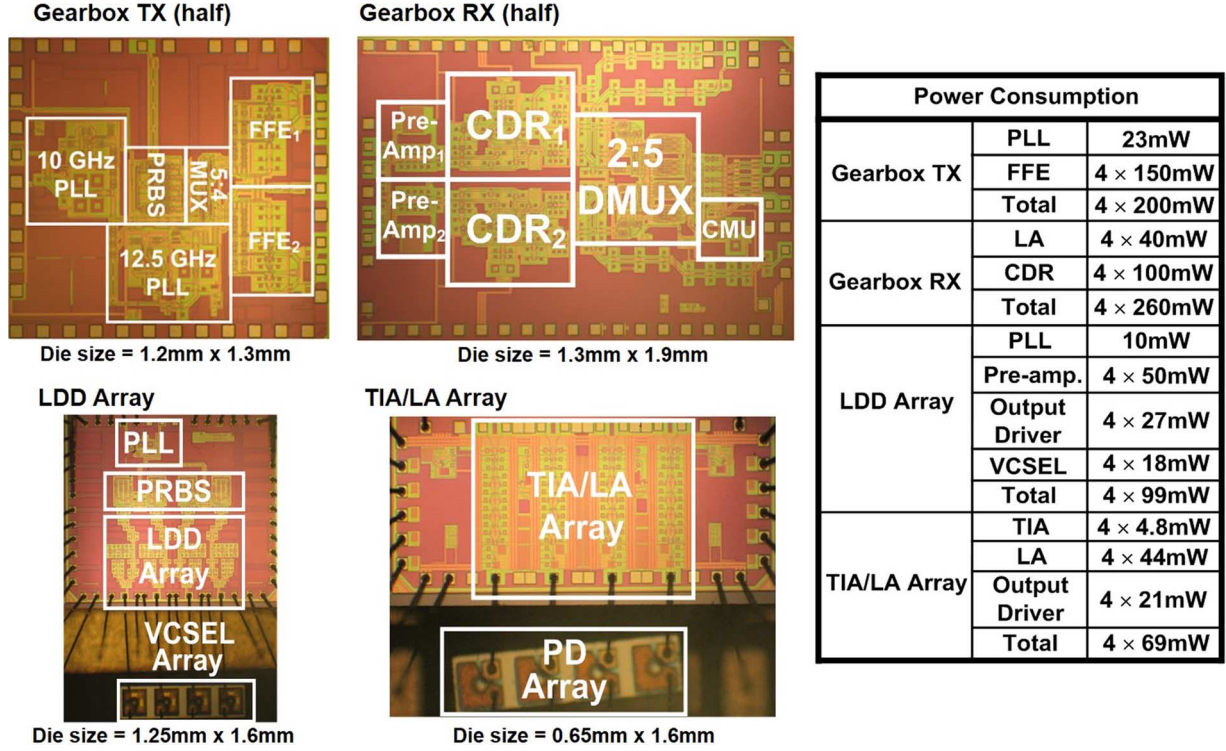


Fig. 15. Chip micrographs and power consumption.

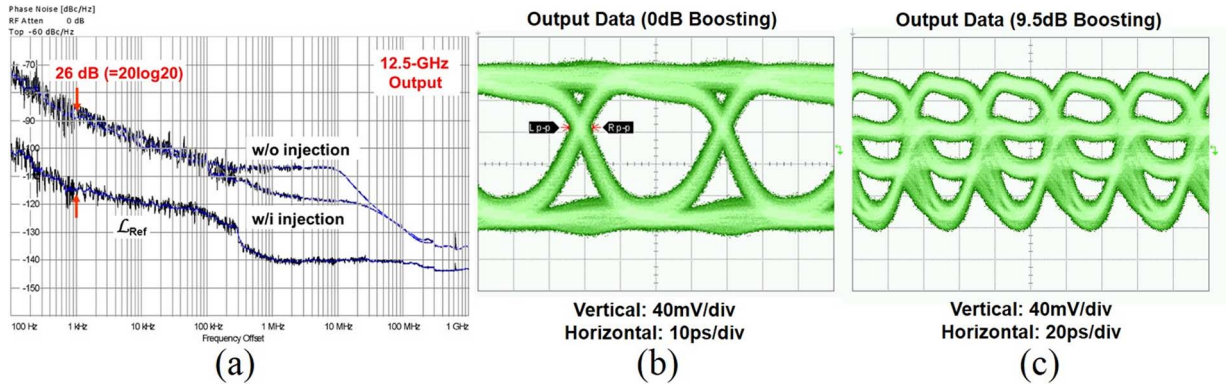


Fig. 16. (a) Gearbox TX PLL phase noise, and 25 Gb/s output data with (b) 0 dB, (c) 9.5 dB boosting.

along with local feedback R_F and L_D forms a fixed input level of $V_{DD} - (I_{SS}R_D)/2 \approx 0.8$ V. The tail current of $M_{1,2}$ pair is biased by a constant IR drop circuit. Here, a sub-1 V bandgap circuit creates a constant voltage V_{BG} :

$$V_{BG} = \ln n \frac{R_3}{R_1} V_T + \frac{R_3}{R_2} \cdot |V_{BE2}| \quad (3)$$

where n is the device ratio between Q_1 and Q_2 . In this design, we set $V_{BG} = 0.7$ V as $R_1 = 1$ k Ω , $R_2 = 12.5$ k Ω , $R_3 = 6.5$ k Ω and $n = 5$. Since V_{BG} is fixed and R_4 is made on chip, the tail current I_{SS} mirrored from M_4 , M_5 , M_6 and M_7 also forms a constant IR drop with R_D . In order words, input DC level is fixed with respect to V_{DD} . A low dropout (LDO) regulator can be used to stabilize the supply. Meanwhile, R_B and C_B provides unaltered bias point to M_2 . As a result, signal current I_{in} flows through R_F , converting current into voltage V_{out} . Here, L_D extends the 50 Ω matching from 23 GHz to 26

GHz, and inductive peaking is also used in the output point to further broaden the bandwidth. TIA reveals 40 dB gain while consuming 4.8 mW of power.

The adaptation of LAs is accomplished by splitting spectrum power and comparing the higher and lower parts, as described in [20]. An on-chip RC filter with corner frequency of 1.5 kHz forms offset cancellation loop. The boosting stage is illustrated in Fig. 14(c), which takes apart the common-source node of $M_{1,2}$ pair and inserts tunable R and C . Each TIA/LA set achieves 72.5 dB Ω gain and 21 GHz bandwidth with 69 mW power consumption. While driven electronically, the TIA/LA itself can be operated at 40 Gb/s with large-signal gain of 68.4 dB Ω [Fig. 14(d)]. VCSEL anodes are powered by a 3.6 V supply to arrive at desired extinction ratio (approximately 4 $\sim$ 5) and thus a symmetric optical data eye. On the other hand, the cathodes of PD array are connected to a 3.6 V supply for optimal performance. The VCSEL and PD capacitance are 350 fF and 150 fF, respectively.

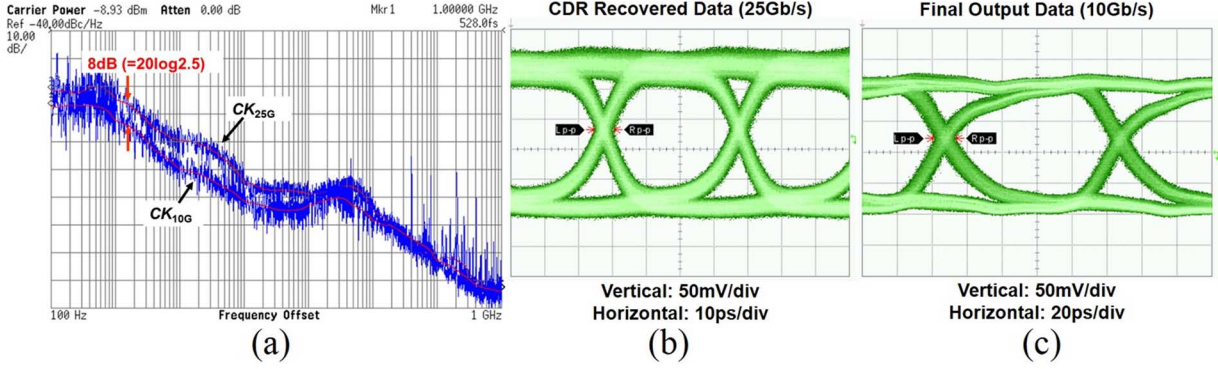


Fig. 17. (a) Gearbox RX CDR phase noise. Recovered and demultiplexed data at (b) 25 Gb/s, (c) 10 Gb/s.

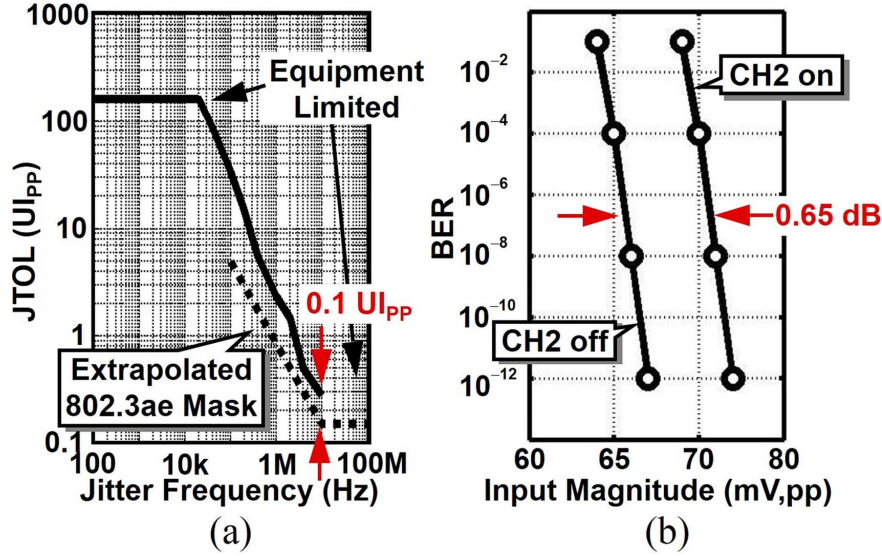


Fig. 18. (a) Gearbox RX jitter tolerance, (b) inter-channel interference.

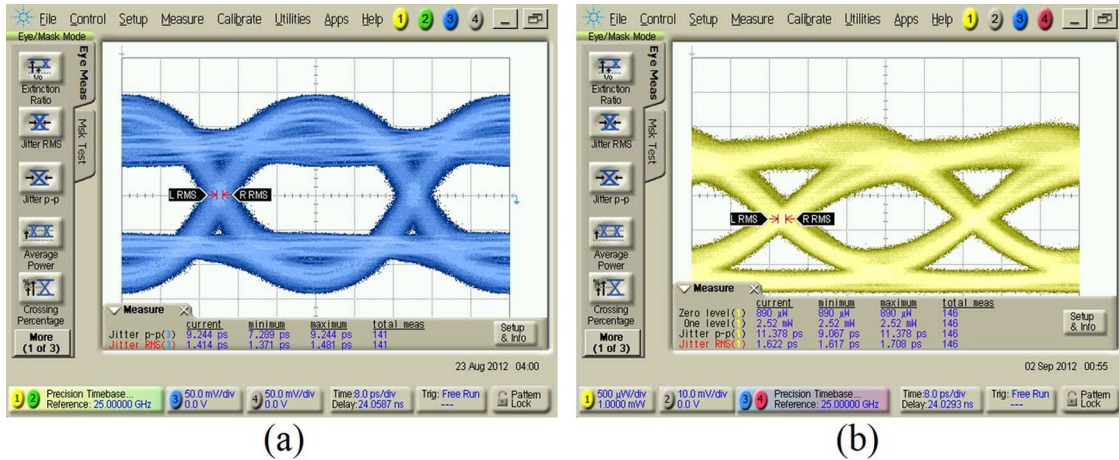


Fig. 19. LDD array's output at 25 Gb/s: (a) electrical, (b) optical.

VIII. MEASUREMENT RESULTS

All chips are fabricated in 65 nm CMOS technology. The 4-channel gearbox TRX consumes a total power of 1.84 W (TX: 4×200 mW, RX: 4×260 mW) from a 1.2 V supply. The LDD and TIA/LA arrays dissipate 4×99 mW and 4×69 mW, respectively. Fig. 15 illustrates the die photos and power consumption of the chips. All of them are tested in a chip-on-board assembly. We present the testing results in the following paragraphs.

1) *Gearbox TX*: Fig. 16(a) depicts the phase noise of the 12.5 GHz PLL in gearbox TX. With the help of injection locking, the rms jitter integrated from 100 Hz to 1 GHz has been reduced from 384 to 187 fs. The reference spur is -80 dBc. Fig. 16(b) and (c) reveals the output data at 25 Gb/s with 0 and 9.5 dB boosting. The single-ended output swing under normal operation (0 dB boosting) is 200 mV_{pp}, while the 20% $\sim 80\%$ rise/fall time is 10.5 ps. The data jitter is 1.0 ps,rms and 6.2 ps,pp, respectively. The TX is capable of delivering

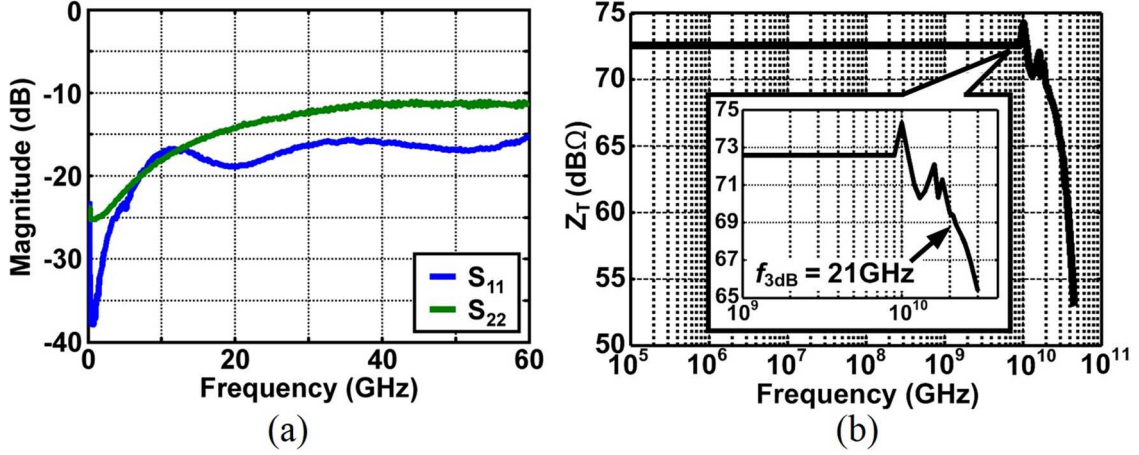


Fig. 20. Measurement results for TIA/LA array: (a) I/O matching, (b) transimpedance gain.

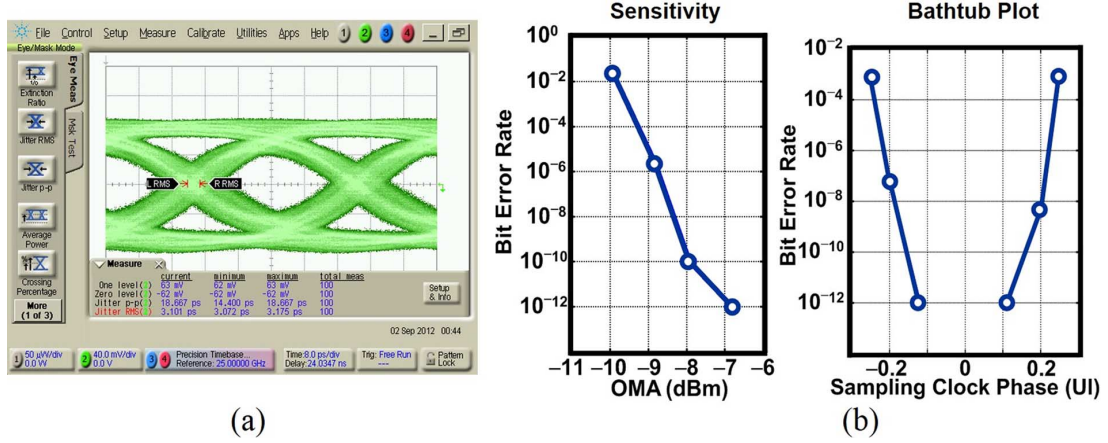


Fig. 21. (a) TIA/LA output with optical input at -5.5 dBm OMA, (b) TIA/LA sensitivity and bathtub curve at -5.5 dBm OMA.

25 Gb/s data to LDD array through a 10-cm PCB channel on a regular FR4 board. The TX presents a tunable range of 24.6 to 25.7 Gb/s.

2) *Gearbox RX*: The spectrum of CDR recovered clock (25 GHz) is plotted in Fig. 17(a), which presents a phase noise of -98.3 dBc/Hz at 1 MHz offset. The sub-rate clock (10 GHz) generated on-chip is also recorded for comparison. The recovered data at 25 Gb/s and 10 Gb/s are depicted in Fig. 17(b) and (c), revealing rms jitter of 1.01 ps and 2.34 ps, respectively. Jitter tolerance is also measured with bit-error rate (BER) = 10^{-12} as threshold. It exceeds the extrapolated 802.3ae Mask by at least 0.1 UI_{pp} [Fig. 18(a)]. Inter-channel interference measurement suggests an input power penalty of only 0.65 dB when the adjacent lane is turned on [Fig. 18(b)]. This result improves significantly as compared with our previous work [16], primarily owing to better substrate isolation. The RX reveals a tunable range of 24.94 to 25.2 Gb/s, and BER $< 10^{-12}$ is achieved.

3) *LDD Array*: Fig. 19 shows the electrical (directly to oscilloscope) and optical (through VCSEL and optical probe) outputs at 25 Gb/s, suggesting output power of 250 mV_{pp} and 1.63 mW, respectively. The jitter measures 1.4 ps,rms and 9.2 ps,pp for the electrical output, and 1.6 ps,rms and 11.4 ps,pp for the optical. Here, the LDD jitter is captured with all four

channels turned on. Jitter could be further reduced if only one channel is activated.

4) *TIA/LA Array*: Fig. 20(a) shows the measured S₁₁ and S₂₂ for TIA/LA array, presenting at least < -12 dB return loss from dc to 60 GHz. The transimpedance gain measures 72.5 dBΩ and the -3 dB bandwidth is equal to 21 GHz [Fig. 20(b)]. The low-frequency cutoff corner is less than 1.5 kHz. End-to-end test for optical link is also conducted, where the VCSEL emits 1.2 mW 850 nm light into a 100 m MMF for TIA/LA to pick up. With 0.5 W/A VCSEL efficiency and 0.47 A/W PD responsivity, we obtain the output data as illustrated in Fig. 21(a). The input referred noise is equal to 4.2 μ A_{rms}. TIA/LA signal integrity is demonstrated in Fig. 21(b). It suggests a sensitivity of -6.8 dBm optical modulation amplitude (OMA) at 25 Gb/s for BER = 10^{-12} , and ± 0.12 UI opening in the bathtub curve. Performance of this work has been summarized in Table I and compared with that of other state-of-the-arts recently published.

IX. CONCLUSION

Advanced CMOS technologies together with broadband circuit techniques have pushed optical and electrical transceivers toward high data rate and lower power dissipation. E/O

TABLE I
PERFORMANCE SUMMARY

Gearbox TX				LDD Array			
	This Work	[8]	[11]		This Work	[21]	[22]
Clock Phase Noise (Carrier = 12.5GHz, @ 1-MHz offset)	-116dBc/Hz	-106dBc/Hz	N/A	Laser Output Power (OMA)	1.63mW	0.77mW	N/A
Integrated Clock Jitter (12.5GHz)	187fs (100Hz~1GHz)	429fs (10kHz~100MHz)	350fs (100kHz~1GHz)	Output Data Jitter @ BER = 10^{-12}	1.6ps,rms* 11.4ps,pp*	16ps,pp	25.2ps,pp
Output Data Jitter @ BER = 10^{-12}	1.01ps,rms 6.67ps,pp	3.3ps,pp	N/A	Commercial VCSEL?	Yes	No	No
D_{out} Rise/Fall Time (20%- 80%)	10.5ps	25ps	22ps	VCSEL parasitic capacitance	350fF	N/A	N/A
Operation Range	24.6 ~ 25.7Gb/s	25.78Gb/s	25~28Gb/s	VCSEL Efficiency	0.5W/A	N/A	N/A
D_{out} Swing (Single-ended)	200mV _{pp}	355mV _{pp}	276mV _{pp}	Power Consumption	99mW/lane	46mW/lane	208mW/lane
Power Consumption	200mW/lane	282mW/lane	N/A*	TIA/LA Array			
Gearbox RX				Transimpedance Gain	72.5dBΩ	78.3dBΩ**	71.2dBΩ
Recovered Clock Phase Noise(Carrier=12.5GHz, @ 1-MHz offset)	-98.3dBc/Hz	N/A	N/A	Output Data Jitter @ BER = 10^{-12}	3.1ps,rms 18.7ps,pp	19.2ps,pp	N/A
Recovered Data Jitter (25Gb/s, @ BER = 10^{-12})	1.01ps,rms 6.22ps,pp	N/A	N/A	Sensitivity @ BER = 10^{-12}	-6.8dBm @ 25Gb/s	-4dBm @ 22Gb/s	N/A
Power Penalty	0.63dB	N/A	N/A	Commercial PD?	Yes	No	No
Jitter Tolerance	0.2UI _{pp}	N/A	0.4UI _{pp}	PD parasitic capacitance	150fF	80fF	N/A
Tolerable phase error between lanes	±7bit	N/A	N/A	PD Responsivity	0.47A/W	0.55A/W	N/A
Operation Range	24.94 ~ 25.2Gb/s	N/A	N/A	Power Consumption	68mW/lane	44.4mW/lane	59mW/lane
Power Consumption	260mW/lane	217mW/lane	N/A*	Power supply, Area and Process			
Power supply, Area and Process				Supply Voltage	1.2V	1.0V/1.6V	1.0V/1.8V/2.5V
Supply Voltage	1.2V	1.0V/1.8V	N/A	Chip Area	LDD: $1.6 \times 1.25\text{mm}^2$ TIA/LA: $1.6 \times 0.65\text{mm}^2$	LDD: $0.8 \times 0.17\text{mm}^2$ *** TIA/LA: $0.25 \times 0.39\text{mm}^2$ ***	$3.6 \times 5.3\text{mm}^2$
Chip Area	TX: $1.2 \times 1.1 \times 2\text{mm}^2$ ** RX: $1.9 \times 1.3 \times 2\text{mm}^2$ **	$6.3 \times 3.7\text{mm}^2$	$2.4 \times 1.5\text{mm}^2$	Technology	65nm CMOS	65nm CMOS	40nm CMOS
Technology	65nm CMOS	65nm CMOS	40nm CMOS	*The optical bandwidth of oscilloscope is 19GHz **Simulated result ***Core circuit area			

*Total power consumption of TX+RX is 900mW

**Calculated for 4x25Gb/s operation

and O/E interfaces can also be implemented and integrated in CMOS as well, demonstrating promising potential for low-cost, low-power, high-performance, and high-yield solution for 100GbE systems.

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