2.3 A 20Gb/s Burst-Mode CDR Circuit Using Injection-Locking Technique

Jri Lee, Mingchung Liu

National Taiwan University, Taipei, Taiwan

A fast locking technique manifests itself in applications that require burst-mode operation and impose no strict specification on jitter transfer, such as passive optical networks (PONs). The design and experimental verification of a 20Gb/s CDR circuit based on injection-locking technique in 90nm CMOS technology is described.

Figure 2.3.1 shows the proposed CDR architecture. The D_{in} input and its delayed replica, D'_{in}, are XORed to create pulses upon occurrence of data transition, leading to instantaneous locking to the subsequent VCOs. The pulse width is adjustable by means of a variable-delay buffer so as to achieve an optimal injection. Two identical oscillators, VCO_1 and VCO_2, are coupled in cascade to purify the clock. In contrast to the gating circuit in [1], this 2-stage coupling ensures constant amplitude in output clock CK_{out}, and suppresses more noise by the filtering nature of the LC tanks. Driven by CK_{out}, the flipflop retimes the input data with proper phase alignment, since the falling edge of the clock locates right in the center of the data eye. The skews caused by the intermediate buffers and imbalanced routing can be compensated by selecting an appropriate data delay from the variable-delay buffer.

It is important to note that the deviation of the natural frequency of the VCO due to PVT variations may considerably exceed the injection-locking range. That is, using a fixed control voltage [2] results in substantial jitter or even out of lock, necessitating a frequency-tracking mechanism. In this design, a reference PLL that contains another duplicated VCO (i.e., VCO_3) is introduced to generate a proper voltage (V_{ctrl}) for VCO_1 and VCO_2. Such a control voltage reproduces itself as V'_{ctrl} by a unity-gain buffer before sending into VCO_1 and VCO_2, facilitating further fine tuning on the frequency offset. This architecture could easily accommodate a wide operation range. A bypass capacitor, C_P=10pF, is placed to stabilize V'_{ctrl} without disturbing the loop filter of the reference PLL. A PFD is employed to ensure minimum ripple on the control line.

Since the transition of a random data sequence is still random, the spectrum of the pulses generated by the XOR gate resembles that of a return-to-zero (RZ) data, as illustrated in Fig. 2.3.2. It consists of a square of sinc function with strong clock spectral lines at data rate and the harmonics, providing a vigorous injection to the subsequent VCOs. The normalized magnitude of $1/T_b$ line can be expressed as $(\sin x\ \pi)/\pi$, where x represents the relative pulse width and $0<x<1$. As a result, a difference of $T_b/2$ between the 2 inputs of the XOR results in a strongest injection. Transistor-level simulation suggests a $1/T_b$ line of −9.78dBm in this design, which is more than $10^4\times$ larger than that induced from leakage [3].

The VCO is depicted in Fig. 2.3.3(a), where the injection pair M_1-M_2 translates the input signals into currents to lock the oscillators. The clock buffer is designed to present an input capacitance approximately equal to that of the VCOs. The pulling between the 2 VCOs is so strong that (1) they oscillate at the same frequency; (2) the overall locking range is primarily determined by the coupling between the XOR gate and VCO_1. Verified with measurement, the locking range is 22MHz. One significant advantage of the cascaded VCOs is that VCO_2 produces an output with almost constant amplitude, mainly because VCO_1 swings even during long runs. In contrast to the single VCO [2] or gated VCO [1] that may suffer from significant clock fluctuations, this design stabilizes the sampling in the flipflop and improves signal integrity. Current-mode logics with peaking inductors are employed in flipflop, XOR gate (Fig. 2.3.3(b)), and buffers, to extend the bandwidth. The inductors are realized as 3-layer stacked spirals to compact the layout and ease the routing. For example, a 0.5nH inductor occupies $14\times14\mu m^2$.

The proposed PLL consists of a 20GHz oscillator VCO_3, a chain of frequency dividers (÷128), a PFD based on SSB mixers along with V/I converters, and a high-order loop filter. Figure 2.3.4 shows the PFD design. The phase detection is accomplished by mixing 2 quadrature signals, one from the reference input (CK_{ref}, provided by a static divide-by-2 circuit) and the other from the last divider stage (CK_{div}). The phase detector distills the phase error with a sinusoidal characteristic and the V/I converter pumps a proportional current into the loop filter and changes the control voltage accordingly. Since no pulse-width comparison is involved, it achieves a truly quiet phase examination and control-line ripples due to reference feedthrough can be significantly reduced. Note that finite "image" would be observed at f_{ref} in the presence of mismatches, necessitating a low-pass filter to further suppress it. Simulation shows that the control line displays a ripple of 20μV. The frequency error can be discerned by introducing another SSB mixer, resulting in 2 orthogonal outputs V_{PD} and V_2. Whether the former is leading or lagging the latter depends on the sign of frequency error, which can be easily obtained by sampling one signal with the other in a flipflop. The automatic switching-off function of the frequency detection loop is preserved [4] by applying *ENFD* to $(V/I)_{FD}$ and making it disabled when the loop is locked.

The CDR is fabricated in 90nm CMOS technology and tested on a high-speed probe station. The chip consumes 175mW from a 1.5V supply, where 102mW is dissipated in the CDR core, 70mW in the reference PLL, and 3mW in the unity-gain buffer. The reference PLL exhibits an operation range of 800MHz and spurs of less than −60dBc.

Figure 2.3.5 shows the recovered data and clock (single-ended waveforms) in response to continuous-mode PRBS of length 2^7-1 and $2^{31}-1$, suggesting data jitters of $1.27ps_{rms}/8.0ps_{pp}$ and $1.87ps_{rms}/13.77ps_{pp}$, respectively. The recovered clock jitter is recorded as $1.2ps_{rms}$. The burst-mode operation is verified by compiling the input data pattern as that in [1] and having it preceded and followed by long runs of 500 bits. The input-output waveforms around the edge of data arrival are plotted in Fig. 2.3.6, demonstrating an immediate locking without any missing bit. The CDR circuit achieves a BER of $<10^{-9}$ in both continuous ($2^{31}-1$ PRBS) and burst modes. The free-running and injection-locked spectra of VCO_2 exhibit noise-shaping phenomenon and suggest a lock range of 22MHz for a fixed control voltage. Note that the CDR achieves a wide tunable range of 800Mb/s, across which no performance degradation is observed. Figure 2.3.7 shows a micrograph of the die that occupies $0.8\times1.2mm^2$ including pads.

Acknowledgments:
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References:
[1] M. Nogawa, K. Nishimura, S. Kimura, et al., "A 10Gb/s Burst-Mode CDR IC in 0.13μm CMOS," *ISSCC Dig. Tech. Papers*, pp. 228-229, Feb., 2005.
[2] J. Zhan, J.S. Duster, K.T. Kornegay, "A Full-Rate Injection-Locked 10.3Gb/s Clock and Data Recovery Circuit in a 45GHz-f_T SiGe Process," *Proc. CICC*, pp. 557-560, Sept., 2005.
[3] T. Gabara, "A 3.25Gb/s Injection Locked CMOS Clock Recovery Cell," *Proc. CICC*, pp. 521-524, Sept., 1999.
[4] Jri Lee, "High-Speed Circuit Designs for Transmitters in Broadband Data Links," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1004-1015, May, 2006.

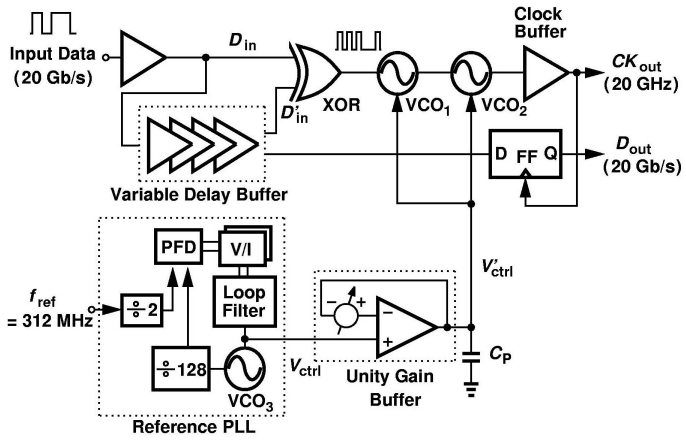

Figure 2.3.1. CDR architecture.

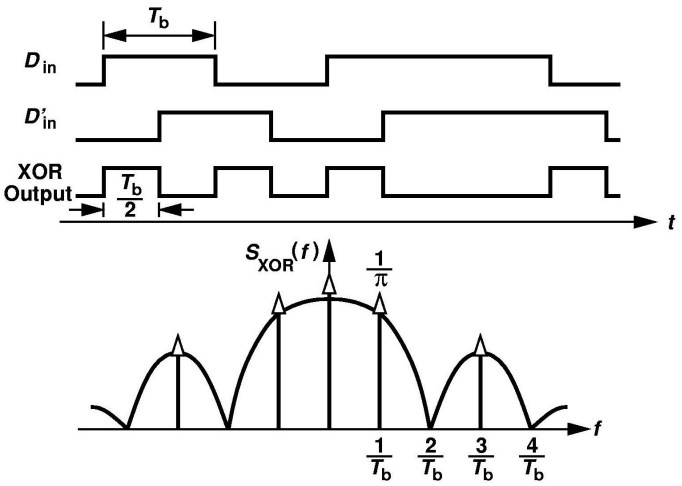

Figure 2.3.2. XOR output and spectrum.

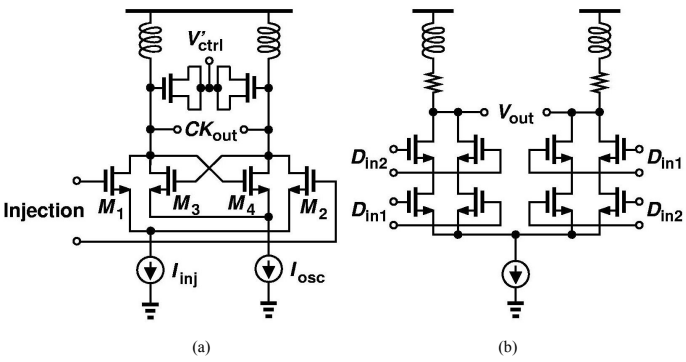

Figure 2.3.3. Realization of (a) VCO (b) XOR gate.

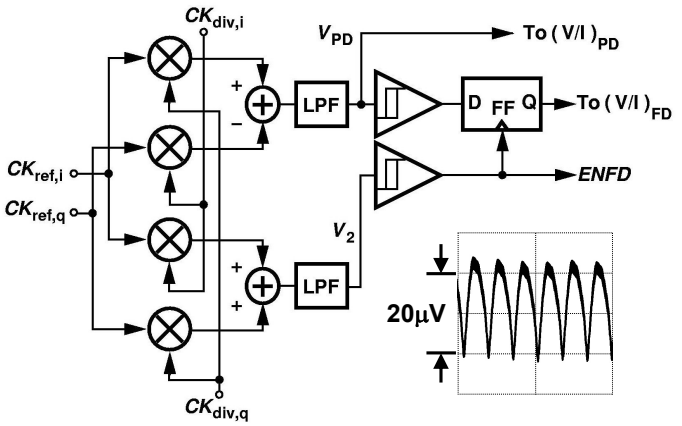

Figure 2.3.4. PFD design and control-line waveform.

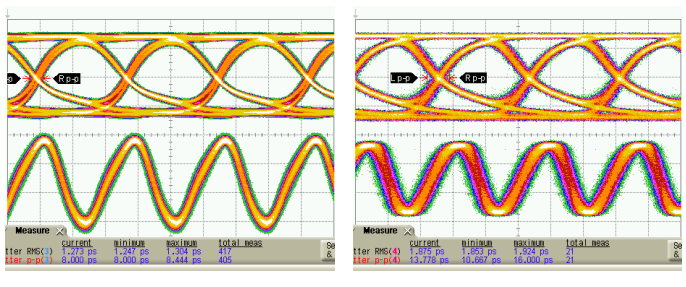

Figure 2.3.5. Recovered data and clock for (a)2^7-1 (b)2^{31}-1 PRBS (horizontal scale: 20ps/div, vertical scale: 100mV/div).

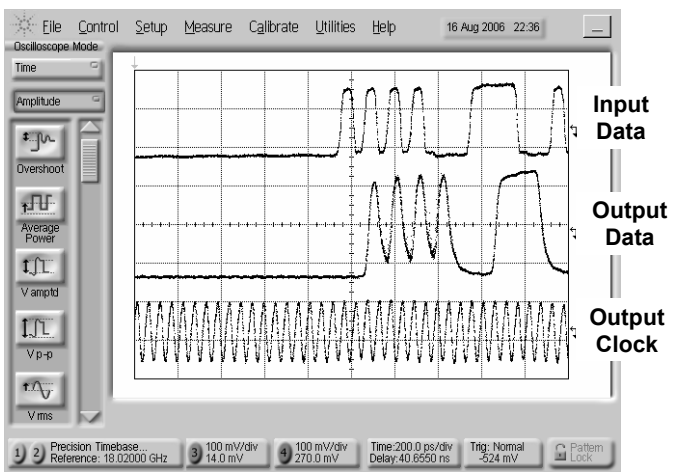

Figure 2.3.6. Measured burst-mode waveforms (horizontal scale: 200ps/div, vertical scale: 100mV/div).

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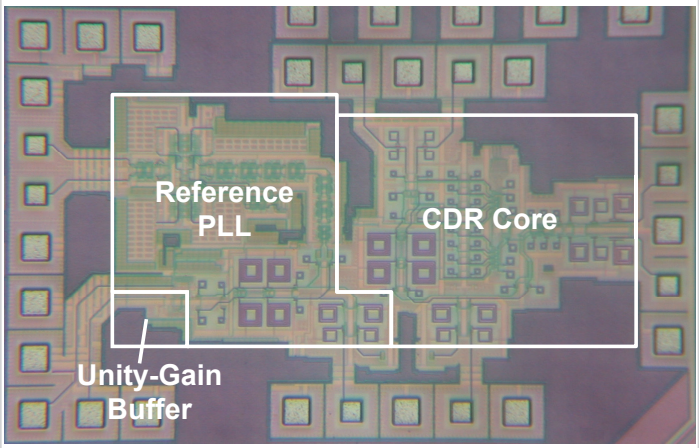

Figure 2.3.7. Chip micrograph.

