4.7 A 20Gb/s Adaptive Equalizer in 0.13µm CMOS Technology

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High-speed equalizers have found extensive usage in modern broadband data communications. Recent researches have reported 10Gb/s adaptive equalizers in 0.13µm CMOS and 150GHz BiCMOS technologies [1, 2]. However, advanced military or instrumental applications require equalizers to operate at even higher frequencies. Conventional designs would suffer from limited bandwidth, poor adaptability, and inadequate boosting at high speed. More importantly, the use of slicers [1, 2, 3] would limit the maximum speed, since the slicer is to generate a clean unaffected waveform for comparison. Realizing such a slicer becomes extremely difficult as the data rate approaches a significant portion of the device f_T.

In this paper, an approach to alleviate the above difficulties is proposed. For an ideal random binary data, the normalized spectrum can be expressed as:

$$S_x(f) = T_b\left[\frac{\sin(\pi f T_b)}{\pi f T_b}\right]^2, \quad (1)$$

Where T_b denotes the bit period of the data stream, and:

$$\int_0^\infty S_x(f)df = \frac{1}{2}. \quad (2)$$

To restore the waveform properly, an equalizer must present an output spectrum as close as an ideal one. In other words, the output of the equalizer can be examined to determine whether the high-frequency part is under or over compensated and adjust the boost accordingly. Note that the slicer is no longer needed here and issues such as imbalanced swings are fully eliminated.

To decompose the spectrum, a frequency f_m that splits the spectrum into 2 parts with equal power is specified (Fig. 4.7.1). That is,

$$\int_0^{f_m} S_x(f)df = \int_{f_m}^\infty S_x(f)df = \frac{1}{4}, \quad (3)$$

arriving at $f_m = 0.28/T_b$. Denoting the power above and below f_m as P_H and P_L, respectively, the spectra of 3 different conditions are shown in Fig. 4.7.1. Note that for a dc-balanced data pattern such as 8B/10B coding, the dc power vanishes, resulting in a slightly higher f_m.

Based on the foregoing observation, the equalizer can be realized as shown in Fig. 4.7.2. Here, two voltage-controlled boosting stages interspersed with gain buffers are cascaded to provide large boosting at high frequencies, and the output is directly fed into the power detector (PD). The equalizing filter is designed to achieve a maximum peaking of 20dB at 10GHz. A compact design of power detector compares the average power of low and high frequencies (P_L and P_H) by means of the (first-order) low- and high-pass filters along with a high-gain rectifier. Rather than an integrator in conventional designs, a V/I converter and a capacitor C_p follow the power detector, generating the appropriate control voltage for the equalizing filter. Such a configuration obviates the need for high-gain error amplifier and preserves flexibility for offset cancellation. It can be shown that the feedback loop remains stable unconditionally, and a simple capacitor C_p is sufficient to serve as a loop filter. Note that the instantaneous ratio of P_H and P_L depends on the input data pattern, and the control voltage would "drift" if the data stream experiences a very high or low transition density. A large on-chip C_p of 3pF is used to minimize this effect.

To equalize 20Gb/s data, the equalizing filter must provide a wide bandwidth and large boosting at high frequencies. A popular approach incorporates a resistively loaded pair with capacitive-degeneration technique to generate tunable boosting [3]. This topology, however, produces only one zero in each stage, leading to limited bandwidth and consequently insufficient compensation at high frequencies. A modified version employs inductive peaking in the output, introducing one more zero and extending the high-frequency boost. To further broaden the bandwidth and enlarge the boost, a filter stage, as shown in Fig. 4.7.3, is proposed. Modified from the Cherry-Hooper amplifier [4], this circuit still employs capacitive degeneration and inductive peaking, but increases the bandwidth and boosting by 2.2GHz and 1.2dB, respectively, as compared with the design in [1] rescaled for the same speed and power consumption.

The power detector compares the low- and high-frequency power and generates the result in voltage with reasonable swings. Conventional rectifiers take the common-source node of a differential pair as output [1, 2]. This topology suffers from small output swing, e.g., a few mV at 20Gb/s, primarily due to the parasitic capacitance at the common-source node. Such a weak signal necessitates a high-gain error amplifier, increasing the power dissipation. In addition, the offset of the amplifier may overwhelm this tiny output signal and severely degrade the performance. As depicted in Fig. 4.7.4, the proposed power detector incorporates 2 RC filters with the same corner frequency to distill the high- and low-frequency signals. For an input data rate of 20Gb/s, R_1C_1 = 28.4ps, but various R_1 and C_1 values could be used to accommodate different data rates and patterns. The high- and low-frequency components convert themselves to power by steering the tail current through a transistor quad, M_1-M_4, and the output is smoothened by capacitor C_2. Simulation shows that the output magnitude is 10-times larger than that of conventional designs. Figure 4.7.5 shows the V/I converter. A tunable resistor R_2 nominally equal to R_1 is used here to cancel out the static offset due to mismatches and channel-length modulation. Note that the required input common-mode levels in Fig. 4.7.4 and 4.7.5 are generated by the 10kΩ resistors.

The equalizer is fabricated in 0.13µm CMOS technology. Inductive-peaking technique is applied to the input termination network, maintaining the 50Ω on-chip termination up to 50GHz. The circuit is tested on a high-speed probe station with Anritsu random data generator providing the input. Figure 4.7.6 shows the measured data eyes at 20Gb/s before and after equalization for 1m and 5m AWG18 coaxial cable with a PRBS of 2^{31}–1. The rms jitter measures 3.2ps and 3.0ps, respectively, in the presence of an intrinsic rms jitter of 1.2ps generated by the pattern generator. The maximum peak-to-peak jitter is equal to 14ps while the pattern generator itself suffers from a peak-to-peak jitter of 7ps. The equalizer achieves error-free operation over 12 hours, suggesting a BER of $<10^{-15}$. The circuit consumes 60mW from a 1.5V supply. Figure 4.7.7 shows the die micrograph, the chip occupies 0.8×0.25mm^2.

Acknowledgments:
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References:
[1] S.Gondi, et al., "A 10Gb/s CMOS Adaptive Equalizer for Backplane Applications," *ISSCC Dig. Tech. Papers*, pp 328-329, Feb., 2005.
[2] G. Zhang, et al., "A BiCMOS 10Gb/s Adaptive Cable Equalizer," *ISSCC Dig. of Tech. Papers*, pp. 482-483, Feb., 2004.
[3] Y. Tomina, et al., "A 10Gb/s Receiver with Equalizer and On-Chip ISI Monitor in 0.11-∝m CMOS," *Symp. VLSI Circuits*, pp. 202-205, June, 2004.
[4] E. M. Cherry and D. E. Hooper, "The Design of Wideband Transistor Feedback Amplifiers," *Proc. IEE*, vol. 110, pp. 375-389, Feb., 1963.

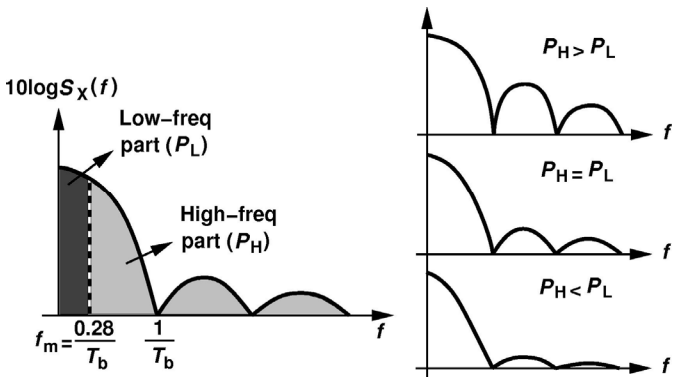


Figure 4.7.1: (a) Spectrum decomposition (b) different compensations.

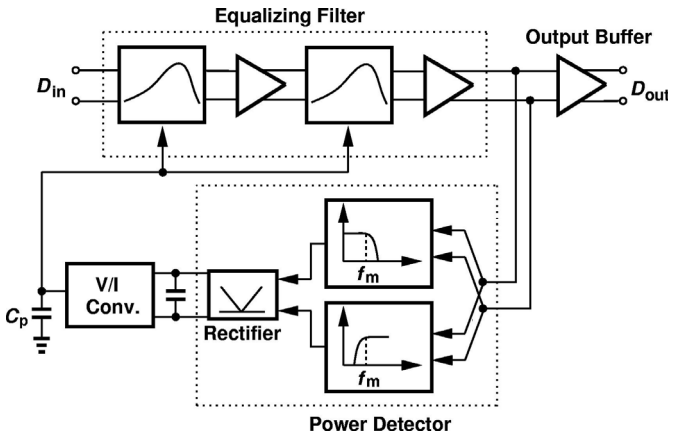


Figure 4.7.2: Equalizer architecture.

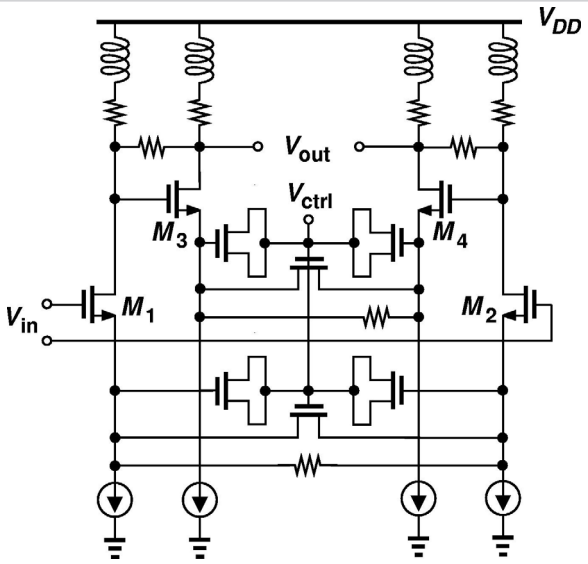


Figure 4.7.3: Equalizing filter stage.

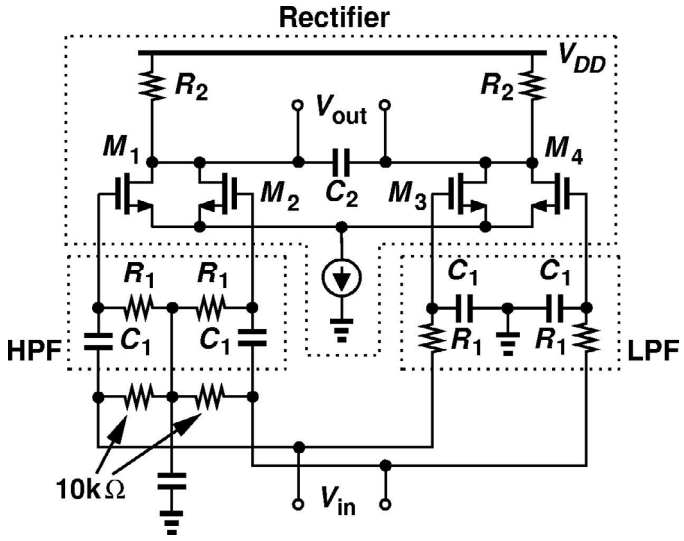


Figure 4.7.4: Power detector.

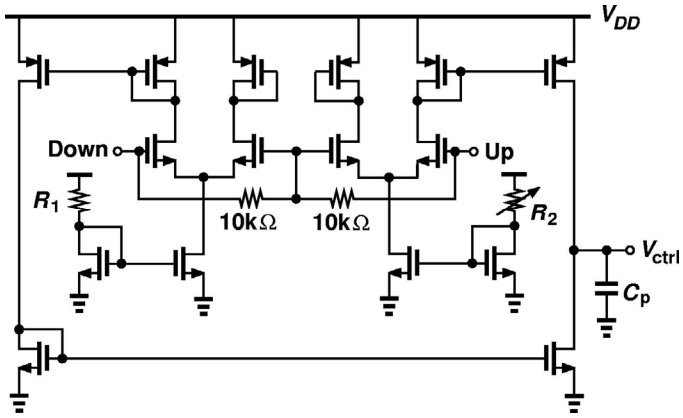


Figure 4.7.5: V/I converter.

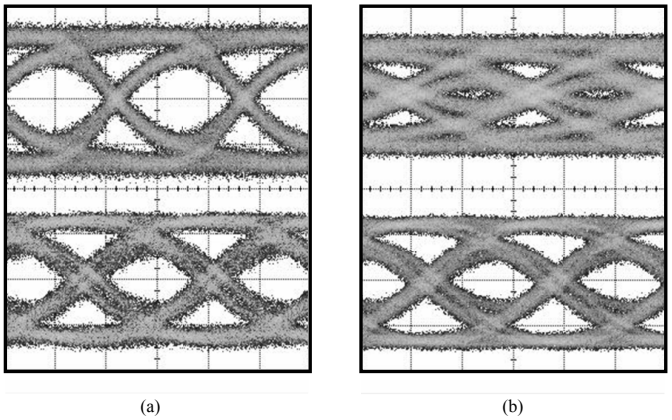


Figure 4.7.6: Measured waveforms before (upper) and after (lower) equalization at 20Gb/s for (a) 1m (b) 5m AWG18 cables (horizontal scale: 20ps/div, vertical scale: 50mV/div).

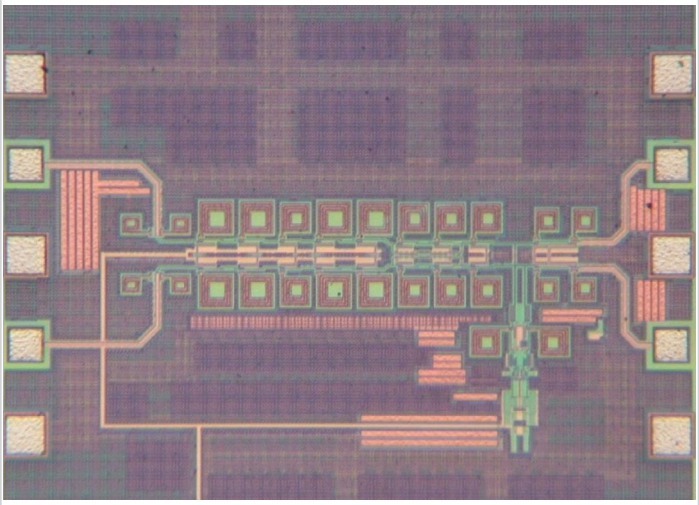
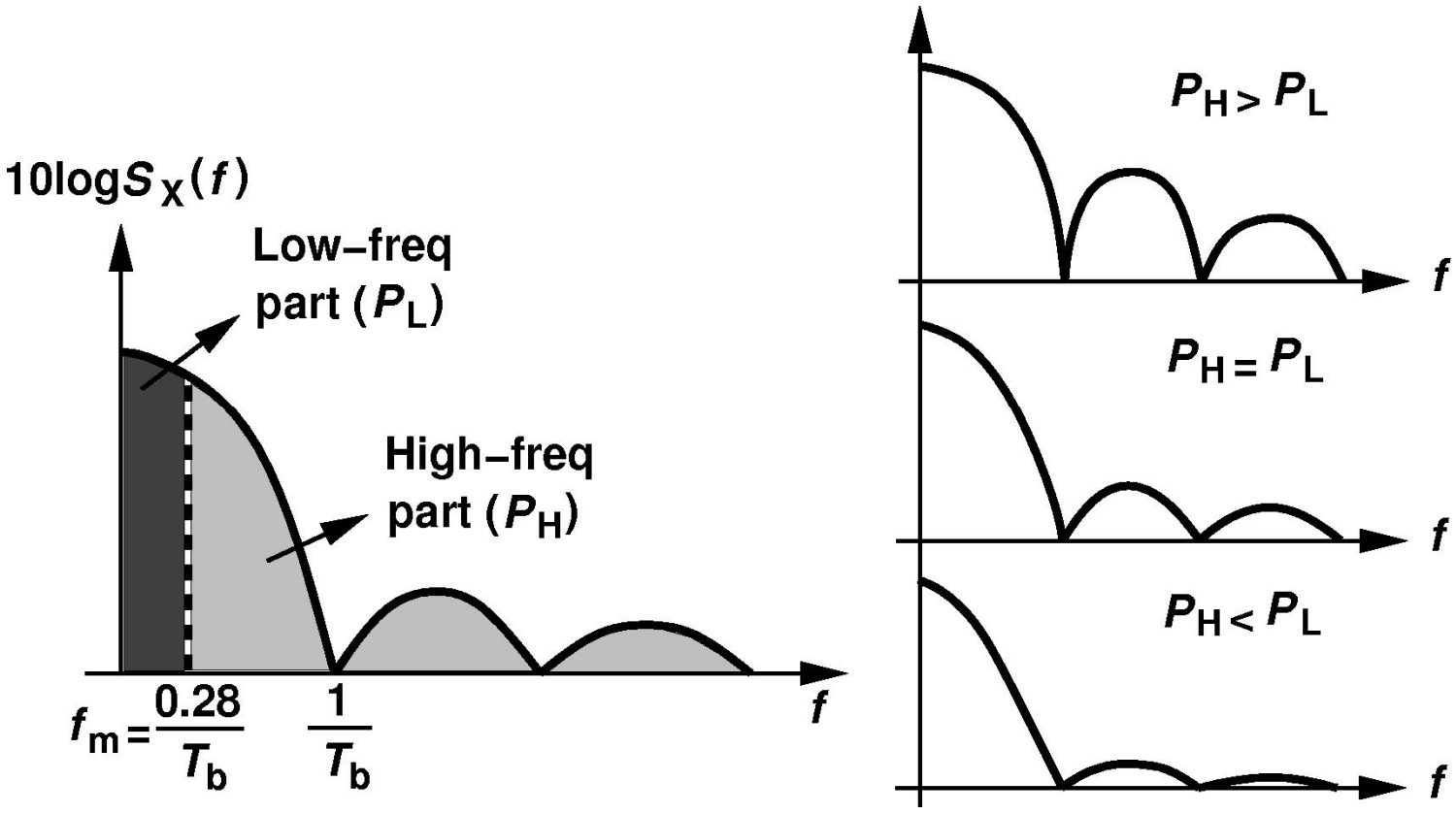


Figure 4.7.7: Chip micrograph.



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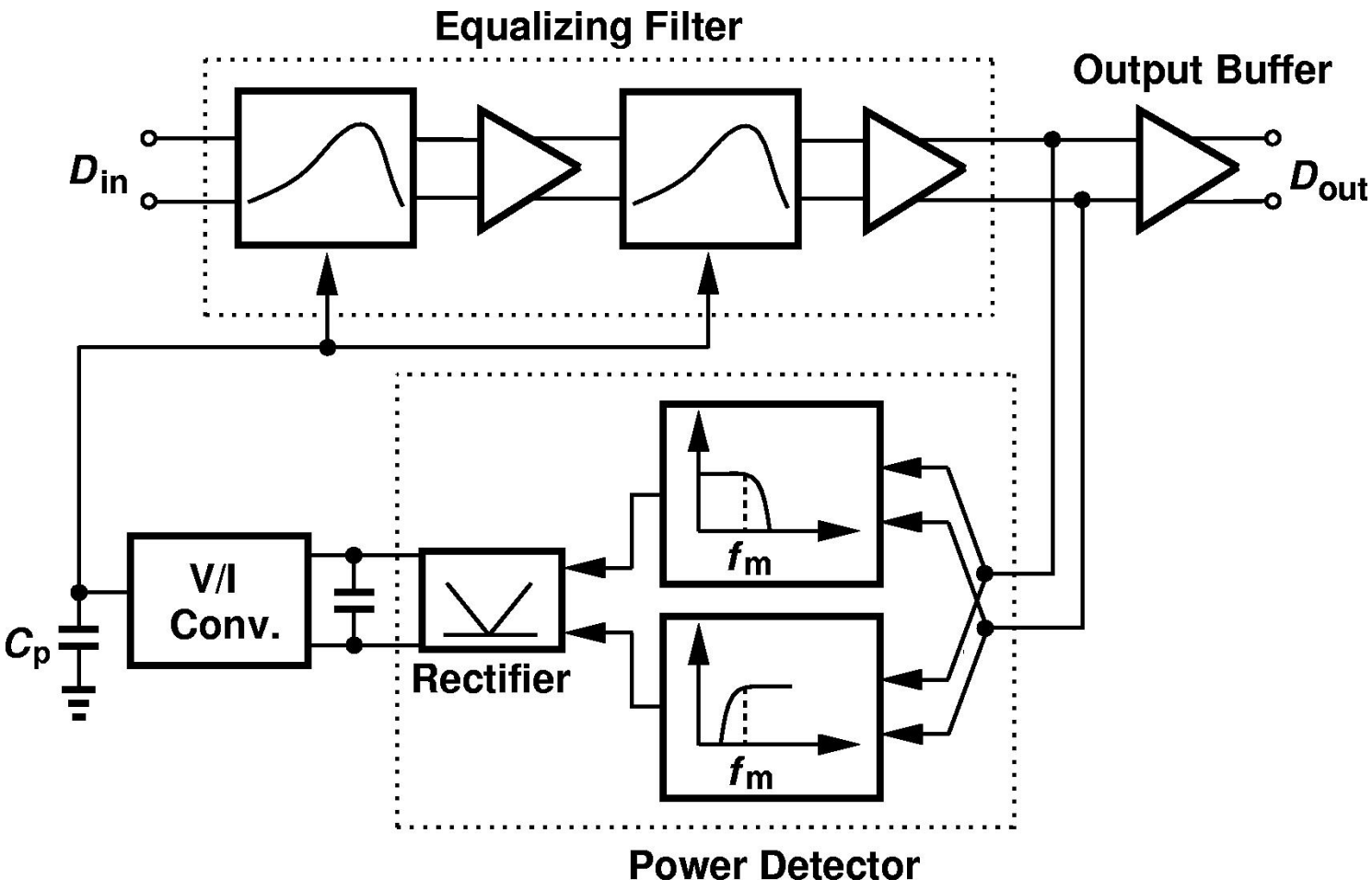

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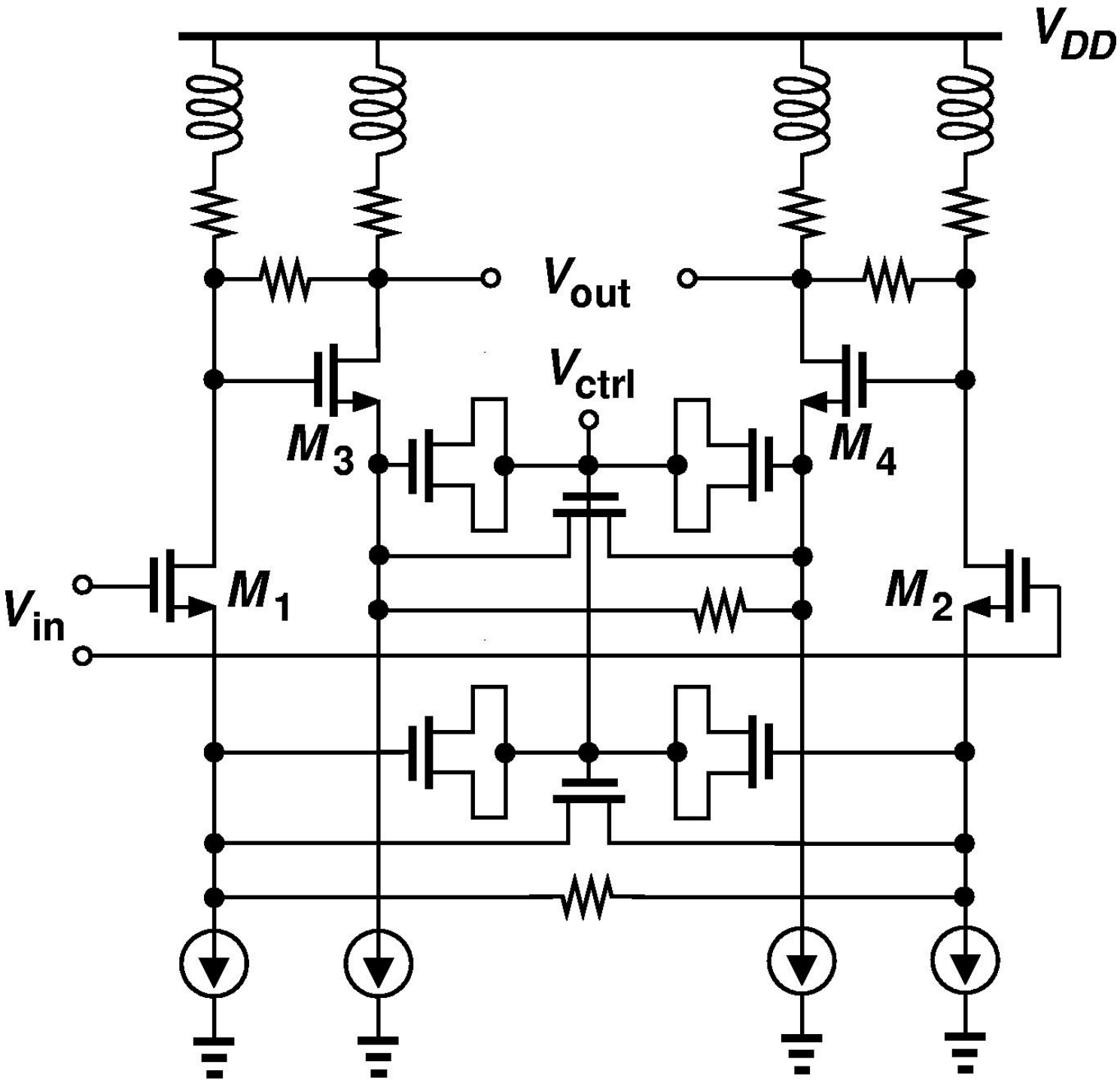
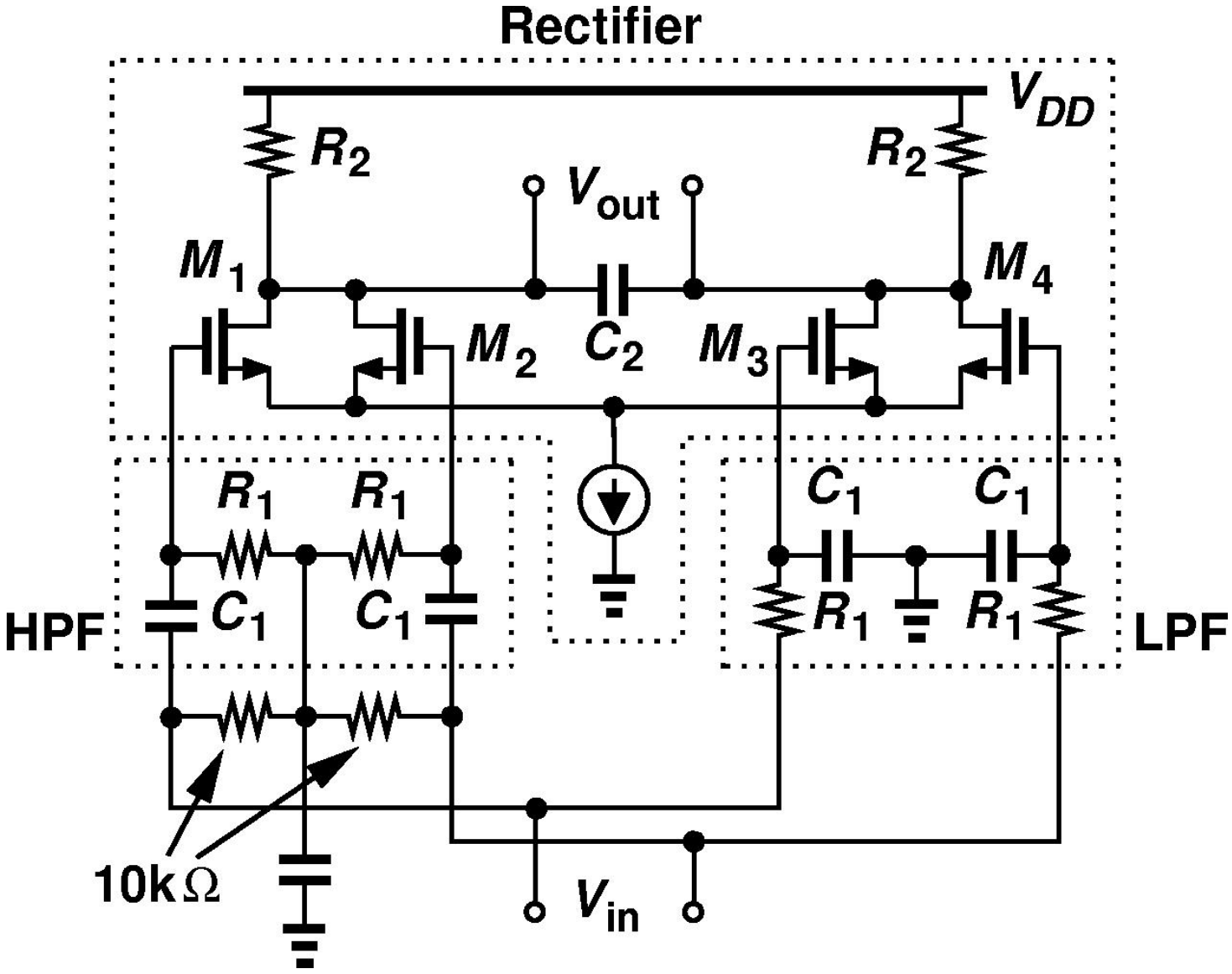


Figure 4.7.3: Equalizing filter stage.



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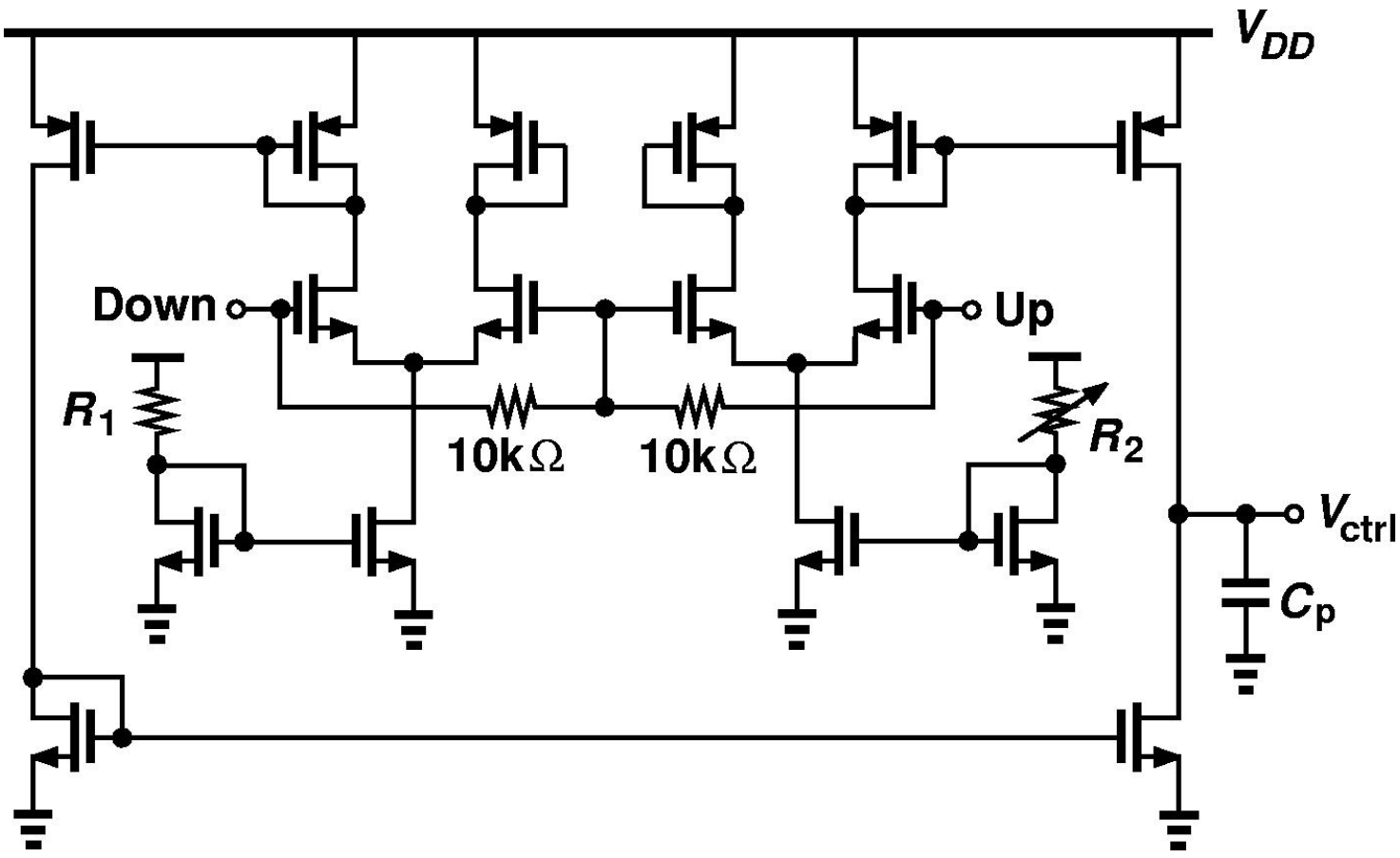

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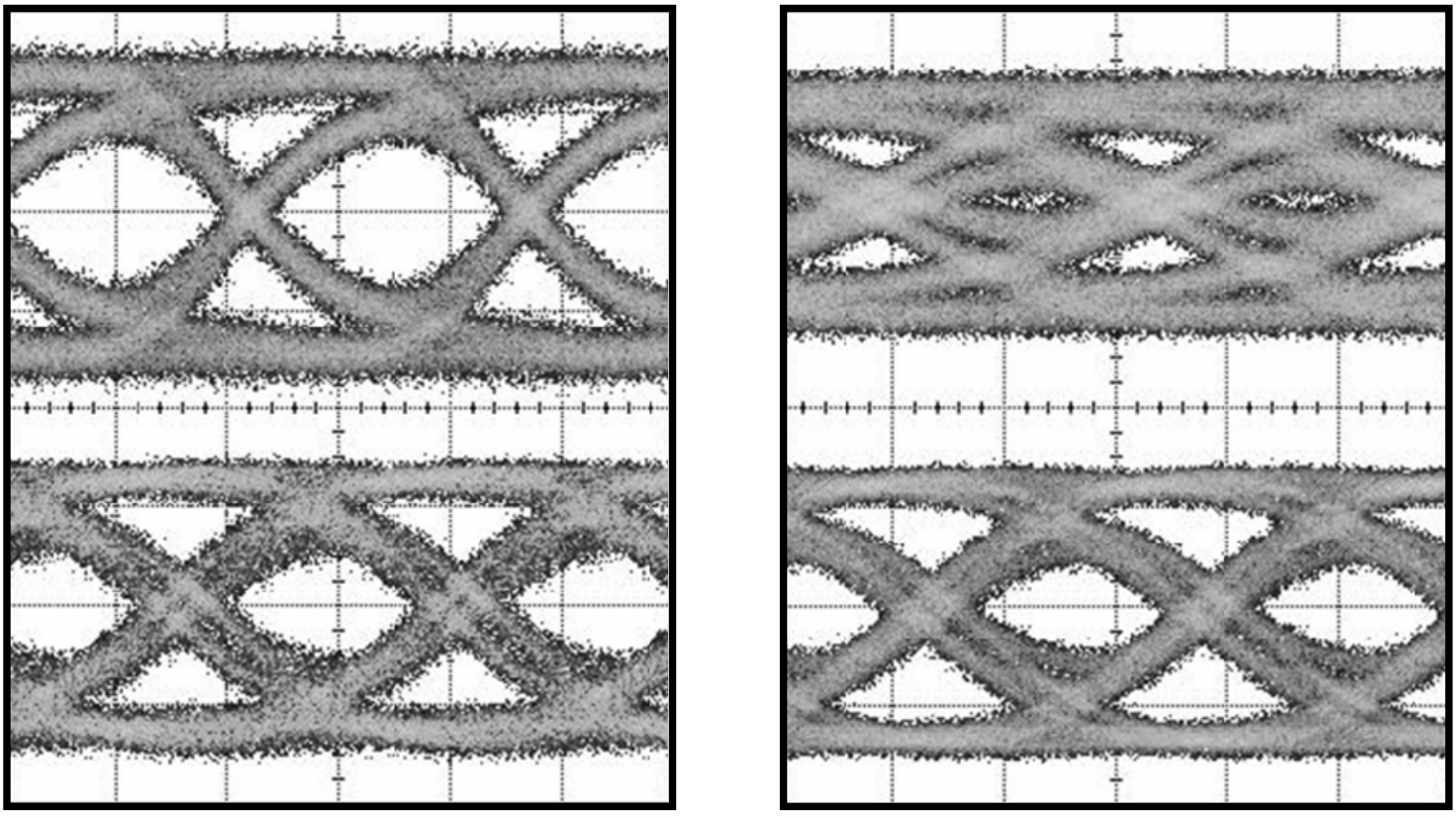

(a) (b)

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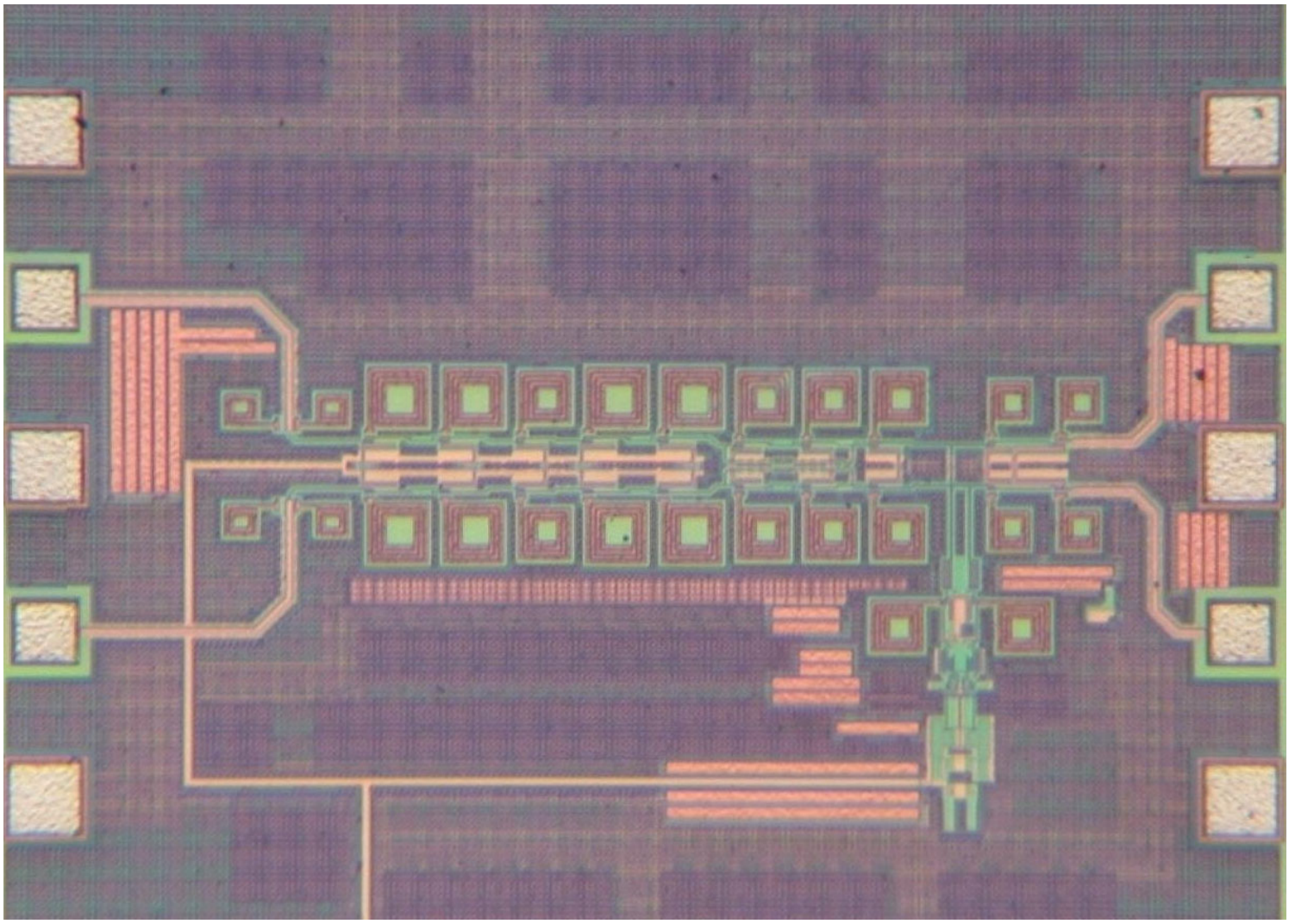

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